Precision Hall-Effect Angle Sensor IC

Discontinued Product

These parts are no longer in production The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: December 5, 2018

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, refer to the A1338 Family.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

ALLEGRO microsystems

Precision Hall-Effect Angle Sensor IC

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Contactless 0° to 360° angle sensor IC, for angular position, rotational speed, and direction measurement
- Available with either a single die or dual independent die housed within a single package
- Circular Vertical Hall (CVH) technology provides a single-channel sensor system, with air-gap independence
- 12-bit resolution possible in low RPM mode, 10-bit resolution in high RPM mode
- Angle Refresh Rate (output rate) configurable between 25 and 3200 μs through EEPROM programming
- Capable of sensing magnet rotational speeds in excess of 7600 rpm
- SPI interface allows use of multiple independent sensors for applications requiring redundancy
- EEPROM programmable angle reference (0°) position and rotation direction (CW or CCW)
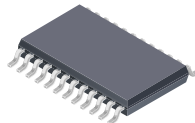- Absolute maximum V_{CC} of 26.5 V for automotive battery-powered applications

Packages:

Not to scale
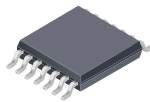
Single SoC
14-pin TSSOP (LE package)

Dual Independent SoCs
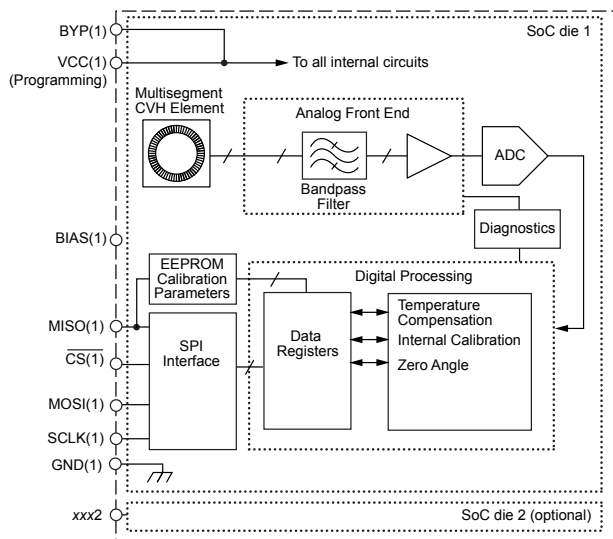**24-pin TSSOP (LE package)**

DESCRIPTION

The A1334 is a 360° angle sensor IC that provides contactless high-resolution angular position information based on magnetic Circular Vertical Hall (CVH) technology. It has a system-on-chip (SoC) architecture that includes: a CVH front end, digital signal processing, and a digital (SPI) output. The A1334 is ideal for automotive applications requiring high-speed 0° to 360° angle measurements, such as electronic power steering (EPS) and throttle systems.

The A1334 supports a Low RPM mode for slower rate applications and a High RPM mode for high-speed applications. High RPM mode is for applications that require higher refresh rates to minimize error due to latency. Low RPM mode is for applications that require higher resolution operating at lower angular velocities.

As part of its signal processing functions, the A1334 includes automotive-grade temperature compensation to provide accurate output over the full operating temperature and voltage ranges. The A1334 also includes EEPROM technology for end-of-line calibration.

The A1334 is available as a single die in a 14-pin TSSOP, or dual die in a 24-pin TSSOP. Both packages are lead (Pb) free with 100% matte-tin leadframe plating.

A1334 Functional Block Diagram

Pin number parentheses refer to chip in dual SoC variant
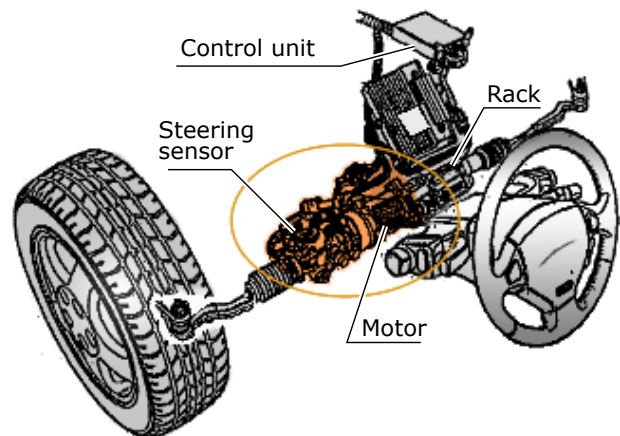
A1334 in Electronic Power Steering (EPS) Application

Selection Guide

Part Number	System Die	Package	Packing*	Notes
A1334LLETR-T	Single	14-pin TSSOP	4000 pieces per 13-in. reel	Optimized for 900 G Field
A1334LLETR-60-T	Single	14-pin TSSOP	4000 pieces per 13-in. reel	Optimized for 600 G Field
A1334LLETR-30-T	Single	14-pin TSSOP	4000 pieces per 13-in. reel	Optimized for 300 G Field
A1334LLETR-DD-T	Dual	24-pin TSSOP	4000 pieces per 13-in. reel	Optimized for 900 G Field
A1334LLETR-DD55-T	Dual	24-pin TSSOP	4000 pieces per 13-in. reel	Optimized for 550 G Field
A1334LLETR-DD30-T	Dual	24-pin TSSOP	4000 pieces per 13-in. reel	Optimized for 300 G Field

*Contact Allegro™ for additional packing options.
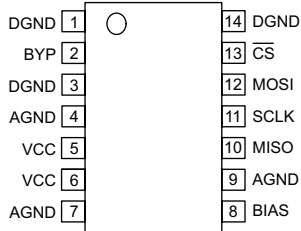
SPECIFICATIONS

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Not sampling angles	26.5	V
Reverse Supply Voltage	V_{RCC}	Not sampling angles	−18	V
All Other Pins Forward Voltage	V_{IN}		5.5	V
All Other Pins Reverse Voltage	V_R		0.5	V
Operating Ambient Temperature	T_A	L range	−40 to 150	ºC
Maximum Junction Temperature	$T_J(max)$		165	ºC
Storage Temperature	T_{stg}		−65 to 170	ºC

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LE-14 package	82	ºC/W
		LE-24 package	117	ºC/W

*Additional thermal information available on the Allegro website.

Pin-Out Diagrams and Terminal List Table

**LE-14 Package (Single SoC)**

DGND	1		14	DGND
BYP	2		13	$\overline{CS}$
DGND	3		12	MOSI
AGND	4		11	SCLK
VCC	5		10	MISO
VCC	6		9	AGND
AGND	7		8	BIAS

**LE-14 Package
(Single SoC)**

LE-24 Package (Dual SoC)

DGND_1	1		24	DGND_1
BYP_1	2		23	$\overline{CS}$_1
DGND_1	3		22	MOSI_1
AGND_1	4		21	SCLK_1
VCC_1	5		20	MISO_1
AGND_1	6		19	BIAS_1
BIAS_2	7		18	AGND_2
MISO_2	8		17	VCC_2
SCLK_2	9		16	AGND_2
MOSI_2	10		15	DGND_2
$\overline{CS}$_2	11		14	BYP_2
DGND_2	12		13	DGND_2
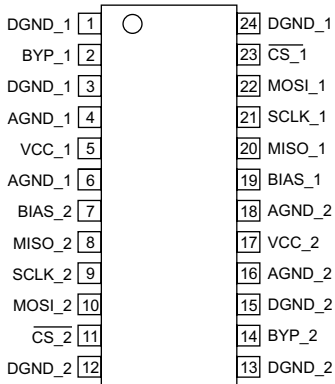
**LE-24 Package
(Dual SoC)**

Terminal List Table

PinName	Pin Number		Function
	LE-14	LE-24	
AGND_1	4, 7, 9	4, 6	Device analog ground terminal (die 1)
AGND_2	–	16, 18	Device analog ground terminal (die 2)
BYP_1	2	2	External bypass capacitor terminal for internal regulator (die 1)
BYP_2	–	14	External bypass capacitor terminal for internal regulator (die 2)
$\overline{CS}$_1	13	23	SPI Chip Select terminal, active low (die 1)
$\overline{CS}$_2	–	11	SPI Chip Select terminal, active low (die 2)
DGND_1	1, 3, 14	1, 3, 24	Device digital ground terminal (die 1)
DGND_2	–	12, 13, 15	Device digital ground terminal (die 2)
MISO_1	10	20	SPI Master Input / Slave Output (die 1)
MISO_2	–	8	SPI Master Input / Slave Output (die 2)
MOSI_1	12	22	SPI Master Output / Slave Input (die 1)
MOSI_2	–	10	SPI Master Output / Slave Input (die 2)
SCLK_1	11	21	SPI Clock terminal (die 1)
SCLK_2	–	9	SPI Clock terminal (die 2)
VCC_1	5, 6	5	Power supply; also used for EEPROM programming (die 1)
VCC_2	–	17	Power supply; also used for EEPROM programming (die 2)
BIAS_1	8	19	Bias connection; connect to ground (shown) or pull-up to 3.3 V (die 1)
BIAS_2	–	7	Bias connection; connect to ground (shown) or pull-up to 3.3 V (die 2)
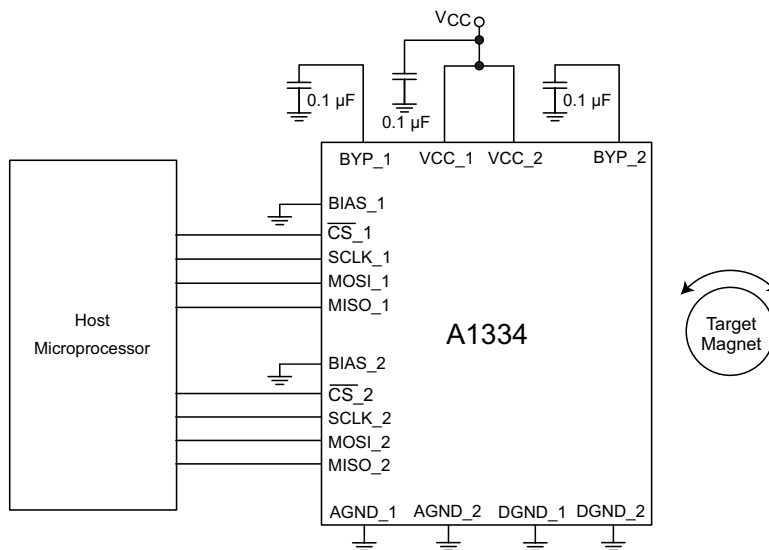
Typical Application Diagram (Dual Die Version)
Either or both internal SoCs can be operated simultaneously. (See page 12 for circuits that require a higher level of EMC immunity.)

OPERATING CHARACTERISTICS: valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit[2]
Electrical Characteristics						
Supply Voltage	V_{CC}		4.5	12	14.5	V
Supply Current	I_{CC}	Each die, A1334 sampling angles	–	7.5	10	mA
Undervoltage Lockout Threshold Voltage[3]	V_{UVLOHI}	Maximum V_{CC}, dV/dt = 1V/ms, T_A = 25°C, A1334 sampling enabled	–	–	4.5	V
	$V_{UVLOLOW}$	Maximum V_{CC}, dV/dt = 1V/ms, T_A = 25°C, A1334 sampling disabled	3.5	–	–	V
VCC Low Flag Threshold[4,5]	V_{UVLOTH}		4.35	4.5	4.75	V
Supply Zener Clamp Voltage	V_{ZSUP}	I_{CC} = I_{CC} + 3 mA, T_A = 25°C	26.5	–	–	V
Reverse-Battery Current	I_{RCC}	V_{RCC} = –18 V, T_A = 25°C	–5	–	–	mA
Power-On Time[6,8]	t_{PO}		–	300	–	µs
Bypass Pin Output Voltage[7]	V_{BYP}	T_A = 25°C, C_{BYP} = 0.1 µF	2.45	2.85	3.4	V
SPI Interface Specifications						
Digital Input High Voltage[8]	V_{IH}	MOSIx, SCLKx, $\overline{CS}$x pins	2.8	–	3.63	V
Digital Input Low Voltage[8]	V_{IL}	MOSIx, SCLKx, $\overline{CS}$x pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	MISOx pins, C_L = 50 pF, T_A = 25°C	2.81	3.3	3.79	V
SPI Output Low Voltage	V_{OL}	MISOx pins, C_L = 50 pF, T_A = 25°C	–	0.3	0.5	V
SPI Clock Frequency[8]	f_{SCLK}	MISOx pins, C_L = 50 pF	0.1	–	10	MHz
SPI Frame Rate[8]	t_{SPI}		5.8	–	588	kHz
Chip Select to First SCLK Edge[8]	t_{CS}	Time from $\overline{CS}$x going low to SCLKx falling edge	50	–	–	ns
Data Output Valid Time[8]	t_{DAV}	Data output valid after SCLKx falling edge	–	40	–	ns
MOSI Setup Time[8]	t_{SU}	Input setup time before SCLKx rising edge	25	–	–	ns
MOSI Hold Time[8]	t_{HD}	Input hold time after SCLKx rising edge	50	–	–	ns
SCLK to CS Hold Time[8]	t_{CHD}	Hold SCLKx high time before $\overline{CS}$x rising edge	5	–	–	ns
Load Capacitance[8]	C_L	Loading on digital output (MISOx) pin	–	–	50	pF
Magnetic Characteristics						
Magnetic Field[9,10]	B	Range of input field	300	–	1000	G
Missing Magnet Flag	MAGM			100	–	G
Angle Characteristics						
Output[11]	RES_{ANGLE}		–	12	–	bit
Effective Resolution[12]		B = 300 G, T_A = 25°C, ORATE = 0	–	10.7	–	bits
Angle Refresh Rate[8,13,14]	t_{ANG}	High RPM mode [18]	–	25	28.33	µs
		Low RPM mode, AVG = 011 (varies with AVG mode, refer to the appendix *Programming Reference*)	–	200	–	µs
Response Time[8]	$t_{RESPONSE}$	High RPM mode (see figure 4) [18]	–	60	68	µs

Continued on the next page…

OPERATING CHARACTERISTICS (continued): valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit[2]
Angle Characteristics (continued)						
Angle Error[15]	ERR$_{ANG}$	T_A = 25°C, ideal magnet alignment, B = 300 G, target rpm = 0	–	±0.6	–	degrees
		T_A = 150°C, ideal magnet alignment, B = 300 G, target rpm = 0	−1.75	–	1.75	degrees
Angle Noise[16, 19]	N$_{ANG}$	T_A = 25°C, B = 300 G, no internal filtering	–	0.2	–	degrees
		T_A = 150°C, no internal filtering, B = 300 G, target rpm = 0	–	0.27	–	degrees
Temperature Drift	ANGLE$_{DRIFT}$	T_A = -40°C, B = 300 G	–	±1.5	–	degrees
		T_A = 150°C, B = 300 G	−1.5	–	1.5	degrees
Angle Drift Over Lifetime[17]	ANGLE$_{DRIFT-LIFE}$	B = 300 G, typical maximum drift observed after AEC-Q100 qualification testing	–	±1.0	–	degrees

[1] Typical data is at T_A = 25°C and V_{CC} = 5 V, and it is for design estimates only.

[2] 1 G (gauss) = 0.1 mT (millitesla).

[3] At power-on, a die will not respond to commands until V_{UVLOHI} rises above V_{UVLOHI}. After that, the die will perform and respond normally until V_{CC} drops below $V_{UVLOLOW}$.

[4] Characterization data shows negligible accuracy degradation at supply voltages between 4.35 V and 4.50 V. Significant degradation in accuracy may occur below 4.30 V.

[5] VCC Low Threshold Flag will be sent via the SPI interface as part of the angle measurement.

[6] During the power-on phase, the A1334 SPI transactions are not guaranteed.

[7] Each die includes a linear regulator. The output voltage and current specifications are to aid in PCB design. The pin is not intended to drive any external circuitry.

[8] Parameter is not guaranteed at final test. Values for this characteristic are determined by design.

[9] The A1334 operates in magnetic fields lower than 300 G, but with reduced accuracy and resolution.

[10] Contact Allegro for field optimization. In general, operation with larger magnetic field values result in improved performance (see Figures 3 and 4).

[11] RES$_{ANGLE}$ represents the number of bits of data available for reading from the die registers.

[12] Effective Resolution is calculated using the formula below:

$$log_2(360) - log_2\left(\overline{\sum_{I=1}^{32}\sigma_I}\right)$$

where σ is the Standard Deviation based on thirty measurements taken at each of the 32 angular positions, I = 11.25, 22.5, … 360.

[13] The rate at which a new angle reading will be ready.

[14] To calculate Low RPM mode, time = 25 × 2^{AVG}. Given AVG = 011 = 3 (decimal), so 2^3 = 8.

[15] In general, Allegro's angle sensor ICs are more accurate when stronger magnetic fields (i.e. 900 G) are used. Please contact Allegro for information regarding how users can realize higher accuracy performance from Allegro's angle sensor ICs by using stronger magnetic fields.

[16] Value reflects 3 standard deviations.

[17] After qualification testing, a typical IC drifted less than 0.5 degrees; however, after certain long duration stresses (for example 1000 cycles of -65 to 175 degree C temperature cycling), a small number of devices drifted by approximately 1.5 degrees.

[18] Maximum value based on worst case simulations.

[19] One sigma value at 300 G. Operation with a larger magnetic field results in improved noise performance. For 600 G operation noise reduced by 50% vs 300 G.
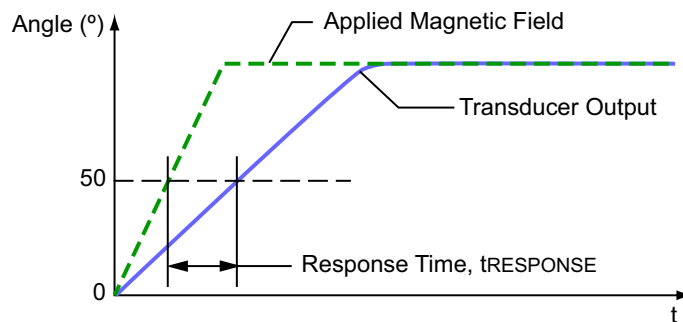
Definition of Response Time

FUNCTIONAL DESCRIPTION

Operational Modes

The A1334 angle sensor device is designed to support a wide variety of automotive applications requiring measuring 0° to 360° angle positions.

An option for two electrically-independent die in the same package provides solid-state consistency and reliability. Each die SPI port can be configured in a different RPM mode. The data output selection is controlled by the address request in the SPI Read command.

The A1334 has dual identical system-on-chip (SoC) architecture. The output of each die is used by the host microcontroller to provide a single channel of target data.

Angle Measurement

The A1334 can monitor the angular position of a rotating magnet at speeds ranging from 0 to more than 7600 rpm. At lower rotational speeds, the A1334 provides high-resolution angle measurement accuracy. It can also support higher rates of rotational speeds at reduced levels of angle measurement accuracy.

The A1334 can be configured to operate in two angular measurement modes of operation: Low RPM mode, and High RPM mode. For applications that have a speed range from 0 to 500 rpm (can vary with AVG), the Low RPM mode provides increased resolution. For applications above 500 rpm, configuring the A1334 in High RPM mode provides angle measurements with standard resolution. Above 7600 rpm, the A1334 continues to provide angle data; however, the accuracy is proportionally reduced.

The actual update rate of Low RPM mode can be changed by setting the AVG bits in the EEPROM. (See the appendix *Programming Reference* for details.) The selection of Low RPM mode or High RPM mode can be programmed, via the Angle_Meas_Mode bit, for the expected maximum rotational speed of the magnet in operation to provide the highest corresponding level of angle accuracy. However, the A1334 provides valid output data regardless of the selected mode and the application speed.

Although the range of the resolution of the measurement data output, RES_{ANGLE}, is determined by the selection of either High RPM or Low RPM mode, the measurement is also affected by the intensity (B, in gauss) of the applied magnetic field from the target. At lower intensities, a reduced signal-to-noise ratio will cause one or two LSBs to change state randomly due to noise,

and the effective DAC resolution is reduced. These factors work together, so when High RPM mode is selected, the effective range of resolution is 8 to 10 bits (from lower to higher field intensities), and in Low RPM mode, the effective range is 11 to 12 bits, depending on field strength and AVG selection.

Regardless of the field intensity and mode selection, the transmission protocol and number formatting remains the same. The MSB is always transmitted first. The entire number should be read.

The Output Angle is always calculated at maximum resolution. To be more explicit:

$$Angle_{OUT} = 360\ (°) \times D[12{:}0]\ /\ (2^{13}) \qquad (1)$$

This formula is always true, regardless of the applied field intensity. What changes with the field and speed setting is how uniform the LSBs of the measurement data (D 12:*x*) will be.

When using the dual die version of the A1334, it should be noted that the secondary die (E2) is rotated 180° relative to the primary die (E1). This results in a difference in measurement of approximately 180° between the two die, given perfect alignment of each die to the target magnet.

This phenomenon can be counteracted by subtracting the offset using a microprocessor. Alternatively, the difference between the two die can be compensated for using the EEPROM for setting the Reference Angle.

System-Level Timing

The A1334 outputs a new angle measurement every t_{ANG} µs. In High RPM mode, the A1334 outputs a new angle measurement every t_{ANG} µs, with an effective resolution of 10 bits. There is, however, a latency of t_{LAT}, from when the rotating magnet is sampled by the CVH to when the sampled data has been completely transmitted over the SPI interface. Because an SPI interface Read command is not synchronous with the CVH timing, but instead is polled by the external host microcontroller, the latency can vary. For single back-to-back SPI transactions (first transaction is sending the Read register 0x0 command, second is retrieving the angle data) the following scenarios are possible:

- Worst case: 2 CVH cycle + 2 SPI cycles

- Best case: 1.5 SPI cycles; 2 µs, assuming a 10 MHz SPI clock

Power-Up

Upon applying power to the A1334, the device automatically runs through an initialization routine. The purpose of this initialization is to ensure that the device comes up in the same predictable operating condition every power cycle. This initialization routine takes a finite amount of time to complete, which is referred to as Power-On Time, t_{PO}.

The A1334 wakes up in a default state that sets all SPI registers to their default value. It is important to note that, regardless of the state of the device before a power cycle, the device will re-power with default values. For example, on every power-up, the device will power up in the mode set in the EEPROM bit RPM. The state of the EEPROM is unchanged.

Diagnostics

The A1334 supports a number of on-chip self-diagnostics to enable the host microcontroller to assess the operational status of each die. For example, the A1334 can detect a low supply voltage and includes an onboard watchdog timer to monitor that internal clocks are running properly.

Table 1: Diagnostic Capabilities

Diagnostic/ Protection	Description	Output State
Reverse VCC	Current Limiting (VCCx pin)	
Output to VCC	Current Limiting (MISOx pin)	
Output to Ground	Current Limiting (MISOx pin)	
Watchdog	Monitors digital logic for proper function	IERR Error flag is set
Missing Magnet	Monitors magnet field level in case of mechanical failure	MAGM Error flag is set
EEPROM Error Detection and Correction	Detection and correction of certain EEPROM memory bit errors	Error flags set in SPI message when errors are detected or corrected
Loss of VCC	Determine if battery power was lost	BATD Error flag is set
Redundancy	Dual die version of the A1334 provides redundant sensors in the same package	

Undervoltage Lockout and VCC Low Flag Diagnostic

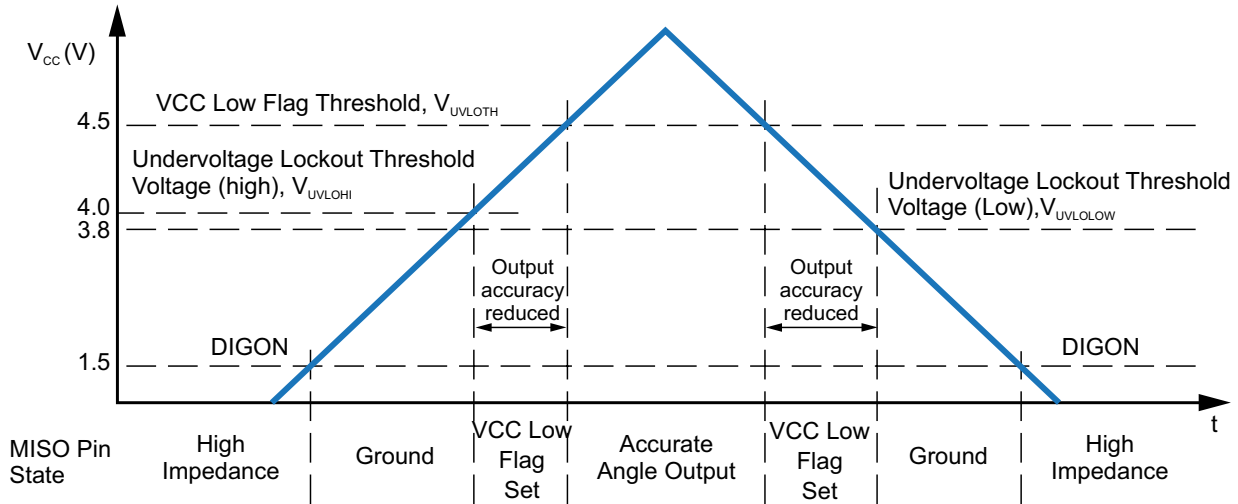The MISO pin state changes according to the state of the VCC ramp, as shown in Figure 1.

Figure 1: Relationship of VCC and MISO Output

APPLICATION INFORMATION

Calculating Target Zero Degree Angle

When shipped from the factory, the default angle value when orientated as shown in Figure 2, is approximately 40º (220º on secondary die). In some cases, the end user may want to program an angle offset in the A1334 to compensate for variation in magnetic assemblies, or for applications where absolute system-level readings are required.

The internal algorithm for computing the output angle is as follows:

$$Angle_{OUT} = Angle_{RAW} - Reference\ Angle \qquad (2)$$

The procedure to zero out the A1334 is quite simple. During final application calibration and programming, position the magnet above the A1334 in the required zero-degree position, and read the angle from the A1334 using the SPI interface ($Angle_{OUT}$). From this angle, the Reference Angle required to program the A1334 can be computed as follows:

$$Reference\ Angle = Angle_{OUT} \qquad (3)$$

Bypass Pin Usage

The Bypass pin is required for proper device operation and is intended to bypass internal IC nodes of the A1334. A 0.1 µF capacitor must be placed in very close proximity to the Bypass pin. It is not intended to be used to source external components. To assist with PCB layout, please see the Operating Characteristics table for output voltage and current requirements.

Changing Sampling Modes

The A1334 features a High RPM sampling mode, and a Low RPM sampling mode. The default power-on state of the A1334 is loaded from EEPROM. To configure the A1334 to Low RPM mode, set the Operating mode to Low RPM mode by writing a logic 1 to bit 2 (RPM) of the configuration commands (CTRL) register, via the SPI interface.

Target alignment for default angle setting
• Target rotation axis intersects primary die
  • Primary die 40° default point
  • Secondary die 220° default point
(Example shows element E1 as primary die element E2 as secondary die)

Target poles aligned with A1334 elements

Target rotation axis
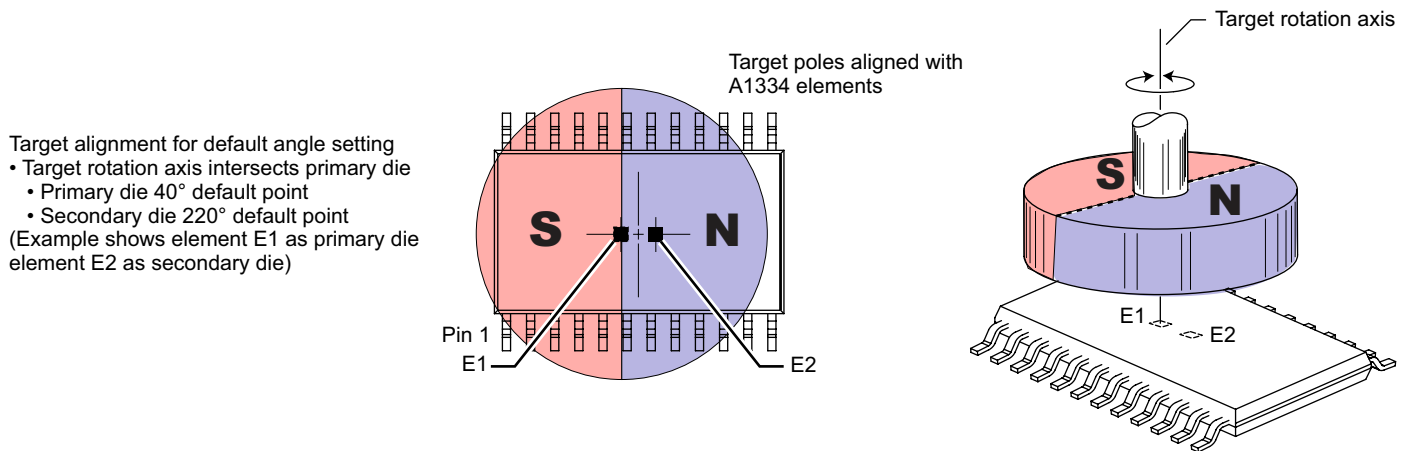
Figure 2: Orientation of Magnet Relative to Primary Die and Secondary Die
(dual die version used as example)

Magnetic Target Requirements

The A1334 is designed to operate with magnets constructed with a variety of magnetic materials, cylindrical geometries, and field strengths, as shown in Table 2. To reach this end, Allegro offers three different "Field Optimization" or trim levels; 300 G, 550 G and 900 G. Figure 8 demonstrates the typical 25ºC performance for these three trim levels over field strength. In general, higher field strengths result in improved performance in terms of angle error and angle noise (see Figures 3 and 4) To obtain maximum performance, it is important to match the operating field with the field trim level. Contact Allegro for more detailed information on magnet selection and performance.

Redundant Applications and Alignment Error

The A1334 dual die version is designed to be used in redundant applications with a single magnet spinning over the two separate dies that are mounted side-by-side in the same package. One challenge with this configuration is correctly lining up the magnet with the device package, so it is important to be aware of the physical separation of the two dies. Figure 5 depicts two possible alignment configurations.
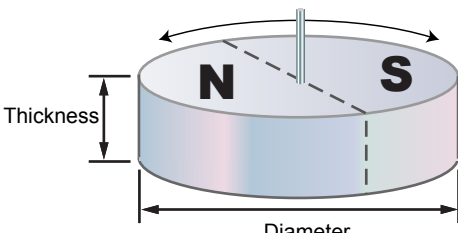
Figure 6 illustrates the behavior of alignment error when using an 8 mm diameter magnet positioned above the branded face of the package. The curve shows the relationship between absolute angle error present on the output of the die versus eccentricity of the die relative to the rotation axis of the magnet. The curve is the same for both dies in the package.

The curve provides guidance to determine what the optimal magnet placement should be for a given application. For example, given that the maximum spacing between the two dies is 1 mm, if the center of the magnet rotation is placed at the midpoint between the two dies, each die will have a maximum eccentricity of 0.5 mm.

For applications with reduced accuracy requirements, considering one die the primary and the other die the secondary, the magnet axis of rotation could be positioned directly above the primary die, and thus offset 1 mm from the secondary die, yielding zero alignment error on the primary die, and approximately ±1° of absolute error on the secondary die due to geometric mismatch.

Table 2: Typical Target Magnet Parameters

Diameter (mm)	Thickness (mm)
15	4
10	2.5
8	2.5
6	2.5

*A magnet with 8 mm (or greater) diameter and 2.5 mm thickness is the recommended magnet for redundant applications.
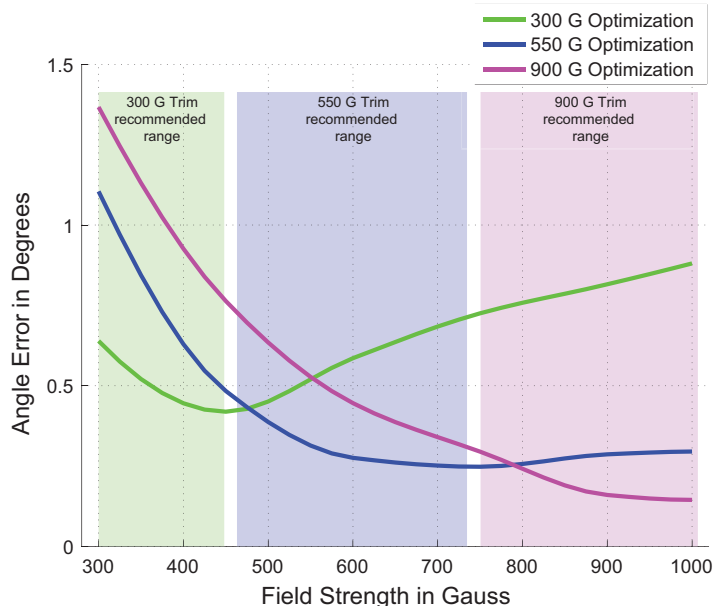

Figure 3: Maximum Peak Angle Error Over Field Strength
Different Factory Optimizations

System Timing and Error

The A1334 is a digital system, and therefore takes angle samples at a fixed sampling rate. When using a sensing device with a fixed sampling rate to sample a continuously moving target, there will be error introduced that can be simply calculated with the sampling rate of the device and the speed at which the magnetic signal is changing. In the case of the A1334, the input signal is rotating at various speeds, and the sampling rate of the A1334 is fixed at ANG. The calculation would be:

$$ANG\ (\mu s) \times angular\ velocity\ (°/\mu s)\ . \qquad (4)$$

So the faster the magnetic object is spinning, the further behind in angle the output signal will seem for a fixed sampling rate.
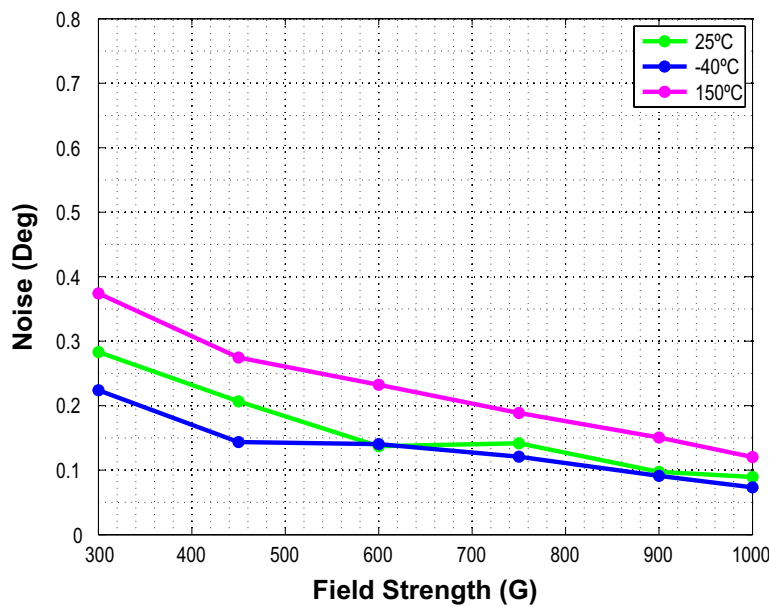
Figure 4: One Sigma Noise over Field Strength
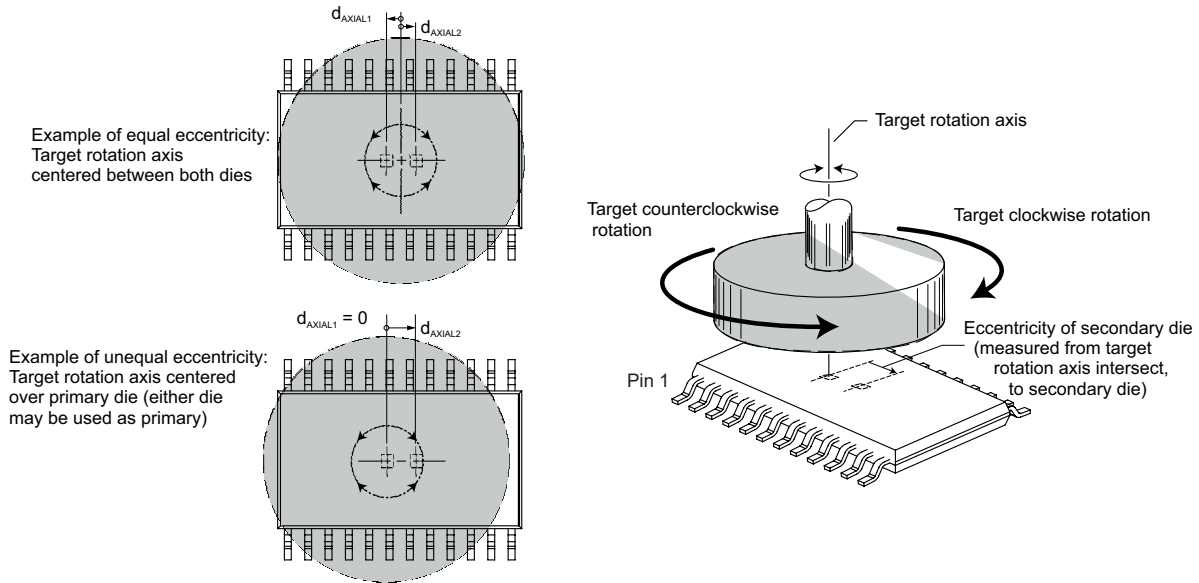
Figure 5: Demonstration of Magnet to Sensing Element Eccentricity
(dual die version used as example)
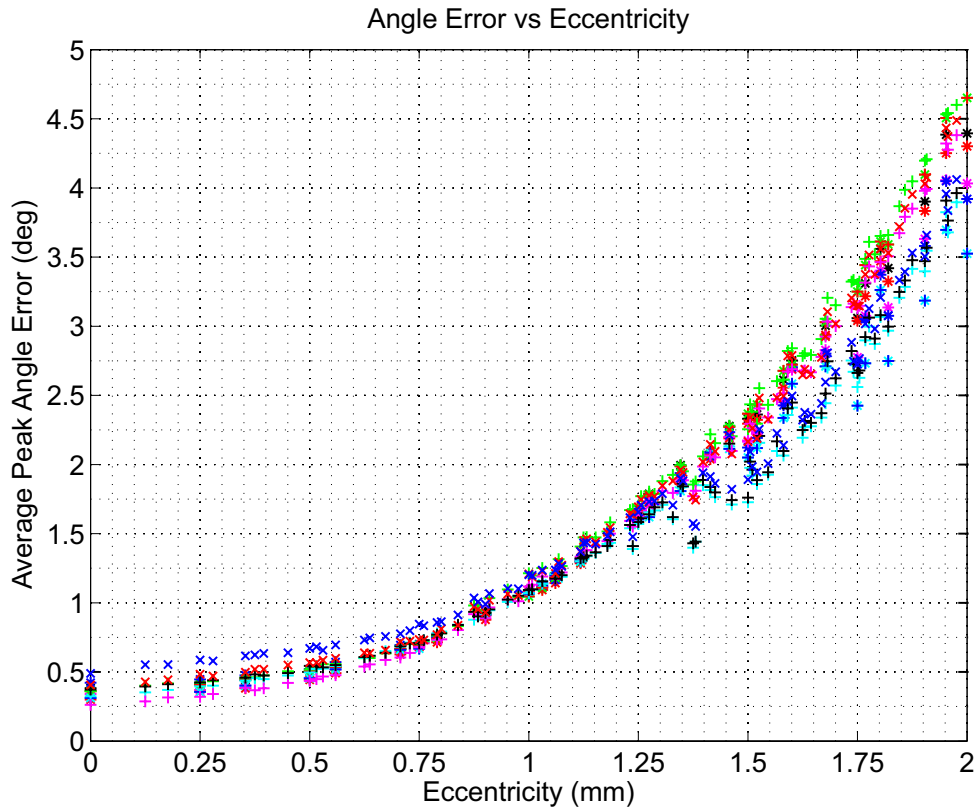
Figure 6: Characteristic Performance Based on 14 Pieces
(900 G Field Strength, 8 mm Diameter Magnet)

TYPICAL CHARACTERISTICS
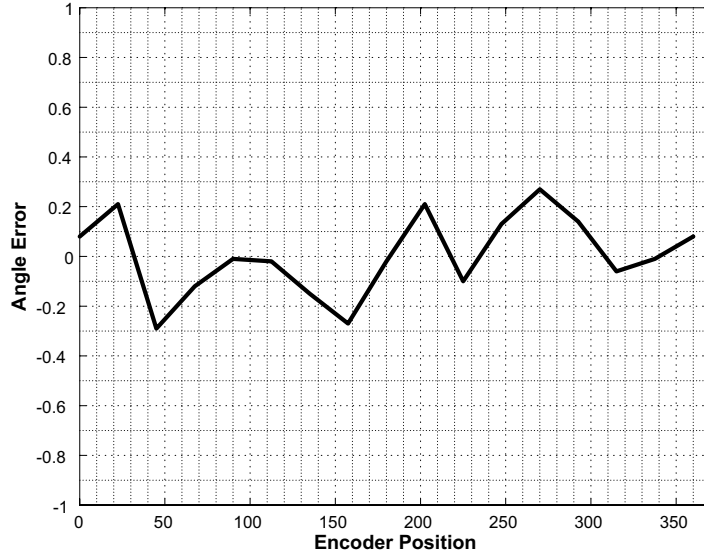
Figure 7: Typical Angle Error versus Absolute Position
(300 G, 25ºC)
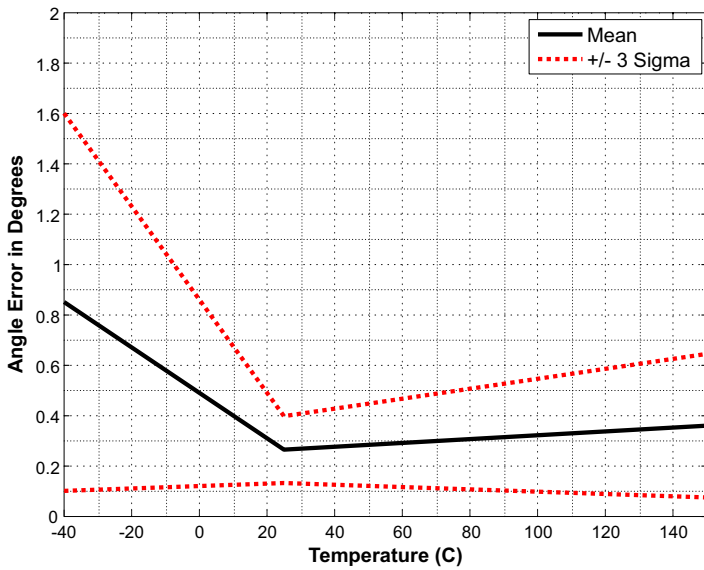
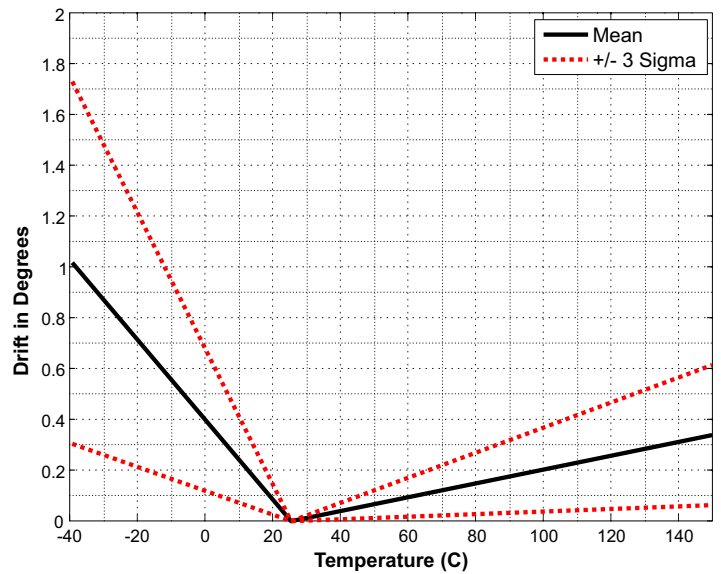Figure 8: Angle Error Over Temperature (300 G)
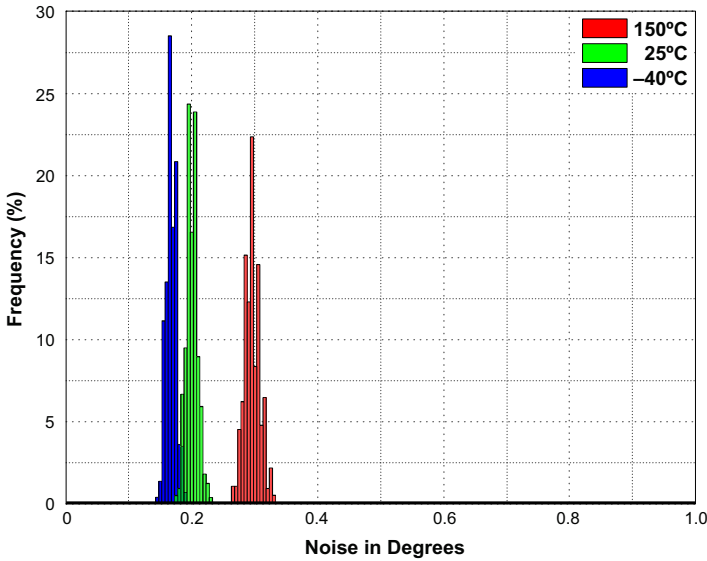

Figure 9: Temperature Drift (300 G)

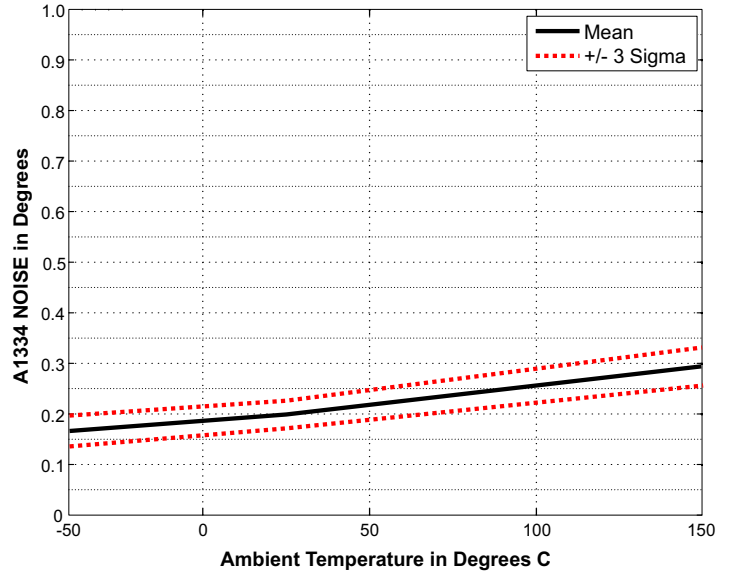**Figure 10: Noise Distribution Over Temperature (1σ, 300 G)**

Figure 11: Noise Performance Over Temperature (1σ, 300 G)
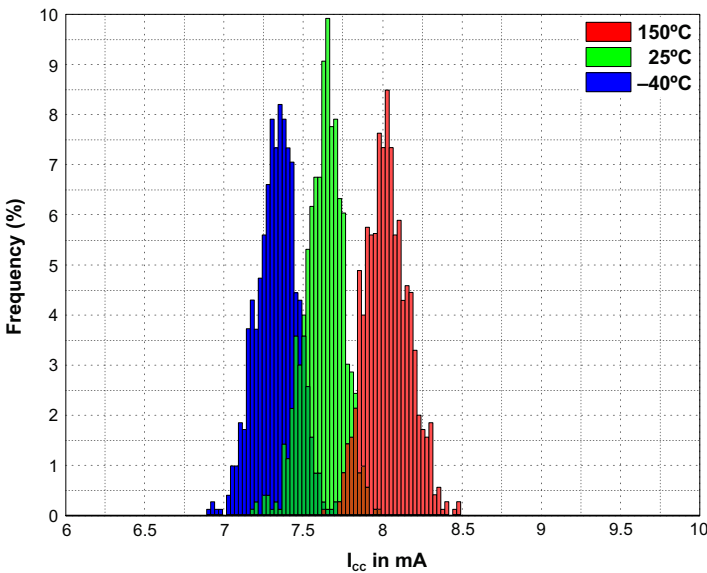
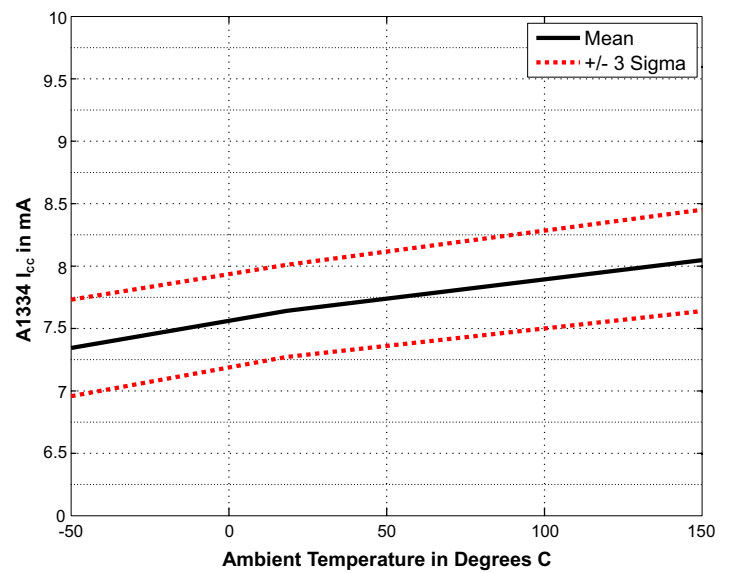**Figure 12: I_{CC} Distribution Over Temperature (V_{CC} = 4.5 V)**

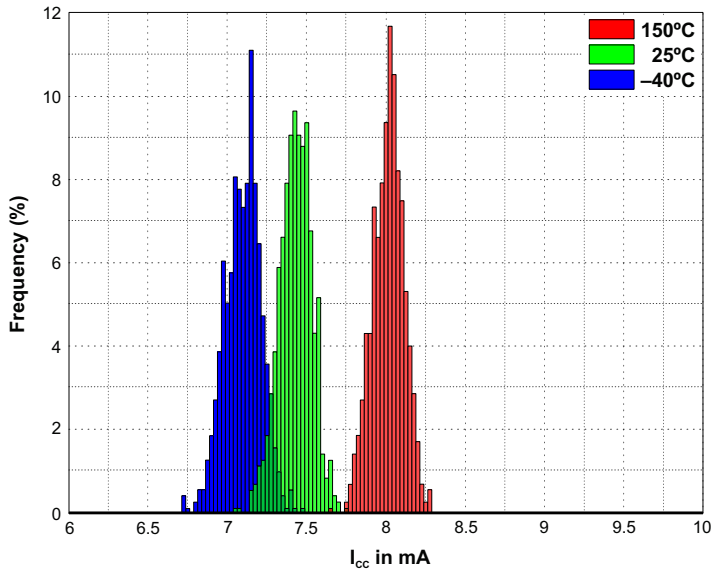**Figure 13: I_{CC} Over Temperature (V_{CC} = 4.5 V)**

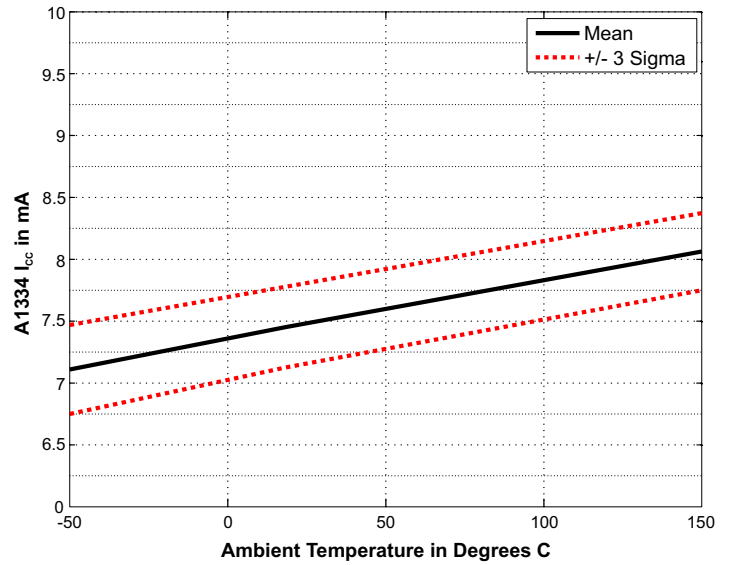**Figure 14: I_CC Distribution Over Temperature (V_CC = 14.5 V)**

Figure 15: I_CC Over Temperature (V_CC = 14.5 V)

EMC Reduction

For applications with stringent EMC requirements, a 100 Ω resistance should be added to the supply for the device in order to suppress noise. A recommended circuit is shown in Figure 16.
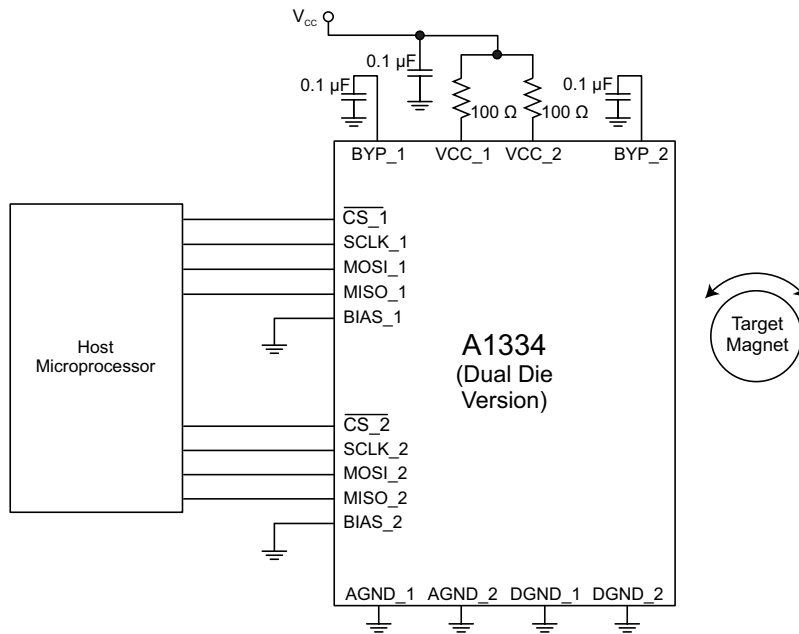

Figure 16: Typical Application Diagram (dual die version) with EMC Suppression Resistor, R$_{SPLY}$, on Supply Line
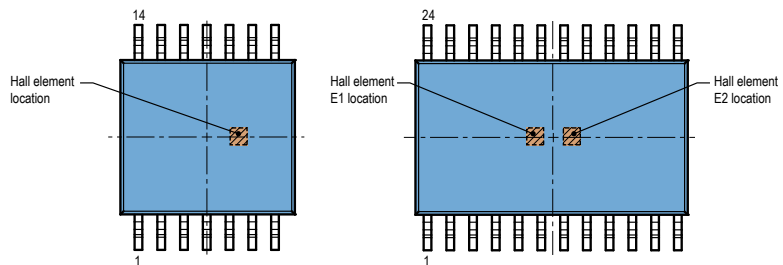

Figure 17: Hall Element Located Off-Center within the Device Body
Refer to the Package Outline Drawing for reference dimensions.

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference MO-153 AB-1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
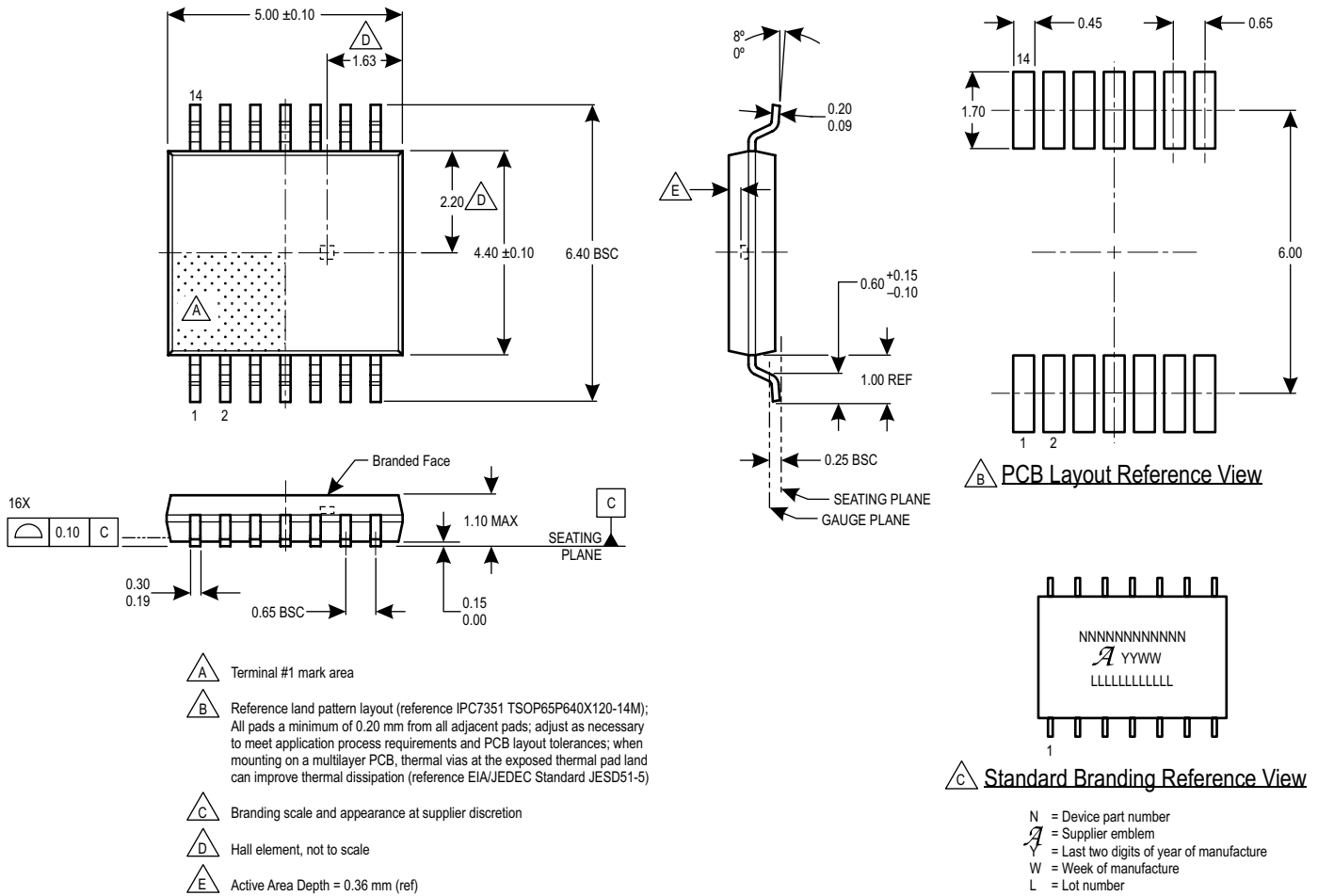Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 TSOP65P640X120-14M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to
meet application process requirements and PCB layout tolerances; when
mounting on a multilayer PCB, thermal vias at the exposed thermal pad land
can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

E Active Area Depth = 0.36 mm (ref)

B PCB Layout Reference View

C Standard Branding Reference View

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

Figure 18: Package LE, 14-Pin TSSOP (Single Die Version)

For Reference Only – Not for Tooling Use
(Reference MO-153 AD)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
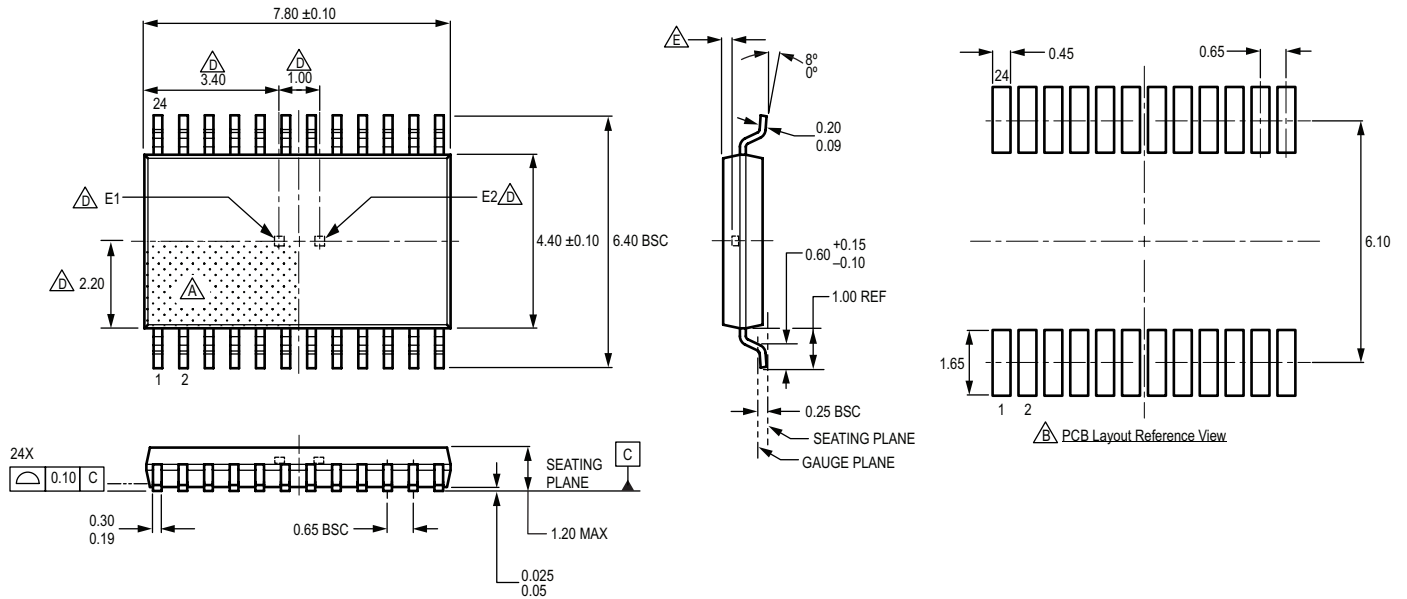Exact case and lead configuration at supplier discretion within limits shown

7.80 ±0.10

D 3.40

D 1.00

24

E1

E2 D

D 2.20

A

1 2

4.40 ±0.10

6.40 BSC

E

8°
0°

0.20
0.09

0.60 +0.15 −0.10

1.00 REF

0.25 BSC

SEATING PLANE

GAUGE PLANE

24

0.45

0.65

6.10

1.65

1 2

B PCB Layout Reference View

24X

0.10 C

0.30
0.19

0.65 BSC

SEATING PLANE

C

1.20 MAX

0.025
0.05

NNNNNNNNNN
𝒜 YYWW
LLLLLLLLLL

1

C Standard Branding Reference View

N = Device part number
𝒜 = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M);
all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary
to meet application process requirements and PCB layout tolerances; when
mounting on a multilayer PCB, thermal vias can improve thermal dissipation
(reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Hall elements (E1, E2), corresponding to respective die; not to scale
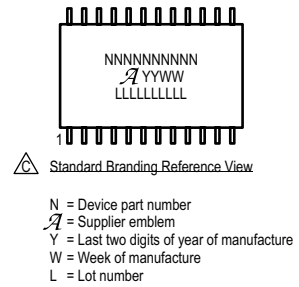
E Active Area Depth 0.36 mm REF

Figure 19: Package LE, 24-Pin TSSOP (Dual Die Version)

Revision History

Revision	Date	Description
–	October 23, 2014	Initial Release
1	December 16, 2014	Revised EC table and Selection Guide to support dual die release; added Typical Chracteristics graphs
2	February 17, 2015	Revised Title and Terminal List Table, added footnotes to EC table
3	June 2, 2015	Updated Selection Guide, revised EC table, Magnetic Target Requirements section, Figure 3, and added new Figure 4
4	July 27, 2015	Updated Figure 3 on page 10
5	April 15, 2016	Corrected LE-24 Package Outline Drawing dimensions and added AEC-Q100 qualification to Features and Benefits
6	December 5, 2016	Updated product status to "Not for New Design"
7	July 2, 2018	Updated product status to "Last-Time Buy"
8	October 9, 2018	Added footnote 8 to Angle Refresh Rate and Response Time characteristics (page 4)
9	November 2, 2018	Corrected Temperature Drift typo (page 5)
10	January 25, 2019	Updated product status to "Discontinued"

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