Product Change Notification - SYST-15FWBL230

Date:

16 Jul 2019

Product Category:

Ethernet Switches

Affected CPNs:

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Notification subject:

Data Sheet - KSZ8567S 7-Port 10/100 Ethernet AVB Switch with SGMII and RGMII/MII/RMII Interface Data Sheet Document Revision

Notification text:

SYST-15FWBL230

Microchip has released a new DeviceDoc for the KSZ8567S 7-Port 10/100 Ethernet AVB Switch with SGMII and RGMII/MII/RMII Interfa of devices. If you are using one of these devices please read the document located at KSZ8567S 7-Port 10/100 Ethernet AVB Switch with SGMII and RGMII/MII/RMII Interfa.

Notification Status: Final

Description of Change:

1) Table 4-15, Transmit Tail Tag Format (from Host to Switch): Bit 7 changed to 15:00, description changed to Reserved.

2) Section 4.5, IEEE 1588 Precision Time Protocol: All PHY ports must be operating at 100 Mbps - or 1 Gbps removed.

3) Section 5.5.1, SGMII Control Register: Bit 12, Auto-Negotiation Enable - Applies to the SGMII Mode Port only

4) Section 2.1, General Description, on page 8: Updated first bullet to indicate the non-blocking wire-speed Ethernet switch fabric supports 1 Gbps on RGMII.

5) Table 3-1, Table 3-2, Table 3-3: Updated INTRP_N and SYNCLKO pin listings to indicate configuration strap functions.

6) Section 4.3.3, Back-Off Algorithm, on page 26: Updated second sentence.

7) Section 4.3.5, Legal Packet Size, on page 26: Simplified paragraph for clarity.

8) Section 4.3.6, Flow Control, on page 26: Simplified last sentence of third paragraph.

9) Table 4-11, Hashed(SA)+FID Lookup in VLAN Mode: Updated Action description for the Yes entry.

10) Section 4.4.3.2.1, Tag Insertion and Removal, on page 34: Updated last paragraph of section.

11) Section 4.4.8, Multiple Spanning Tree Support, on page 38: Updated second sentence.

12) Table 4-18, ACL Matching Rule Parameters for MD = 01: Corrected ENB[1:0] 01 and 10 definitions to match those in Table 4-17, Matching Rule Options.

13) Section 4.5, IEEE 1588 Precision Time Protocol, on page 50: Added additional paragraph to end of section.

14) Section 4.12, In-Band Management, on page 62:

a) Added to last sentence of first paragraph.

b) Added additional sentence to end of second paragraph.

c) Added additional sentence to end of sixth paragraph.

15) Section 5.1.6.17, Timestamp Control and Status Register, on page 123: Updated bit 6 definition.

16) Section 5.2.1.7, Port Operation Control 0 Register, on page 141: Updated bit 6 and 7 descriptions to include references to the MAC and additional clarification.

17) Section 5.2.2.12, PHY Remote Loopback Register, on page 151: Simplified bit 8 description.

18) Section 5.2.3, Port N: Port SGMII Control Registers (0xN200 - 0xN2FF), on page 154: Added new note to end of section.

19) Section 5.2.5.1, Port MAC Control 0 Register, on page 157: Bit 0 made reserved.

20) Section 6.4.8, Power-up and Reset Timing:

a) Updated Note 1.

b) Updated Figure 6-13 to include SGMII power supplies (VDDHS, VDDLS).

21) Table 6-12 Added new trw entry to table.

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 16 July 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A
Attachment(s):
KSZ8567S 7-Port 10/100 Ethernet AVB Switch with SGMII and RGMII/MII/RMII Interfa

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Affected Catalog Part Numbers (CPN)

KSZ8567STXI
KSZ8567STXI-TR
KSZ8567STXV-TRVAO
KSZ8567STXV-VAO