Product / Process Change Notification

N° 2020-057-A

Dear Customer,

Please find attached our INFINEON Technologies PCN:

DC offset level reduction of MERUS™ products and Introduction of MERUS™ trademark

Important information for your attention:

- Please respond to this PCN by indicating your decision on the approval form, sign it and return to your sales partner before **12th August 2020**.
- Infineon aligns with the widely-recognized JEDEC STANDARD **"JESD46",** which stipulates: **"Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change."**

Your prompt reply will help Infineon Technologies to assure a smooth and well executed transition. If Infineon does not hear from your side by the due date, we will assume your full acceptance to this proposed change and its implementation.

Your attention and response to this matter is greatly appreciated.

Infineon Technologies AG
Postal Address Headquarters: Am Campeon 1-15, D-85579 Neubiberg, Phone +49 (0)89 234-0
Chairman of the Supervisory Board: Dr. Wolfgang Eder
Management Board: Dr. Reinhard Ploss (CEO), Dr. Helmut Gassel, Jochen Hanebeck, Dr. Sven Schneider
Registered Office: Neubiberg
Commercial Register: München HRB 126492

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▶ Products affected:

Please refer to attached affected product list 1_cip20057_a

▶ Detailed Change Information:

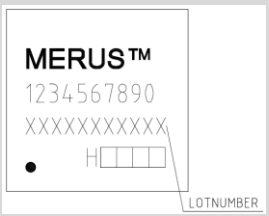
Subject:

- Reduction of DC offset for digital input parts
- Introduction of MERUS™ trademark

Reason:

- Main reason for this revision update is to reduce the DC offset for digital input parts (MA12040P and MA12070P) in order to elimate click/pop noise during start-up. Other limitations and known issues have been resolved with this update as well.
- Integration of MERUS products into Infineon Technologies AG

Description (applies to):

	Old	New
DC offset MA12040P, MA12070P	■ High output voltage offset leading to potential audible click/pop noise during start-up. - BTL/PBTL = +/-200mV - SE = not specified	■ DC offset is trimmed in production giving inaudible click/pop nosie during start-up. - BTL/PBTL = +/-35mV - SE = +/-90mV Note that is only valid for the follwoing output configurations: BTL, PBTL, BTL+2xSE (2.1), i.e. not for 4xSE output configuration (OUT0A and OUT0B not trimmed).
Thermal fold-back MA12040P, MA12070P	■ Active on default potentially causing unwanted limiter behaviour	■ Functionality has been turned off on default
Limiter active flag MA12040P, MA12070P	■ flag errounously set with low volume settings	■ not set with low volume settings
Output polarity MA12040P, MA12070P	■ reversed for BTL and PBTL output configurations.	■ Datasheet now reflects the correct polarity sign for BTL and PBTL output configuration
/CLIP pin MA12040P, MA12070P, MA12040, MA12070	■ always active for PBTL output configuration.	■ now only active when clipping occurs for all output configurations.
Marking on device	■ eximo® 	■ MERUS™  rotating the top marking by 90°C without changing the pin1 location

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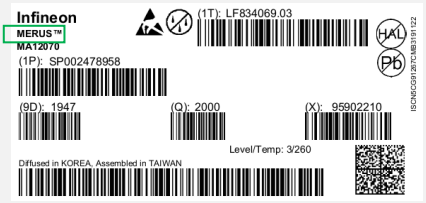
▶ Product Identification:

External traceability via marking on device and Trademark on the label



Internal traceability via Baunumber, Lotnumber, date code

▶ Impact of Change:

NO change in quality and reliability verified within product qualification

NO changes in bill of material

NO change in fit, form and function

▶ Attachments:

Affected product list 1_cip20057_a

▶ Time Schedule:

■ Final qualification report:	on request
■ First samples available:	30-July-2020
■ Intended start of delivery:	30-September-2020 or earlier pending on customer approval

If you have any questions, please do not hesitate to contact your local Sales office.

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Sales name	SP number	OPN	Package
MA12040	SP002478940	MA12040XUMA1	PG-VQFN-64
MA12040P	SP002478950	MA12040PXUMA1	PG-VQFN-64
MA12070	SP002478958	MA12070XUMA1	PG-VQFN-64
MA12070P	SP002478966	MA12070PXUMA1	PG-VQFN-64