CHANGE NOTIFICATION

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900

September 16, 2014

Dear Sir/Madam: PCN# 091614

Subject: Notification of Change to LTC2486, LTC2487, LTC2488, LTC2489, LTC2492, LTC2493, LTC2494, LTC2495, LTC2496, LTC2497, LTC2498, LTC2499 Datasheet

Please be advised that Linear Technology Corporation has made a change to the datasheet specifications of subject devices in order to improve device manufacturability. The changes are mentioned below.

For all devices:
The Maximum External Oscillator Frequency (f_{EOSC}) in the Timing Characteristics is being reduced from 4000kHz to 1000kHz. In addition, the Input Voltage Range has been clarified as shown in the attached datasheet pages. There are many applications that are using the part at 4MHz and the performance is perfectly adequate. But at 4MHz, performance is significantly reduced from the limits guaranteed in the specification table, as shown in the graphs at the end of the datasheet.
This change is intended to apply to future customer designs. No changes are being made to the circuit or the test methodology, so customers that are using these devices with F0 frequencies between 1000kHz and 4000kHz and are satisfied with the performance will continue to receive the same product.

For LTC2492, LTC2493, LTC2498, LTC2499:
Summary of Output Data Format Table has been clarified as shown in the attached datasheet pages.

For LTC2486, LTC2487, LTC2494, LTC2495:
An error in the Converter Configuration Table (Table 4) was corrected to display the external input gain in autocalibration mode as 256 (incorrectly shown as 264).

No changes are being made to all devices or test program, this is just a change to the datasheet. New customer designs after November 16, 2014 must adhere to the new datasheet limit.

Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2077, or by email at JASON.HU@LINEAR.COM. If I do not hear from you by November 16, 2014, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10		1000 ~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		50	µs
t_{LEO}	External Oscillator Low Period		●	0.125		50	µs
t_{CONV_1}	Conversion Time for 1x Speed Mode	50Hz Mode 60Hz Mode Simultaneous 50/60Hz Mode External Oscillator	● ● ●	157.2 131 144.1	160.3 133.6 146.9 41036/f_{EOSC} (in kHz)	163.5 136.3 149.9	ms ms ms ms
t_{CONV_2}	Conversion Time for 2x Speed Mode	50Hz Mode 60Hz Mode Simultaneous 50/60Hz Mode External Oscillator	● ● ●	78.7 65.6 72.2	80.3 66.9 73.6 20556/f_{EOSC} (in kHz)	81.9 68.2 75.1	ms ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Notes 10, 17) External Oscillator (Notes 10, 11, 15)			38.4 f_{EOSC}/8		kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Notes 10, 17)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Notes 10, 11, 15)	●			4000	kHz
t_{LESCK}	External SCK Low Period	(Notes 10, 11, 15)	●	125			ns
t_{HESCK}	External SCK High Period	(Notes 10, 11, 15)	●	125			ns
t_{DOUT_ISCK}	Internal SCK 24-Bit Data Output Time	Internal Oscillator (Notes 10, 17) External Oscillator (Notes 10, 11, 15)	●	0.61	0.625 192/f_{EOSC} (in kHz)	0.64	ms ms
t_{DOUT_ESCK}	External SCK 24-Bit Data Output Time	(Notes 10, 11, 15)			24/f_{ESCK} (in kHz)		ms
t_1	$\overline{CS}$↓ to SDO Low		●	0		200	ns
t_2	$\overline{CS}$↑ to SDO High Z		●	0		200	ns
t_3	$\overline{CS}$↓ to SCK↓	Internal SCK Mode	●	0		200	ns
t_4	$\overline{CS}$↓ to SCK↑	External SCK Mode	●	50			ns
t_{KQMAX}	SCK↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$↓		●	50			ns
t_7	SDI Setup Before SCK↑	(Note 5)	●	100			ns
t_8	SDI Hold After SCK↑	(Note 5)	●	100			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: Unless otherwise specified:

V_{CC} = 2.7V to 5.5V

$V_{REFCM} = V_{REF}/2$, $F_S = 0.5V_{REF}$/Gain

$V_{IN} = IN^+ - IN^-$, $V_{IN(CM)} = (IN^+ - IN^-)/2$,

where IN^+ and IN^- are the selected input channels.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless other wise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The SCK can be configured in external SCK mode or internal SCK mode. In external SCK mode, the SCK pin is used as a digital input and the driving clock is f_{ESCK}. In the internal SCK mode, the SCK pin is used as a digital output and the output clock signal during the data output is f_{ISCK}.

Note 11: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses its internal oscillator.

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: Guaranteed by design and test correlation.

Note 15: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

Note 16: Refer to Applications Information section for performance vs data rate graphs.

Note 17: The converter in internal SCK mode of operation such that the SCK pin is used as a digital output.

Note 18: For V_{CC} < 3V, V_{IH} is 2.5V for pin f_O.

The LTC2486 input measurement range -0.5*VREF to +0.5*VREF in both differential and single-ended configurations as shown in Figure 38. Highest linearity is achieved with Fully Differential drive and a constant common-mode voltage (Figure 38b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

APPLICATIONS INFORMATION

Easy Drive Input Current Cancellation

The LTC2486 combines a high precision, delta-sigma ADC with an automatic, differential, input current cancellation front end. A proprietary front end passive sampling network transparently removes the differential input current. This enables external RC networks and high impedance sensors to directly interface to the LTC2486 without external amplifiers. The remaining common mode input current is eliminated by either balancing the differential input impedances or setting the common mode input equal to the common mode reference (see Automatic Differential Input Current Cancellation section). This unique architecture does not require on-chip buffers, thereby enabling signals to swing beyond ground and V_{CC}. Moreover, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2486 automatically enters an internal reset state when the power supply voltage, V_{CC}, drops below approximately 2V. This feature guarantees the integrity of the conversion result, input channel selection, and serial clock mode.

When V_{CC} rises above this threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channel IN^+ = CH0 and IN^- = CH1 with simultaneous 50Hz/60Hz rejection, 1x output rate, and gain = 1. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel, rejection mode, speed mode, temperature selection or gain can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for the REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$).

The LTC2486 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front end circuits, and as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a decreased reference will improve the converter's overall INL performance.

Input Voltage Range

The analog inputs are truly differential with an absolute, common mode range for the CH0 to CH3 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2486 converts the bipolar differential input signal $V_{IN} = IN^+ - IN^-$ (where IN^+ and IN^- are the selected input channels), from –FS = $-0.5 \cdot V_{REF}$/Gain to +FS = $0.5 \cdot V_{REF}$/Gain where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes (see Table 1).

Signals applied to the input (CH0 to CH3, COM) may extend 300mV below ground and above V_{CC}. In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

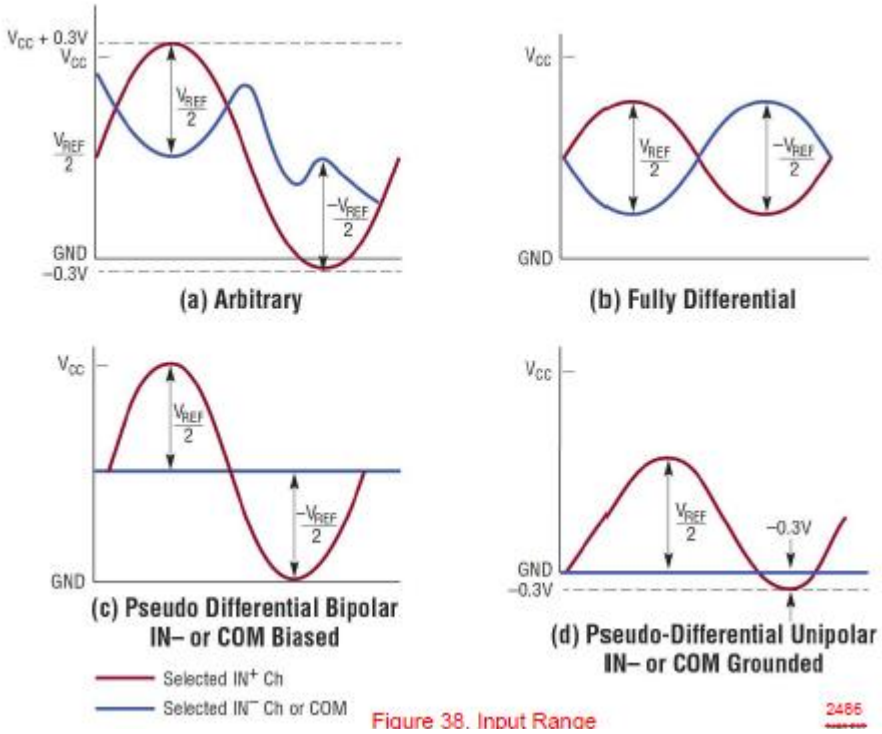

Figure 38. Input Range

APPLICATIONS INFORMATION

Table 4. Converter Configuration

1	0	EN	SGL	ODD	A2	A1	A0	EN2	IM	FA	FB	SPD	GS2	GS1	GS0	CONVERTER CONFIGURATION
1	0	0	Any Input Channel					X	X	X	X	X	X	X	X	Keep Previous
1	0	1						0	X	X	X	X	X	X	X	Keep Previous
1	0	1						1	0	Any Rejection Mode		0	0	0	0	External Input, Gain = 1, Autocalibration
1	0	1						1	0			0	0	0	1	External Input, Gain = 4, Autocalibration
1	0	1						1	0			0	0	1	0	External Input, Gain = 8, Autocalibration
1	0	1						1	0			0	0	1	1	External Input, Gain = 16, Autocalibration
1	0	1						1	0			0	1	0	0	External Input, Gain = 32, Autocalibration
1	0	1						1	0			0	1	0	1	External Input, Gain = 64, Autocalibration
1	0	1						1	0			0	1	1	0	External Input, Gain = 128, Autocalibration
1	0	1						1	0			0	1	1	1	External Input, Gain = ~~264~~, Autocalibration
1	0	1						1	0			1	0	0	0	External Input, Gain = 1, 2x Speed
1	0	1						1	0			1	0	0	1	External Input, Gain = 2, 2x Speed
1	0	1						1	0			1	0	1	0	External Input, Gain = 4, 2x Speed
1	0	1						1	0			1	0	1	1	External Input, Gain = 8, 2x Speed
1	0	1						1	0			1	1	0	0	External Input, Gain = 16, 2x Speed
1	0	1						1	0			1	1	0	1	External Input, Gain = 32, 2x Speed
1	0	1						1	0			1	1	1	0	External Input, Gain = 64, 2x Speed
1	0	1						1	0			1	1	1	1	External Input, Gain = 128, 2x Speed
1	0	1						1	0	0	0	Any Speed	Any Gain			External Input, Simultaneous 50Hz/60Hz Rejection
1	0	1						1	0	0	1					External Input, 50Hz Rejection
1	0	1						1	0	1	0					External Input, 60Hz Rejection
1	0	1						1	0	1	1					Reserved, Do Not Use
1	0	1						1	1	0	0	X	X	X	X	Temperature Input, Simultaneous 50Hz/60Hz Rejection
1	0	1						1	1	0	1	X	X	X	X	Temperature Input, 50Hz Rejection
1	0	1						1	1	1	0	X	X	X	X	Temperature Input, 60Hz Rejection
1	0	1						1	1	1	1	X	X	X	X	Reserved, Do Not Use

256

Rejection Mode (FA, FB)

The LTC2486 includes a high accuracy on-chip oscillator with no required external components. Coupled with an integrated 4th order digital low pass filter, the LTC2486 rejects line frequency noise. In the default mode, the LTC2486 simultaneously rejects 50Hz and 60Hz by at least 87dB. If more rejection is required, the LTC2486 can be configured to reject 50Hz or 60Hz to better than 110dB.

Speed Mode (SPD)

Every conversion cycle, two conversions are combined to remove the offset (default mode). This result is free from offset and drift. In applications where the offset is not critical, the auto-calibration feature can be disabled with the benefit of twice the output rate. While operating in the 2x mode (SPD = 1), the linearity and full-scale errors are unchanged from the 1x mode performance. In both the 1x and 2x mode there is no latency. This enables input steps or multiplexer changes to settle in a single conversion cycle, easing system overhead and increasing the effective conversion rate. During temperature measurements, the 1x mode is always used independent of the value of SPD.

GAIN (GS2, GS1, GS0)

The input referred gain of the LTC2486 is adjustable from 1 to 256 (see Tables 5a and 5b). With a gain of 1, the differential input range is $\pm V_{REF}/2$ and the common mode input range is rail-to-rail. As the gain is increased, the differential input range is reduced to $\pm 0.5 \bullet V_{REF}/Gain$ but the common mode input range remains rail-to-rail. As the differential gain is increased, low level voltages are digitized with greater resolution. At a gain of 256, the LTC2486 digitizes an input signal range of ±9.76mV (V_{REF} = 5V) with over 16,000 counts.

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current	Conversion Current (Note 11)	●		160	275	µA
		Temperature Measurement (Note 11)	●		200	300	µA
		Sleep Mode (Note 11)	●		1	2	µA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10		1000 ~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		50	µs
t_{LEO}	External Oscillator Low Period		●	0.125		50	µs
t_{CONV_1}	Conversion Time for 1x Speed Mode	50Hz Mode	●	157.2	160.3	163.5	ms
		60Hz Mode	●	131	133.6	136.3	ms
		Simultaneous 50Hz/60Hz Mode	●	144.1	146.9	149.9	ms
		External Oscillator (Note 10)			41036/f_{EOSC} (in kHz)		ms
t_{CONV_2}	Conversion Time for 2x Speed Mode	50Hz Mode	●	78.7	80.3	81.9	ms
		60Hz Mode	●	65.6	66.9	68.2	ms
		Simultaneous 50Hz/60Hz Mode	●	72.2	73.6	75.1	ms
		External Oscillator (Note 10)			20556/f_{EOSC} (in kHz)		ms

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3, 15)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(STA)}$	Hold Time (Repeated) Start Condition		●	0.6			µs
t_{LOW}	Low Period of the SCL Pin		●	1.3			µs
t_{HIGH}	High Period of the SCL Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated Start Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for SDA Signals	(Note 14)	●	20 + 0.1C_B		300	ns
t_f	Fall Time for SDA Signals	(Note 14)	●	20 + 0.1C_B		300	ns
$t_{SU(STO)}$	Set-Up Time for Stop Condition		●	0.6			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: Unless otherwise specified: V_{CC} = 2.7V to 5.5V

$V_{REFCM} = V_{REF}/2$, $F_S = 0.5V_{REF}$/Gain

$V_{IN} = IN^+ - IN^-$, $V_{IN(CM)} = (IN^+ - IN^-)/2$,
where IN^+ and IN^- are the selected input channels.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 11: The converter uses its internal oscillator.

Note 12: The output noise includes the contribution of the internal calibration operations.

Note 13: Guaranteed by design and test correlation.

Note 14: C_B = capacitance of one bus line in pF (10pF ≤ C_B ≤ 400pF).

Note 15: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 16: Refer to Applications Information section for Performance vs Data Rate graphs.

APPLICATIONS INFORMATION

amplifiers. The remaining common mode input current is eliminated by either balancing the differential input impedances or setting the common mode input equal to the common mode reference (see the Automatic Differential Input Current Cancellation section). This unique architecture does not require on-chip buffers, thereby enabling signals to swing beyond ground and V_{CC}. Moreover, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2487 automatically enters an internal reset state when the power supply voltage, V_{CC}, drops below a threshold of approximately 2.0V. This feature guarantees the integrity of the conversion result and input channel selection.

When V_{CC} rises above this threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channels IN^+ = CH0 and IN^- = CH1 with simultaneous 50Hz/60Hz rejection, 1x output rate, and gain = 1. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel, rejection mode, speed mode, temperature selection or gain can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for the REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$).

The LTC2487 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front end circuits and, as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a decreased reference will improve the converter's overall INL performance.

Input Voltage Range

The analog inputs are truly differential with an absolute, common mode range for the CH0-CH3 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2487 converts the bipolar differential input signal $V_{IN} = IN^+ - IN^-$ (where IN^+ and IN^- are the selected input channels), from $-FS = -0.5 \cdot V_{REF}/Gain$ to $+FS = 0.5 \cdot V_{REF}/Gain$ where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes (see Table 1).

In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

The LTC2487 input measurement range is -0.5*VREF to +0.5*VREF in both differential and single-ended configurations as shown in Figure 37. Highest linearity achieved with Fully Differential drive and a constant common-mode voltage (Figure 37b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

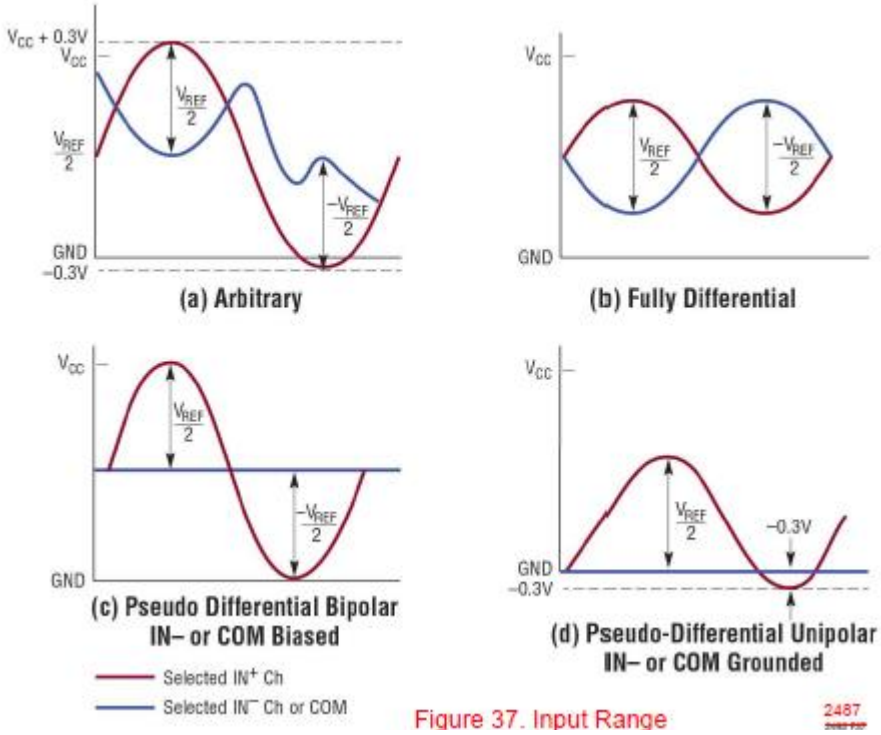

Figure 37. Input Range

2487

APPLICATIONS INFORMATION

The first input bit (SGL) following the 101 sequence determines if the input selection is differential (SGL = 0) or single-ended (SGL = 1). For SGL = 0, two adjacent channels can be selected to form a differential input. For SGL = 1, one of 4 channels is selected as the positive input. The negative input is COM for all single-ended operations. The remaining four bits (ODD, A2, A1, A0) determine which channel(s) is/are selected and the polarity (for a differential input).

Once the first word is written into the device, a second word may be input in order to select a configuration mode. The first bit of the second word is the enable bit for the conversion configuration (EN2). If this bit is set to 0, then the next conversion is performed using the previously selected converter configuration.

The second set of configuration data can be loaded into the device (see Table 4). The first bit (IM) is used to select the internal temperature sensor. If IM = 1, the following conversion will be performed on the internal temperature sensor rather than the selected input channel. The next two bits (FA and FB) are used to set the rejection frequency. The next bit (SPD) is used to select either the 1x output rate if SPD = 0 (auto-calibration is enabled and the offset is continuously calibrated and removed from the final conversion result) or the 2x output rate if SPD = 1 (offset calibration disabled, multiplexing output rates up to 15Hz with no latency). The final three bits (GS2, GS1, GS0) are used to set the gain. When IM = 1 (temperature measurement) SPD, GS2, GS1 and GS0 will be ignored and the device will operate in 1x mode.

Table 4. Converter Configuration

1	0	EN	SGL	ODD	A2	A1	A0	EN2	IM	FA	FB	SPD	GS2	GS1	GS0	CONVERTER CONFIGURATION
1	0	0	Any Input Channel					X	X	X	X	X	X	X	X	Keep Previous
1	0	1						0	X	X	X	X	X	X	X	Keep Previous
1	0	1						1	0	Any Rejection Mode		0	0	0	0	External Input, Gain = 1, Autocalibration
1	0	1						1	0			0	0	0	1	External Input, Gain = 4, Autocalibration
1	0	1						1	0			0	0	1	0	External Input, Gain = 8, Autocalibration
1	0	1						1	0			0	0	1	1	External Input, Gain = 16, Autocalibration
1	0	1						1	0			0	1	0	0	External Input, Gain = 32, Autocalibration
1	0	1						1	0			0	1	0	1	External Input, Gain = 64, Autocalibration
1	0	1						1	0			0	1	1	0	External Input, Gain = 128, Autocalibration
1	0	1						1	0			0	1	1	1	External Input, Gain = ~~264~~, Autocalibration
1	0	1						1	0			1	0	0	0	External Input, Gain = 1, 2x Speed
1	0	1						1	0			1	0	0	1	External Input, Gain = 2, 2x Speed
1	0	1						1	0			1	0	1	0	External Input, Gain = 4, 2x Speed
1	0	1						1	0			1	0	1	1	External Input, Gain = 8, 2x Speed
1	0	1						1	0			1	1	0	0	External Input, Gain = 16, 2x Speed
1	0	1						1	0			1	1	0	1	External Input, Gain = 32, 2x Speed
1	0	1						1	0			1	1	1	0	External Input, Gain = 64, 2x Speed
1	0	1						1	0			1	1	1	1	External Input, Gain = 128, 2x Speed
1	0	1						1	0	0	0	Any Speed	Any Gain			External Input, Simultaneous 50Hz/60Hz Rejection
1	0	1						1	0	0	1					External Input, 50Hz Rejection
1	0	1						1	0	1	0					External Input, 60Hz Rejection
1	0	1						1	0	1	1					Reserved, Do Not Use
1	0	1						1	1	0	0	X	X	X	X	Temperature Input, Simultaneous 50Hz/60Hz Rejection
1	0	1						1	1	0	1	X	X	X	X	Temperature Input, 50Hz Rejection
1	0	1						1	1	1	0	X	X	X	X	Temperature Input, 60Hz Rejection
1	0	1						1	1	1	1	X	X	X	X	Reserved, Do Not Use

256

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10		1000 ~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV}	Conversion Time	Simultaneous 50Hz/60Hz External Oscillator	●	144.1	146.9 41036/f_{EOSC} (in kHz)	149.9	ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Notes 10, 17) External Oscillator (Notes 10, 11, 15)			38.4 f_{EOSC}/8		kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Notes 10, 17)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Notes 10, 11, 15)	●			4000	kHz
t_{LESCK}	External SCK Low Period	(Notes 10, 11, 15)	●	125			ns
t_{HESCK}	External SCK High Period	(Notes 10, 11, 15)	●	125			ns
t_{DOUT_ISCK}	Internal SCK 24-Bit Data Output Time	Internal Oscillator (Notes 10, 17) External Oscillator (Notes 10, 11, 15)	●	0.61	0.625 192/f_{EOSC} (in kHz)	0.64	ms ms
t_{DOUT_ESCK}	External SCK 24-Bit Data Output Time				24/f_{ESCK} (in kHz)		ms
t_1	$\overline{CS}$↓ to SDO Low		●	0		200	ns
t_2	$\overline{CS}$↑ to SDO High Z		●	0		200	ns
t_3	$\overline{CS}$↓ to SCK↓	Internal SCK Mode	●	0		200	ns
t_4	$\overline{CS}$↓ to SCK↑	External SCK Mode	●	50			ns
t_{KQMAX}	SCK↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$↓		●	50			ns
t_7	SDI Setup Before SCK↑	(Note 5)	●	100			ns
t_8	SDI Hold After SCK↑	(Note 5)	●	100			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: Unless otherwise specified:

V_{CC} = 2.7V to 5.5V

$V_{REFCM} = V_{REF}/2$, $F_S = 0.5V_{REF}$

$V_{IN} = IN^+ - IN^-$, $V_{IN(CM)} = (IN^+ + IN^-)/2$,
where IN^+ and IN^- are the selected input channels.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless other wise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The SCK can be configured in external SCK mode or internal SCK mode. In external SCK mode, the SCK pin is used as a digital input and the driving clock is f_{ESCK}. In the internal SCK mode, the SCK pin is used as a digital output and the output clock signal during the data output is f_{ISCK}.

Note 11: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses its internal oscillator.

Note 13: The output noise includes the contribution of the internal calibration operations. $V_{REF} \le V_{CC}$.

Note 14: Guaranteed by design and test correlation.

Note 15: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

Note 16: Refer to Applications Information section for performance vs data rate graphs.

Note 17: The converter in internal SCK mode of operation such that the SCK pin is used as a digital output.

Note 18: For V_{CC} < 3V, V_{IH} is 2.5V for pin f_O.

The LTC2488 input measurement range is -0.5*VREF to +0.5*VREF in both differential and single-ended configurations as shown in Figure 28. Highest linearity is achieved with Fully Differential drive and a constant common-mode voltage (Figure 28b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

APPLICATIONS INFORMATION

enables external RC networks and high impedance sensors to directly interface to the LTC2488 without external amplifiers. The remaining common mode input current is eliminated by either balancing the differential input impedances or setting the common mode input equal to the common mode reference (see Automatic Differential Input Current Cancellation Section). This unique architecture does not require on-chip buffers, thereby enabling signals to swing beyond ground and V_{CC}. Moreover, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2488 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2V. This feature guarantees the integrity of the conversion result, input channel selection, and serial clock mode.

When V_{CC} rises above this threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channel IN^+ = CH0, IN^- = CH1. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$).

The LTC2488 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front end circuits. Since the transition noise is well below 1LSB (0.02LSB), a decrease in reference voltage will proportionally improve the converter resolution and improve INL.

Input Voltage Range

The analog inputs are truly differential with an absolute, common mode range for the CH0 to CH3 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2488 converts the bipolar differential input signal $V_{IN} = IN^+ - IN^-$ (where IN^+ and IN^- are the selected input channels), from –FS = $-0.5 \cdot V_{REF}$ to +FS = $0.5 \cdot V_{REF}$ where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes (see Table 1).

Signals applied to the input (CH0 to CH3, COM) may extend 300mV below ground and above V_{CC}. In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

SERIAL INTERFACE PINS

The LTC2488 transmits the conversion result, reads the input channel selection, and receives a start of conversion command through a synchronous 3- or 4-wire interface. During the conversion and sleep states, this interface can be used to access the converter status. During the data output state, it is used to read the conversion result and program the input channel.

Serial Clock Input/Output (SCK)

The serial clock pin (SCK) is used to synchronize the data input/output transfer. Each bit is shifted out of the SDO pin on the falling edge of SCK and data is shifted into the SDI pin on the rising edge of SCK.

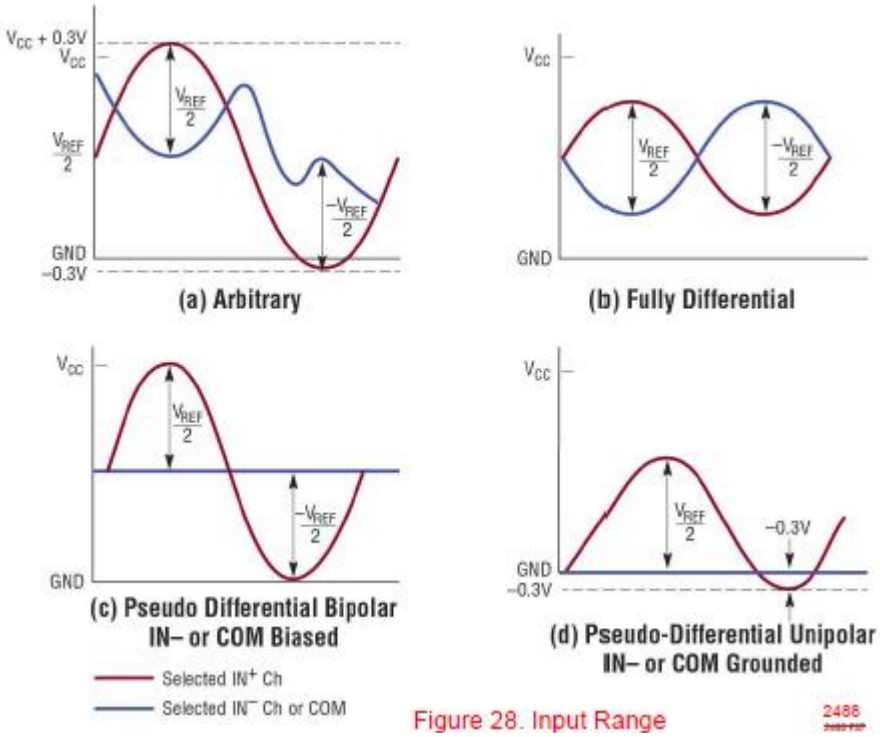

Figure 28. Input Range

2488

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10		1000 ~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		50	µs
t_{LEO}	External Oscillator Low Period		●	0.125		50	µs
t_{CONV}	Conversion Time	Internal Oscillator External Oscillator (Note 10)	●	144.1	146.9 41036/f_{EOSC} (in kHz)	149.9	ms ms

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3, 15)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(STA)}$	Hold Time (Repeated) Start Condition		●	0.6			µs
t_{LOW}	Low Period of the SCL Pin		●	1.3			µs
t_{HIGH}	High Period of the SCL Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated Start Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for SDA Signals	(Note 14)	●	$20 + 0.1C_B$		300	ns
t_f	Fall Time for SDA Signals	(Note 14)	●	$20 + 0.1C_B$		300	ns
$t_{SU(STO)}$	Set-Up Time for Stop Condition		●	0.6			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified.

$V_{REFCM} = V_{REF}/2$, $F_S = 0.5V_{REF}$

$V_{IN} = IN^+ – IN^–$, $V_{IN(CM)} = (IN^+ – IN^–)/2$,
where IN^+ and $IN^–$ are the selected input channels.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 11: The converter uses its internal oscillator.

Note 12: The output noise includes the contribution of the internal calibration operations.

Note 13: Guaranteed by design and test correlation.

Note 14: C_B = capacitance of one bus line in pF (10pF ≤ C_B ≤ 400pF).

Note 15: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 16: Refer to Applications Information section for performance versus data rate graphs.

APPLICATIONS INFORMATION

cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2489 automatically enters an internal reset state when the power supply voltage, V_{CC}, drops below approximately 2.0V. This feature guarantees the integrity of the conversion result and input channel selection.

When V_{CC} rises above this threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channels IN^+ = CH0 and IN^- = CH1. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential, external reference voltage. The absolute/common mode voltage range for the REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$).

The LTC2489 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front end circuits. Since the transition noise is well below 1LSB (0.02LSB), a decrease in reference voltage will proportionally improve the converter resolution and improve INL.

Input Voltage Range

The analog inputs are truly differential with an absolute, common mode range for the CH0-CH3 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Within these limits, the LTC2489 converts the bipolar differential input signal $V_{IN} = IN^+ – IN^-$ (where IN^+ and IN^- are the selected input channels), from $–FS = –0.5 \bullet V_{REF}$ to $+FS = 0.5 \bullet V_{REF}$ where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes (see Table 1).

In order to limit any fault current due to input ESD leakage current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

I²C INTERFACE

The LTC2489 communicates through an I^2C interface. The I^2C interface is a 2-wire open-drain interface supporting multiple devices and multiple masters on a single bus. The connected devices can only pull the data line (SDA) low and can never drive it high. SDA is required to be externally connected to the supply through a pull-up resistor. When the data line is not being driven, it is high. Data on the I^2C bus can be transferred at rates up to 100kbits/s in the standard mode and up to 400kbits/s in the fast mode. The V_{CC} power should not be removed from the device when the I^2C bus is active to avoid loading the I^2C bus lines through the internal ESD protection diodes.

Each device on the I^2C bus is recognized by a unique address stored in that device and can operate either as a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. Devices addressed by the master are considered a slave.

The LTC2489 can only be addressed as a slave. Once addressed, it can receive channel selection bits or transmit the last conversion result. The serial clock line, SCL, is always an input to the LTC2489 and the serial data line SDA is bidirectional. The device supports the standard mode and the fast mode for data transfer speeds up to 400kbits/s. Figure 2 shows the definition of the I^2C timing.

The LTC2489 input measurement range is -0.5*VREF to +0.5*VREF in both differential and single-ended configurations as shown in Figure 27. Highest linearity is achieved with Fully Differential drive and a constant common-mode voltage (Figure 27b). Other drive schemes may incur an INL error approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

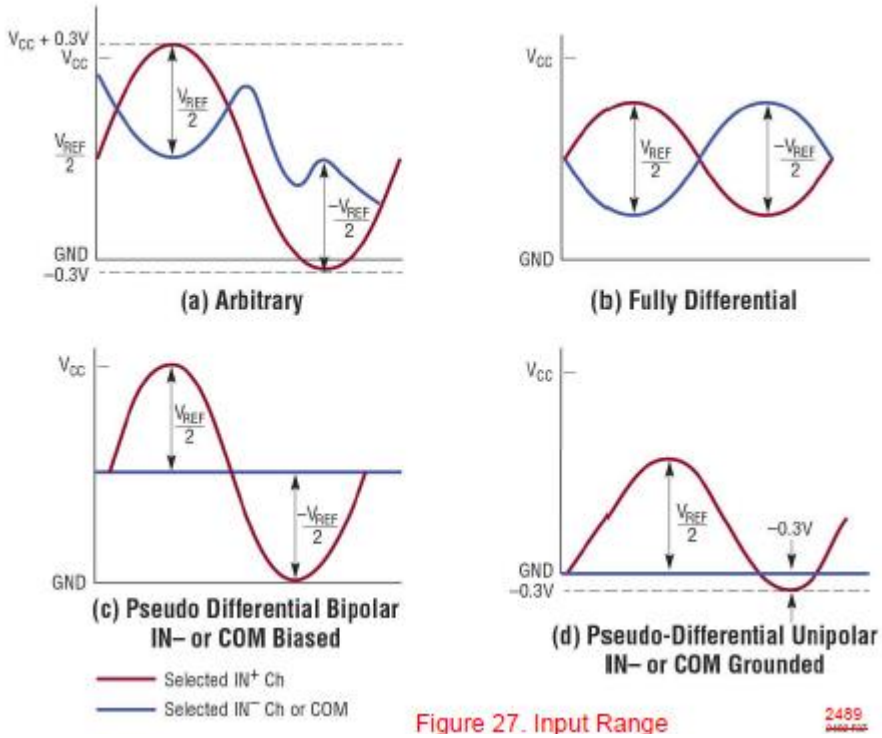

Figure 27. Input Range

2489

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10		1000~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV_1}	Conversion Time for 1x Speed Mode	50Hz Mode 60Hz Mode Simultaneous 50/60Hz Mode External Oscillator	● ● ●	157.2 131 144.1	160.3 133.6 146.9 41036/f_{EOSC} (in kHz)	163.5 136.3 149.9	ms ms ms ms
t_{CONV_2}	Conversion Time for 2x Speed Mode	50Hz Mode 60Hz Mode Simultaneous 50/60Hz Mode External Oscillator	● ● ●	78.7 65.6 72.2	80.3 66.9 73.6 20556/f_{EOSC} (in kHz)	81.9 68.2 75.1	ms ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Notes 10, 17) External Oscillator (Notes 10, 11, 15)			38.4 f_{EOSC}/8		kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Notes 10, 17)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Notes 10, 11, 15)	●			4000	kHz
t_{LESCK}	External SCK Low Period	(Notes 10, 11, 15)	●	125			ns
t_{HESCK}	External SCK High Period	(Notes 10, 11, 15)	●	125			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 17) External Oscillator (Notes 10, 11, 15)	●	0.81	0.83 256/f_{EOSC} (in kHz)	0.85	ms ms
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Notes 10, 11, 15)			32/f_{ESCK} (in kHz)		ms
t_1	$\overline{CS}$↓ to SDO Low		●	0		200	ns
t_2	$\overline{CS}$↑ to SDO Hi-Z		●	0		200	ns
t_3	$\overline{CS}$↓ to SCK↓	Internal SCK Mode	●	0		200	ns
t_4	$\overline{CS}$↓ to SCK↑	External SCK Mode	●	50			ns
t_{KQMAX}	SCK↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK↓	(Note 5)	●	15			ns
t_5	SCK Set Up Before $\overline{CS}$↓		●	50			ns
t_7	SDI Set Up Before SCK↑	(Note 5)	●	100			ns
t_8	SDI Hold After SCK↑	(Note 5)	●	100			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: Unless otherwise specified:

V_{CC} = 2.7V to 5.5V

$V_{REFCM} = V_{REF}/2$, $F_S = 0.5V_{REF}$

$V_{IN} = IN^+ - IN^-$, $V_{IN(CM)} = (IN^+ - IN^-)/2$,
where IN^+ and IN^- are the selected input channels.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless other wise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The SCK can be configured in external SCK mode or internal SCK mode. In external SCK mode, the SCK pin is used as a digital input and the driving clock is f_{ESCK}. In the internal SCK mode, the SCK pin is used as a digital output and the output clock signal during the data output is f_{ISCK}.

Note 11: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses its internal oscillator.

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: Guaranteed by design and test correlation.

Note 15: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

Note 16: Refer to Applications Information section for performance vs data rate graphs.

Note 17: The converter in internal SCK mode of operation such that the SCK pin is used as a digital output.

Note 18: For V_{CC} < 3V, V_{IH} is 2.5V for pin f_O.

The LTC2492 input measurement range is -0.5*VREF to +0.5*VREF in both differential and single-ended configurations as shown in Figure 38. Highest linearity is achieved with Fully Differential drive and a constant common-mode voltage (Figure 38b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

APPLICATIONS INFORMATION

Easy Drive Input Current Cancellation

The LTC2492 combines a high precision delta-sigma ADC with an automatic, differential, input current cancellation front end. A proprietary front-end passive sampling network transparently removes the differential input current. This enables external RC networks and high impedance sensors to directly interface to the LTC2492 without external amplifiers. The remaining common mode input current is eliminated by either balancing the differential input impedances or setting the common mode input equal to the common mode reference (see Automatic Differential Input Current Cancellation Section). This unique architecture does not require on-chip buffers, thereby enabling signals to swing beyond ground and V_{CC}. Moreover, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2492 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2V. This feature guarantees the integrity of the conversion result, input channel selection and serial clock mode.

When V_{CC} rises above this threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channel IN^+ = CH0, IN^- = CH1, simultaneous 50Hz/60Hz rejection and 1× output rate. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel, rejection mode, speed mode, or temperature selection can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$).

The LTC2492 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a decreased reference will improve the converter's overall INL performance.

Input Voltage Range

The analog inputs are truly differential with an absolute, common mode range for the CH0 to CH3 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2492 converts the bipolar differential input signal $V_{IN} = IN^+ - IN^-$ (where IN^+ and IN^- are the selected input channels), from –FS = $-0.5 \cdot V_{REF}$ to +FS = $0.5 \cdot V_{REF}$ where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes (see Table 1).

Signals applied to the input (CH0 to CH3, COM) may extend 300mV below ground and above V_{CC}. In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

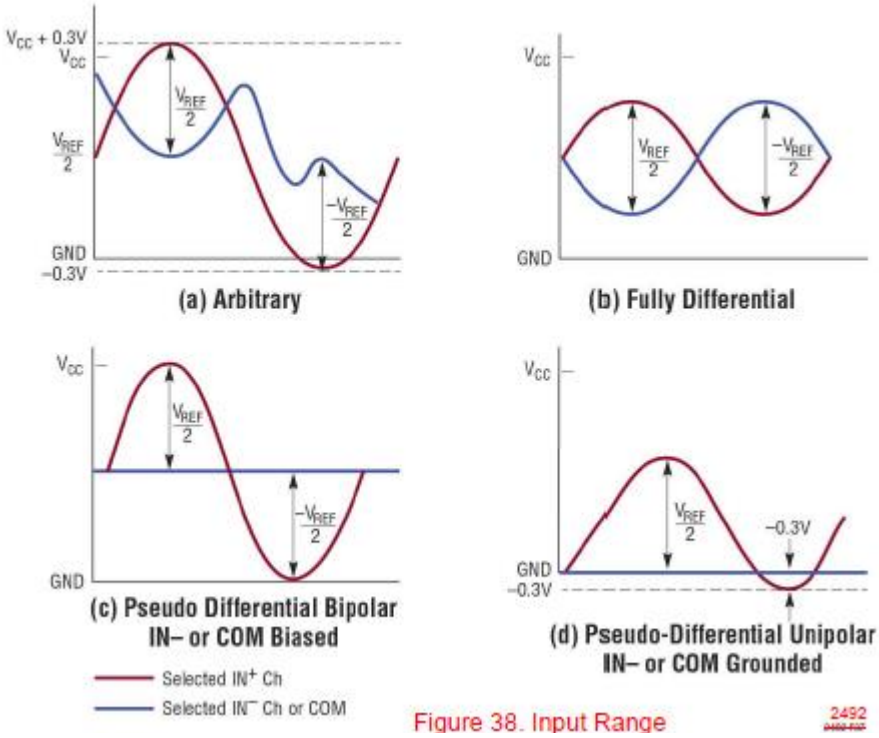

Figure 38. Input Range

2492

APPLICATIONS INFORMATION

1/0†

Table 2. Output Data Format

DIFFERENTIAL INPUT VOLTAGE V_{IN}*	BIT 31 EOC	BIT 30 DMY	BIT 29 SIG	BIT 28 MSB	BIT 27	BIT 26	BIT 25	...	BIT 5 LSB	BITS 4 to 0 SUB LSBs
V_{IN}* ≥ 0.5 • V_{REF}**	0	0	1	1	0	0	0	...	0	00000
0.5 • V_{REF}** – 1LSB	0	0	1	0	1	1	1	...	1	XXXXX
0.25 • V_{REF}**	0	0	1	0	1	0	0	...	0	XXXXX
0.25 • V_{REF}** – 1LSB	0	0	~~1/0~~†	0	0	1	1	...	1	XXXXX
0	0	0	~~1~~	0	0	0	0	...	0	XXXXX
–1LSB	0	0	0	1	1	1	1	...	1	XXXXX
–0.25 • V_{REF}**	0	0	0	1	1	0	0	...	0	XXXXX
–0.25 • V_{REF}** – 1LSB	0	0	0	1	0	1	1	...	1	XXXXX
–0.5 • V_{REF}**	0	0	0	1	0	0	0	...	0	XXXXX
V_{IN}* < –0.5 • V_{REF}**	0	0	0	0	1	1	1	...	~~1~~ X	~~11111~~ XXXXX ****

*The differential input voltage V_{IN} = IN^+ – IN^-.
**The differential reference voltage V_{REF} = REF^+ – REF^-. Sub LSBs are below the 24-bit level. They may be included in averaging, or discarded without loss of resolution.
†The sign bit changes state during the 0 output code when the device is operating in the 2x speed mode.
****The underrange output code is 0X0FFFFXXX in 2x mode.

conversion automatically begins at power up using this default configuration. Once the conversion is complete, a new word may be written into the device.

The first three bits shifted into the device consist of two preamble bits and an enable bit. These bits are used to enable the device configuration and input channel selection. Valid settings for these three bits are 000, 100 and 101. Other combinations should be avoided. If the first three bits are 000 or 100, the following data is ignored (don't care) and the previously selected input channel and configuration remain valid for the next conversion.

If the first three bits shifted into the device are 101, then the next five bits select the input channel for the next conversion cycle (see Table 3).

Table 3 Channel Selection

MUX ADDRESS					CHANNEL SELECTION				
SGL	ODD/ SIGN	A2	A1	A0	0	1	2	3	COM
*0	0	0	0	0	IN^+	IN^-			
0	0	0	0	1			IN^+	IN^-	
0	1	0	0	0	IN^-	IN^+			
0	1	0	0	1			IN^-	IN^+	
1	0	0	0	0	IN^+				IN^-
1	0	0	0	1			IN^+		IN^-
1	1	0	0	0		IN^+			IN^-
1	1	0	0	1				IN^+	IN^-

*Default at power up

The first input bit (SGL) following the 101 sequence determines if the input selection is differential (SGL = 0) or single-ended (SGL = 1). For SGL = 0, two adjacent channels can be selected to form a differential input. For SGL = 1, one of four channels is selected as the positive input. The negative input is COM for all single-ended operations. The remaining four bits (ODD, A2, A1, A0) determine which channel(s) is/are selected and the polarity (for a differential input).

The next serial input bit immediately following the input channel selection is the enable bit for the conversion configuration (EN2). If this bit is set to 0, then the next conversion is performed using the previously selected converter configuration.

A new configuration can be loaded into the device by setting EN2 = 1 (see Table 4). The first bit (IM) is used to select the internal temperature sensor. If IM = 1, the following conversion will be performed on the internal temperature sensor rather than the selected input channel. The next two bits (FA and FB) are used to set the rejection frequency. The final bit (SPD) is used to select either the 1x output rate if SPD = 0 (auto-calibration is enabled and the offset is continuously calibrated and removed from the final conversion result) or the 2x output rate if SPD = 1 (offset calibration disabled, multiplexing output rates up to 15Hz with no latency). When IM = 1 (temperature measurement) SPD will be ignored and the device will operate in 1× mode. The configuration remains valid until

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current	Conversion Current (Note 11)	●		160	275	µA
		Temperature Measurement (Note 11)	●		200	300	µA
		Sleep Mode (Note 11)	●		1	2	µA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10		1000 ~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		50	µs
t_{LEO}	External Oscillator Low Period		●	0.125		50	µs
t_{CONV_1}	Conversion Time for 1× Speed Mode	50Hz Mode	●	157.2	160.3	163.5	ms
		60Hz Mode	●	131	133.6	136.3	ms
		Simultaneous 50Hz/60Hz Mode	●	144.1	146.9	149.9	ms
		External Oscillator (Note 10)			41036/f_{EOSC} (in kHz)		ms
t_{CONV_2}	Conversion Time for 2× Speed Mode	50Hz Mode	●	78.7	80.3	81.9	ms
		60Hz Mode	●	65.6	66.9	68.2	ms
		Simultaneous 50Hz/60Hz Mode	●	72.2	73.6	75.1	ms
		External Oscillator (Note 10)			20556/f_{EOSC} (in kHz)		ms

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3, 15)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(STA)}$	Hold Time (Repeated) START Condition		●	0.6			µs
t_{LOW}	LOW Period of the SCL Pin		●	1.3			µs
t_{HIGH}	HIGH Period of the SCL Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated START Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for SDA Signals	(Note 14)	●	20 + 0.1C_B		300	ns
t_f	Fall Time for SDA Signals	(Note 14)	●	20 + 0.1C_B		300	ns
$t_{SU(STO)}$	Set-Up Time for STOP Condition		●	0.6			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: Unless otherwise specified: V_{CC} = 2.7V to 5.5V

$V_{REFCM} = V_{REF}/2$, $f_S = 0.5V_{REF}$

$V_{IN} = IN^+ - IN^-$, $V_{IN(CM)} = (IN^+ - IN^-)/2$,
where IN^+ and IN^- are the selected input channels.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 11: The converter uses its internal oscillator.

Note 12: The output noise includes the contribution of the internal calibration operations.

Note 13: Guaranteed by design and test correlation.

Note 14: C_B = capacitance of one bus line in pF (10pF ≤ C_B ≤ 400pF).

Note 15: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 16: Refer to Applications Information section for Performance vs Data Rate graphs.

The LTC2493 input measurement range is -0.5*VREF in both differential and single-ended configurations as shown in Figure 37. Highest linearity is achieved wit Fully Differential drive and a constant common-mode voltage (Figure 37b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

APPLICATIONS INFORMATION

signals to swing beyond ground and V_{CC}. Moreover, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full-scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2493 automatically enters an internal reset state when the power supply voltage, V_{CC}, drops below approximately 2.0V. This feature guarantees the integrity of the conversion result and input channel selection.

When V_{CC} rises above this threshold, the converter creates an internal power-on reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channel IN^+ = CH0, IN^- = CH1 with simultaneous 50Hz/60Hz rejection and 1x output rate. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel, rejection mode, speed mode, or temperature selection can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for the REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$).

The LTC2493 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front end circuits and, as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a decreased reference will improve the converter's overall INL performance.

Input Voltage Range

The analog inputs are truly differential with an absolute, common mode range for the CH0-CH3 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2493 converts the bipolar differential input signal $V_{IN} = IN^+ - IN^-$ (where IN^+ and IN^- are the selected input channels), from $-FS = -0.5 \cdot V_{REF}$ to $+FS = 0.5 \cdot V_{REF}$ where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes (see Table 1).

In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

I^2C INTERFACE

The LTC2493 communicates through an I^2C interface. The I^2C interface is a 2-wire open-drain interface supporting multiple devices and multiple masters on a single bus. The connected devices can only pull the data line (SDA) low and can never drive it high. SDA is required to be externally connected to the supply through a pull-up resistor. When the data line is not being driven, it is high. Data on the I^2C bus can be transferred at rates up to 100kbits/s in the standard mode and up to 400kbits/s in the fast mode. The V_{CC} power should not be removed from the device when the I^2C bus is active to avoid loading the I^2C bus lines through the internal ESD protection diodes.

Each device on the I^2C bus is recognized by a unique address stored in that device and can operate either as a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals

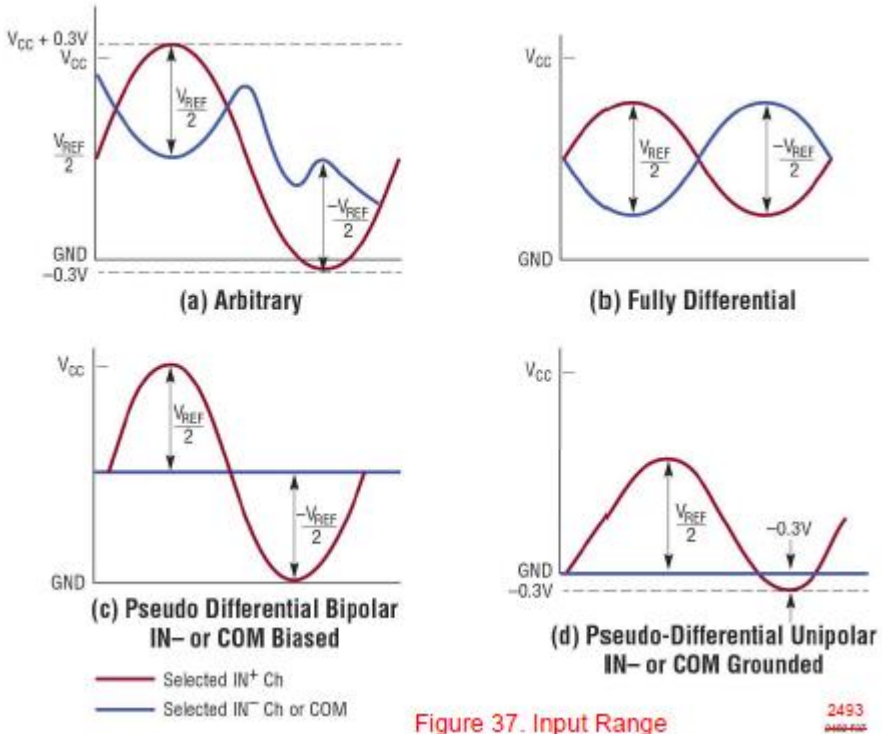

Figure 37. Input Range

APPLICATIONS INFORMATION

DATA OUTPUT FORMAT

The output register contains the last conversion result. After each conversion is completed, the device automatically enters the sleep state where the supply current is reduced to 1µA. When the LTC2493 is addressed for a read operation, it acknowledges (by pulling SDA low) and acts as a transmitter. The master/receiver can read up to four bytes from the LTC2493. After a complete read operation (4 bytes), a new conversion is initiated. The device will NACK subsequent read operations while a conversion is being performed.

The data output stream is 32 bits long and is shifted out on the falling edges of SCL (see Figure 3a). The first bit is the conversion result sign bit (SIG) (see Tables 1 and 2). This bit is high if $V_{IN} \geq 0$ and low if $V_{IN} < 0$ (where V_{IN} corresponds to the selected input signal $IN^+ - IN^-$). The second bit is the most significant bit (MSB) of the result. The first two bits (SIG and MSB) can be used to indicate over and under range conditions (see Table 2). If both bits are high, the differential input voltage is equal to or above +FS. If both bits are set low, the input voltage is below –FS. The function of these bits is summarized in Table 2. The 24 bits following the MSB bit are the conversion result in binary two's, complement format. The remaining six bits are sub LSBs below the 24-bit level.

As long as the voltage on the selected input channels (IN^+ and IN^-) remains between –0.3V and V_{CC} + 0.3V (absolute maximum operating range) a conversion result is generated for any differential input voltage V_{IN} from –FS = –0.5 • V_{REF} to +FS = 0.5 • V_{REF}. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to +FS. For differential input voltages below –FS, the conversion result is clamped to the value –FS – 1 LSB.

Table 2. LTC2493 Status Bits

INPUT RANGE	BIT 31 SIG	BIT 30 MSB
$V_{IN} \geq FS$	1	1
$0V \leq V_{IN} < FS$	1/0	0
$-FS \leq V_{IN} < 0V$	0	1
$V_{IN} < -FS$	0	0

Table 1. Output Data Format

DIFFERENTIAL INPUT VOLTAGE V_{IN}*	BIT 31 SIG	BIT 30 MSB	BIT 29	BIT 28	BIT 27	...	BIT 6 LSB	BITS 5-0 Sub LSBs
V_{IN}* ≥ FS**	1	1	0	0	0	...	0	00000
FS** – 1 LSB	1	0	1	1	1	...	1	XXXXX
0.5 • FS**	1	0	1	0	0	...	0	XXXXX
0.5 • FS** – 1 LSB	1	0	0	1	1	...	1	XXXXX
0	1/0†	0	0	0	0	...	0	XXXXX
–1 LSB	0	1	1	1	1	...	1	XXXXX
–0.5 • FS**	0	1	1	0	0	...	0	XXXXX
–0.5 • FS** – 1 LSB	0	1	0	1	1	...	1	XXXXX
–FS**	0	1	0	0	0	...	0	XXXXX
V_{IN}* < –FS**	0	0	1	1	1	...	X ~~1~~	~~11111~~ XXXXX ***

*The differential input voltage $V_{IN} = IN^+ - IN^-$.
**The full-scale voltage FS = 0.5 • V_{REF}. Sub LSBs are below the 24-bit level. They may be included in averaging, or discarded without loss of resolution.
†The sign bit changes state during the 0 output code when the device is operating in the 2x speed mode.
*** The underrange output code is 0X3FFFFXXX in 2x mode

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10	1000	~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		50	µs
t_{LEO}	External Oscillator Low Period		●	0.125		50	µs
t_{CONV_1}	Conversion Time for 1x Speed Mode	50Hz Mode 60Hz Mode Simultaneous 50/60Hz Mode External Oscillator	● ● ●	157.2 131 144.1	160.3 133.6 146.9 41036/f_{EOSC} (in kHz)	163.5 136.3 149.9	ms ms ms ms
t_{CONV_2}	Conversion Time for 2x Speed Mode	50Hz Mode 60Hz Mode Simultaneous 50/60Hz Mode External Oscillator	● ● ●	78.7 65.6 72.2	80.3 66.9 73.6 20556/f_{EOSC} (in kHz)	81.9 68.2 75.1	ms ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Notes 10, 17) External Oscillator (Notes 10, 11, 15)			38.4 f_{EOSC}/8		kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Notes 10, 17)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Notes 10, 11, 15)	●			4000	kHz
t_{LESCK}	External SCK LOW Period	(Notes 10, 11, 15)	●	125			ns
t_{HESCK}	External SCK HIGH Period	(Notes 10, 11, 15)	●	125			ns
t_{DOUT_ISCK}	Internal SCK 24-Bit Data Output Time	Internal Oscillator (Notes 10, 17) External Oscillator (Notes 10, 11, 15)	●	0.61	0.625 192/f_{EOSC} (in kHz)	0.64	ms ms
t_{DOUT_ESCK}	External SCK 24-Bit Data Output Time	(Notes 10, 11, 15)			24/f_{ESCK} (in kHz)		ms
t_1	$\overline{CS}$↓ to SDO LOW		●	0		200	ns
t_2	$\overline{CS}$↑ to SDO Hi-Z		●	0		200	ns
t_3	$\overline{CS}$↓ to SCK↑	Internal SCK Mode	●	0		200	ns
t_4	$\overline{CS}$↓ to SCK↑	External SCK Mode	●	50			ns
t_{KQMAX}	SCK↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$↓		●	50			ns
t_7	SDI Setup Before SCK↑	(Note 5)	●	100			ns
t_8	SDI Hold After SCK↑	(Note 5)	●	100			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified.

$V_{REFCM} = V_{REF}/2$, $f_S = 0.5V_{REF}$/Gain

$V_{IN} = IN^+ - IN^-$, $V_{IN(CM)} = (IN^+ - IN^-)/2$,
where IN^+ and IN^- are the selected input channels.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless other wise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The SCK can be configured in external SCK mode or internal SCK mode. In external SCK mode, the SCK pin is used as a digital input and the driving clock is f_{ESCK}. In the internal SCK mode, the SCK pin is used as a digital output and the output clock signal during the data output is f_{ISCK}.

Note 11: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses its internal oscillator.

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: Guaranteed by design and test correlation.

Note 15: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

Note 16: Refer to Applications Information section for performance vs data rate graphs.

Note 17: The converter is in internal SCK mode of operation such that the SCK pin is used as a digital output.

Note 18: For V_{CC} < 3V, V_{IH} is 2.5V for Pin f_O.

The LTC2494 input measurement range is -0.5*VREF to +0.5*VREF in both differential and single-ended configurations as shown in Figure 39. Highest linearity is achieved with Fully Differential drive and a constant common-mode voltage (Figure39b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

APPLICATIONS INFORMATION

transparently removes the differential input current. This enables external RC networks and high impedance sensors to directly interface to the LTC2494 without external amplifiers. The remaining common mode input current is eliminated by either balancing the differential input impedances or setting the common mode input equal to the common mode reference (see the Automatic Differential Input Current Cancellation section). This unique architecture does not require on-chip buffers, thereby enabling signals to swing beyond ground or up to V_{CC}. Moreover, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full-scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2494 automatically enters an internal reset state when the power supply voltage, V_{CC}, drops below approximately 2V. This feature guarantees the integrity of the conversion result, input channel selection and serial clock mode.

When V_{CC} rises above this threshold, the converter creates an internal power-on reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channels IN^+ = CH0 and IN^- = CH1 with simultaneous 50Hz/60Hz rejection 1x output rate, and gain = 1. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel, rejection mode, speed mode, temperature selection, or gain can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for the REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$).

The LTC2494 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front end circuits, and as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a decreased reference will improve the converter's overall INL performance.

Input Voltage Range

The analog input is truly differential with an absolute, common mode range for CH0 to CH15 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD projection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2494 converts the bipolar differential input signal $V_{IN} = IN^+ + IN^-$ (where IN^+ and IN^- are the selected input channels), from $-FS = -0.5 \cdot V_{REF}/Gain$ to $+FS = 0.5 \cdot V_{REF}/Gain$ where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes.

Signals applied to the input (CH0 to CH15, COM) may extend 300mV below ground and above V_{CC}. In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

MUXOUT/ADCIN

The output of the multiplexer (MUXOUT) and the input to the ADC (ADCIN) can be used to perform input signal conditioning on any of the selected input channels or simply shorted together for direct digitization. If an external amplifier is used, the LTC2494 automatically calibrates both the offset and drift of this circuit and the Easy Drive sampling scheme enables a wide variety of amplifiers to be used.

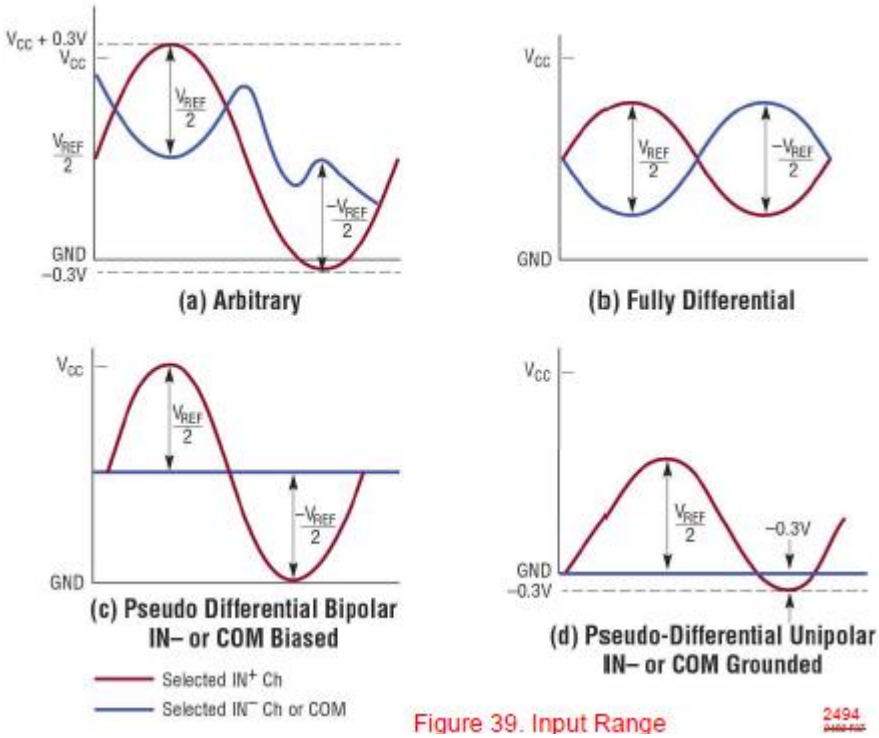

Figure 39. Input Range

2494

APPLICATIONS INFORMATION

Table 4. Converter Configuration

1	0	EN	SGL	ODD	A2	A1	A0	EN2	IM	FA	FB	SPD	GS2	GS1	GS0	CONVERTER CONFIGURATION
1	0	0	Any Input Channel					X	X	X	X	X	X	X	X	Keep Previous
1	0	1						0	X	X	X	X	X	X	X	Keep Previous
1	0	1						1	0	Any Rejection Mode		0	0	0	0	External Input, Gain = 1, Auto-Calibration
1	0	1						1	0			0	0	0	1	External Input, Gain = 4, Auto-Calibration
1	0	1						1	0			0	0	1	0	External Input, Gain = 8, Auto-Calibration
1	0	1						1	0			0	0	1	1	External Input, Gain = 16, Auto-Calibration
1	0	1						1	0			0	1	0	0	External Input, Gain = 32, Auto-Calibration
1	0	1						1	0			0	1	0	1	External Input, Gain = 64, Auto-Calibration
1	0	1						1	0			0	1	1	0	External Input, Gain = 128, Auto-Calibration
1	0	1						1	0			0	1	1	1	External Input, Gain = ~~264~~ 256, Auto-Calibration
1	0	1						1	0			1	0	0	0	External Input, Gain = 1, 2x Speed
1	0	1						1	0			1	0	0	1	External Input, Gain = 2, 2x Speed
1	0	1						1	0			1	0	1	0	External Input, Gain = 4, 2x Speed
1	0	1						1	0			1	0	1	1	External Input, Gain = 8, 2x Speed
1	0	1						1	0			1	1	0	0	External Input, Gain = 16, 2x Speed
1	0	1						1	0			1	1	0	1	External Input, Gain = 32, 2x Speed
1	0	1						1	0			1	1	1	0	External Input, Gain = 64, 2x Speed
1	0	1						1	0			1	1	1	1	External Input, Gain = 128, 2x Speed
1	0	1						1	0	0	0	Any Speed	Any Gain			External Input, Simultaneous 50Hz/60Hz Rejection
1	0	1						1	0	0	1					External Input, 50Hz Rejection
1	0	1						1	0	1	0					External Input, 60Hz Rejection
1	0	1						1	0	1	1					Reserved, Do Not Use
1	0	1						1	1	0	0	X	X	X	X	Temperature Input, Simultaneous 50Hz/60Hz Rejection
1	0	1						1	1	0	1	X	X	X	X	Temperature Input, 50Hz Rejection
1	0	1						1	1	1	0	X	X	X	X	Temperature Input, 60Hz Rejection
1	0	1						1	1	1	1	X	X	X	X	Reserved, Do Not Use

= 1 (offset calibration disabled, multiplexing output rates up to 15Hz with no latency). When IM = 1 (temperature measurement), SPD, GS2, GS1, GS0 will be ignored and the device will operate in 1x mode. The final 3 bits (GS2, GS1, GS0) are used to select the gain. The configuration remains valid until a new input word with EN = 1 (the first 3 bits are 101) and EN2 = 1 is shifted into the device.

Rejection Mode (FA, FB)

The LTC2494 includes a high accuracy on-chip oscillator with no required external components. Coupled with an integrated 4th order digital low pass filter, the LTC2494 rejects line frequency noise. In the default mode, the LTC2494 simultaneously rejects 50Hz and 60Hz by at least 87dB. If more rejection is required, the LTC2494 can be configured to reject 50Hz or 60Hz to better than 110dB.

Speed Mode (SPD)

Every conversion cycle, two conversions are combined to remove the offset (default mode). This result is free from offset and drift. In applications where the offset is not critical, the auto-calibration feature can be disabled with the benefit of twice the output rate. While operating in the 2x mode (SPD = 1), the linearity and full-scale errors are unchanged from the 1x mode performance. In both the 1x and 2x mode there is no latency. This enables input steps or multiplexer changes to settle in a single conversion cycle easing system overhead and increasing the effective conversion rate. During temperature measurements, the 1x mode is always used independent of the value of SPD.

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10	1000	~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV_1}	Conversion Time for 1x Speed Mode	50Hz Mode	●	157.2	160.3	163.5	ms
		60Hz Mode	●	131	133.6	136.3	ms
		Simultaneous 50Hz/60Hz Mode	●	144.1	146.9	149.9	ms
		External Oscillator (Note 10)			41036/f_{EOSC} (in kHz)		ms
t_{CONV_2}	Conversion Time for 2x Speed Mode	50Hz Mode	●	78.7	80.3	81.9	ms
		60Hz Mode	●	65.6	66.9	68.2	ms
		Simultaneous 50Hz/60Hz Mode	●	72.2	73.6	75.1	ms
		External Oscillator (Note 10)			20556/f_{EOSC} (in kHz)		ms

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3, 15)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(SDA)}$	Hold Time (Repeated) START Condition		●	0.6			µs
t_{LOW}	LOW Period of the SCL Pin		●	1.3			µs
t_{HIGH}	HIGH Period of the SCL Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated START Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for SDA Signals	(Note 14)	●	20 + 0.1C_B		300	ns
t_f	Fall Time for SDA Signals	(Note 14)	●	20 + 0.1C_B		300	ns
$t_{SU(STO)}$	Set-Up Time for STOP Condition		●	0.6			µs
t_{BUF}	Bus Free Time Between a Second START Condition		●	1.3			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: Unless otherwise specified: V_{CC} = 2.7V to 5.5V

$V_{REFCM} = V_{REF}/2$, $F_S = 0.5V_{REF}$/Gain

$V_{IN} = IN^+ - IN^-$, $V_{IN(CM)} = (IN^+ - IN^-)/2$,
where IN^+ and IN^- are the selected input channels.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 11: The converter uses its internal oscillator.

Note 12: The output noise includes the contribution of the internal calibration operations.

Note 13: Guaranteed by design and test correlation.

Note 14: C_B = capacitance of one bus line in pF (10pF ≤ C_B ≤ 400pF).

Note 15: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 16: Refer to Applications Information section for Performance vs Data Rate graphs.

The LTC2495 input measurement range is -0.5*VREF to +0.5*VREF in both differential and single-ended configurations as shown in Figure 38. Highest linearity is achieved with Fully Differential drive and a constant common-mode voltage (Figure 38b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

APPLICATIONS INFORMATION

cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full-scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2495 automatically enters an internal reset state when the power supply voltage, V_{CC}, drops below a threshold of approximately 2.0V. This feature guarantees the integrity of the conversion result and input channel selection.

When V_{CC} rises above this threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channels IN^+ = CH0 and IN^- = CH1 with simultaneous 50Hz/60Hz rejection, 1x output rate, and gain = 1. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel, rejection mode, speed mode, temperature selection or gain can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for the REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$).

The LTC2495 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front-end circuits and, as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a decreased reference will improve the converter's overall INL performance.

Input Voltage Range

The analog inputs are truly differential with an absolute, common mode range for the CH0-CH15 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2495 converts the bipolar differential input signal $V_{IN} = IN^+ - IN^-$ (where IN^+ and IN^- are the selected input channels), from $-FS = -0.5 \cdot V_{REF}/Gain$ to $+FS = 0.5 \cdot V_{REF}/Gain$ where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes (see Table 1).

Signals applied to the input (CH0-CH15, COM) may extend 300mV below ground and above V_{CC}. In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

MUXOUT/ADCIN

The outputs of the multiplexer (MUXOUTP/MUXOUTN) and the inputs to the ADC (ADCINP/ADCINN) can be used to perform input signal conditioning on any of the selected input channels or simply shorted together for direct digitization. If an external amplifier is used, the LTC2495 automatically calibrates both the offset and drift of this circuit and the Easy Drive sampling scheme enables a wide variety of amplifiers to be used.

In order to achieve optimum performance, if an external amplifier is not used, short these pins directly together (ADCINP to MUXOUTP and ADCINN to MUXOUTN) and minimize their capacitance to ground.

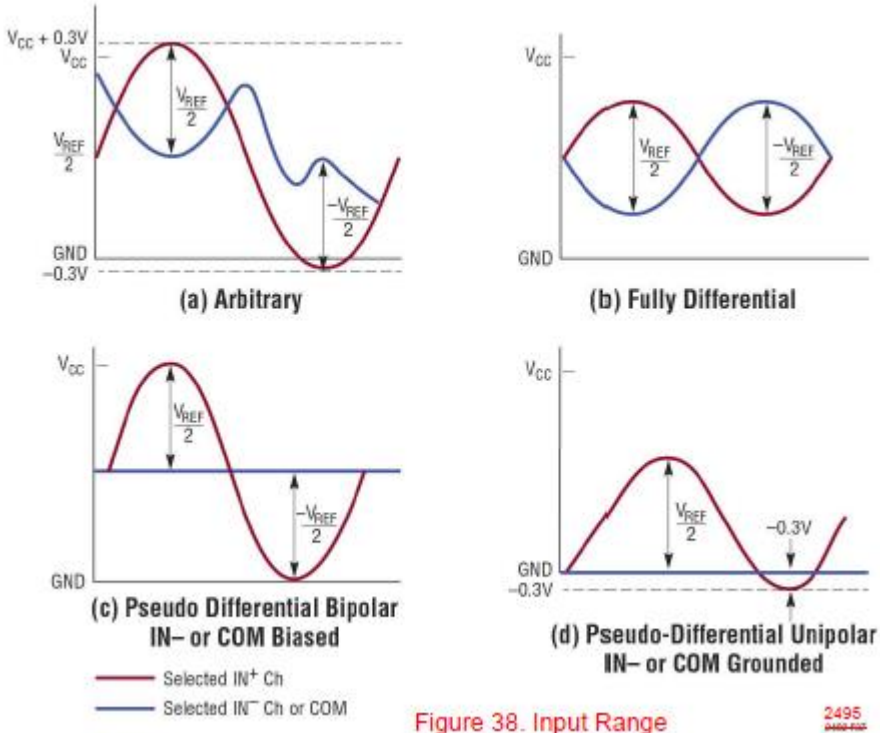

Figure 38. Input Range

2495

APPLICATIONS INFORMATION

one of 16 channels is selected as the positive input. The negative input is COM for all single-ended operations. The remaining four bits (ODD, A2, A1, A0) determine which channel(s) is/are selected and the polarity (for a differential input).

Once the first word is written into the device, a second word may be input in order to select a configuration mode. The first bit of the second word is the enable bit for the conversion configuration (EN2). If this bit is set to 0, then the next conversion is performed using the previously selected converter configuration.

If the EN2 bit is set to a 1, a new configuration can be loaded into the device (see Table 4). The first bit (IM) is used to select the internal temperature sensor. If IM = 1, the following conversion will be performed on the internal temperature sensor rather than the selected input channel. The next two bits (FA and FB) are used to set the rejection frequency. The next bit (SPD) is used to select either the 1x output rate if SPD = 0 (auto-calibration is enabled and the offset is continuously calibrated and removed from the final conversion result) or the 2x output rate if SPD = 1 (offset calibration disabled, multiplexing output rates up to 15Hz with no latency). The final three bits (GS2, GS1, GS0) are used to set the gain. When IM = 1 (temperature measurement) SPD, GS2, GS1 and GS0 will be ignored and the device will operate in 1x mode.

The configuration remains valid until a new input word with EN = 1 (the first three bits are 101 for the first word) and EN2 = 1 (for the second write byte) is shifted into the device.

Table 4. Converter Configuration

1	0	EN	SGL	ODD	A2	A1	A0	EN2	IM	FA	FB	SPD	GS2	GS1	GS0	CONVERTER CONFIGURATION
1	0	0	Any Input Channel					X	X	X	X	X	X	X	X	Keep Previous
1	0	1						0	X	X	X	X	X	X	X	Keep Previous
1	0	1						1	0	Any Rejection Mode		0	0	0	0	External Input, Gain = 1, Auto-Calibration
1	0	1						1	0			0	0	0	1	External Input, Gain = 4, Auto-Calibration
1	0	1						1	0			0	0	1	0	External Input, Gain = 8, Auto-Calibration
1	0	1						1	0			0	0	1	1	External Input, Gain = 16, Auto-Calibration
1	0	1						1	0			0	1	0	0	External Input, Gain = 32, Auto-Calibration
1	0	1						1	0			0	1	0	1	External Input, Gain = 64, Auto-Calibration
1	0	1						1	0			0	1	1	0	External Input, Gain = 128, Auto-Calibration
1	0	1						1	0			0	1	1	1	External Input, Gain = 264, Auto-Calibration
1	0	1						1	0			1	0	0	0	External Input, Gain = 1, 2x Speed
1	0	1						1	0			1	0	0	1	External Input, Gain = 2, 2x Speed
1	0	1						1	0			1	0	1	0	External Input, Gain = 4, 2x Speed
1	0	1						1	0			1	0	1	1	External Input, Gain = 8, 2x Speed
1	0	1						1	0			1	1	0	0	External Input, Gain = 16, 2x Speed
1	0	1						1	0			1	1	0	1	External Input, Gain = 32, 2x Speed
1	0	1						1	0			1	1	1	0	External Input, Gain = 64, 2x Speed
1	0	1						1	0			1	1	1	1	External Input, Gain = 128, 2x Speed
1	0	1						1	0	0	0	Any Speed	Any Gain			External Input, Simultaneous 50Hz/60Hz Rejection
1	0	1						1	0	0	1					External Input, 50Hz Rejection
1	0	1						1	0	1	0					External Input, 60Hz Rejection
1	0	1						1	0	1	1					Reserved, Do Not Use
1	0	1						1	1	0	0	X	X	X	X	Temperature Input, Simultaneous 50Hz/60Hz Rejection
1	0	1						1	1	0	1	X	X	X	X	Temperature Input, 50Hz Rejection
1	0	1						1	1	1	0	X	X	X	X	Temperature Input, 60Hz Rejection
1	0	1						1	1	1	1	X	X	X	X	Reserved, Do Not Use

256

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage ($\overline{CS}$, f_O, SDI)	2.7V ≤ V_{CC} ≤ 5.5V (Note 18)	●	V_{CC} – 0.5			V
V_{IL}	Low Level Input Voltage ($\overline{CS}$, f_O, SDI)	2.7V ≤ V_{CC} ≤ 5.5V	●			0.5	V
V_{IH}	High Level Input Voltage (SCK)	2.7V ≤ V_{CC} ≤ 5.5V (Notes 10, 15)	●	V_{CC} – 0.5			V
V_{IL}	Low Level Input Voltage (SCK)	2.7V ≤ V_{CC} ≤ 5.5V (Notes 10, 15)	●			0.5	V
I_{IN}	Digital Input Current ($\overline{CS}$, f_O, SDI)	0V ≤ V_{IN} ≤ V_{CC}	●	–10		10	µA
I_{IN}	Digital Input Current (SCK)	0V ≤ V_{IN} ≤ V_{CC} (Notes 10, 15)	●	–10		10	µA
C_{IN}	Digital Input Capacitance ($\overline{CS}$, f_O, SDI)				10		pF
C_{IN}	Digital Input Capacitance (SCK)	(Notes 10, 17)			10		pF
V_{OH}	High Level Output Voltage (SDO)	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage (SDO)	I_O = 1.6mA	●			0.4	V
V_{OH}	High Level Output Voltage (SCK)	I_O = –800µA (Notes 10, 17)	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage (SCK)	I_O = 1.6mA (Notes 10, 17)	●			0.4	V
I_{OZ}	Hi-Z Output Leakage (SDO)		●	–10		10	µA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current	Conversion Current (Note 12) Sleep Mode (Note 12)	● ●		160 1	275 2	µA µA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10		1000 ~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV}	Conversion Time	Simultaneous 50/60Hz External Oscillator	●	144.1	146.9 41036/f_{EOSC} (in kHz)	149.9	ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)			38.4 f_{EOSC} /8		kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 10)	●			4000	kHz
t_{LESCK}	External SCK Low Period	(Note 10)	●	125			ns
t_{HESCK}	External SCK High Period	(Note 10)	●	125			ns
t_{DOUT_ISCK}	Internal SCK 24-Bit Data Output Time	Internal Oscillator External Oscillator	●	0.61	0.625 192/f_{EOSC} (in kHz)	0.64	ms ms
t_{DOUT_ESCK}	External SCK 24-Bit Data Output Time	(Note 10)			24/f_{ESCK} (in kHz)		ms

The LTC2496 input measurement range is -0.5*VREF to +0.5*VREF in both differential and single-ended configurations as shown in Figure 29. Highest linearity is achieved with Fully Differential drive and a constant common-mode voltage (Figure 29b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

APPLICATIONS INFORMATION

front end. A proprietary front end passive sampling network transparently removes the differential input current. This enables external RC networks and high impedance sensors to directly interface to the LTC2496 without external amplifiers. The remaining common mode input current is eliminated by either balancing the differential input impedances or setting the common mode input equal to the common mode reference (see Automatic Differential Input Current Cancellation Section). This unique architecture does not require on-chip buffers thereby enabling signals to swing beyond ground or up to V_{CC}. Moreover, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full-scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2496 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2V. This feature guarantees the integrity of the conversion result, input channel selection, and serial clock mode.

When V_{CC} rises above this threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channel IN^+ = CH0, IN^- = CH1. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel, can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$)

The LTC2496 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front end circuits. Since the transition noise is well below 1LSB (0.02LSB), a decrease in reference voltage will proportionally improve the converter's effective resolution and improve the INL.

Input Voltage Range

The analog input is truly differential with an absolute, common mode range for CH0 to CH15 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD projection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2496 converts the bipolar differential input signal $V_{IN} = IN^+ + IN^-$ (where IN^+ and IN^- are the selected input channels), from $-FS = -0.5 \bullet V_{REF}$ to $+FS = 0.5 \bullet V_{REF}$ where $V_{REF} = REF^+ – REF^-$. Outside this range, the converter indicates the over range or the under range condition using distinct output codes.

Signals applied to the input (CH0 to CH15, COM) may extend 300mV below ground and above V_{CC}. In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

MUXOUT/ADCIN

The output of the multiplexer (MUXOUT) and the input to the ADC (ADCIN) can be used to perform input signal conditioning on any of the selected input channels or simply shorted together for direct digitization. If an external amplifier is used, the LTC2496 automatically calibrates both the offset and drift of this circuit and the Easy Drive sampling scheme enables a wide variety of amplifiers to be used.

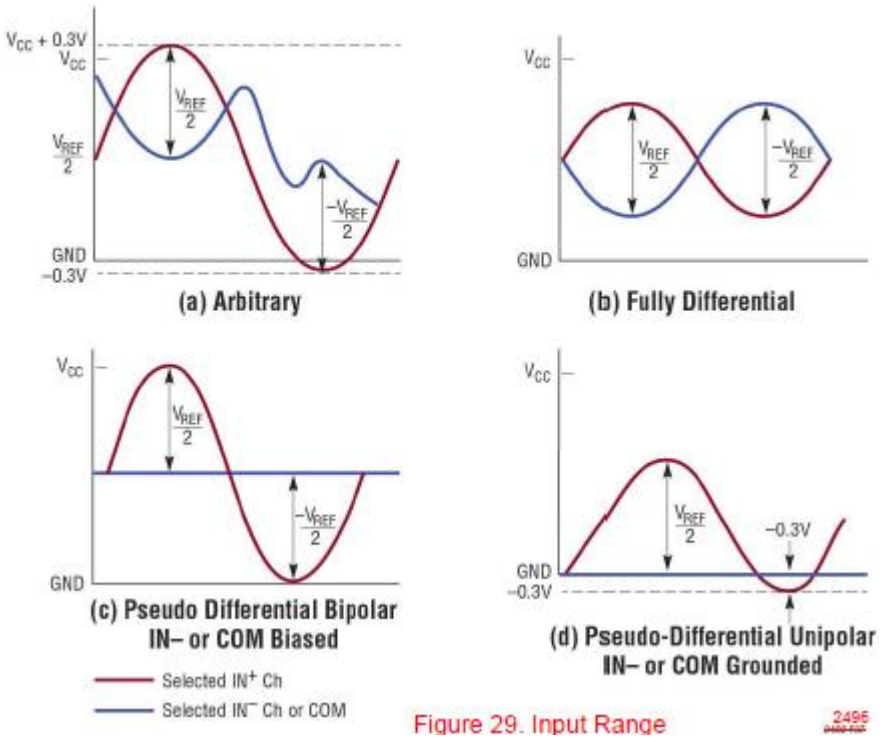

Figure 29. Input Range

2495

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10		1000 ~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV}	Conversion Time	Internal Oscillator External Oscillator (Note 10)	●	144.1	146.9 41036/f_{EOSC} (in kHz)	149.9	ms ms

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3, 15)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(SDA)}$	Hold Time (Repeated) Start Condition		●	0.6			µs
t_{LOW}	Low Period of the SCL Pin		●	1.3			µs
t_{HIGH}	High Period of the SCL Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated Start Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for SDA Signals	(Note 14)	●	20 + 0.1C_B		300	ns
t_f	Fall Time for SDA Signals	(Note 14)	●	20 + 0.1C_B		300	ns
$t_{SU(STO)}$	Set-Up Time for Stop Condition		●	0.6			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified.

$V_{REFCM} = V_{REF}/2$, $F_S = 0.5V_{REF}$

$V_{IN} = IN^+ – IN^–$, $V_{IN(CM)} = (IN^+ – IN^–)/2$,
where IN^+ and $IN^–$ are the selected input channels.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 11: The converter uses its internal oscillator.

Note 12: The output noise includes the contribution of the internal calibration operations.

Note 13: Guaranteed by design and test correlation.

Note 14: C_B = capacitance of one bus line in pF (10pF ≤ C_B ≤ 400pF).

Note 15: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 16: Refer to Applications Information section for performance versus data rate graphs.

The LTC2497 input measurement range is -0.5*VREF to +0.5*VREF in both differential and single-ended configurations as shown in Figure 28. Highest linearity is achieved with Fully Differential drive and a constant common-mode voltage (Figure 28b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

APPLICATIONS INFORMATION

common mode reference (see the Automatic Differential Input Current Cancellation section). This unique architecture does not require on-chip buffers, thereby enabling signals to swing beyond ground and V_{CC}. Moreover, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2497 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2.0V. This feature guarantees the integrity of the conversion result and input channel selection.

When V_{CC} rises above this threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channel IN^+ = CH0, IN^- = CH1. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential, external reference voltage. The absolute/common mode voltage range for REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$).

The LTC2497 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front end circuits. Since the transition noise is well below 1LSB (0.02LSB), a decrease in reference voltage will proportionally improve the converter resolution and improve INL.

Input Voltage Range

The analog inputs are truly differential with an absolute, common mode range for the CH0-CH15 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Within these limits, the LTC2497 converts the bipolar differential input signal $V_{IN} = IN^+ – IN^-$ (where IN^+ and IN^- are the selected input channels), from – FS = – 0.5 • V_{REF} to + FS = 0.5 • V_{REF} where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes (see Table 1).

Signals applied to the input (CH0-CH15, COM) may extend 300mV below ground and above V_{CC}. In order to limit any fault current due to input ESD leakage current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

MUXOUT/ADCIN

The outputs of the multiplexer (MUXOUTP/MUXOUTN) and the inputs to the ADC (ADCINP/ADCINN) can be used to perform input signal conditioning on any of the selected input channels or simply shorted together for direct digitization. If an external amplifier is used, the LTC2497 automatically calibrates both the offset and drift of this circuit and the Easy Drive sampling scheme enables a wide variety of amplifiers to be used.

In order to achieve optimum performance, if an external amplifier is not used, short these pins directly together (ADCINP to MUXOUTP and ADCINN to MUXOUTN) and minimize their capacitance to ground.

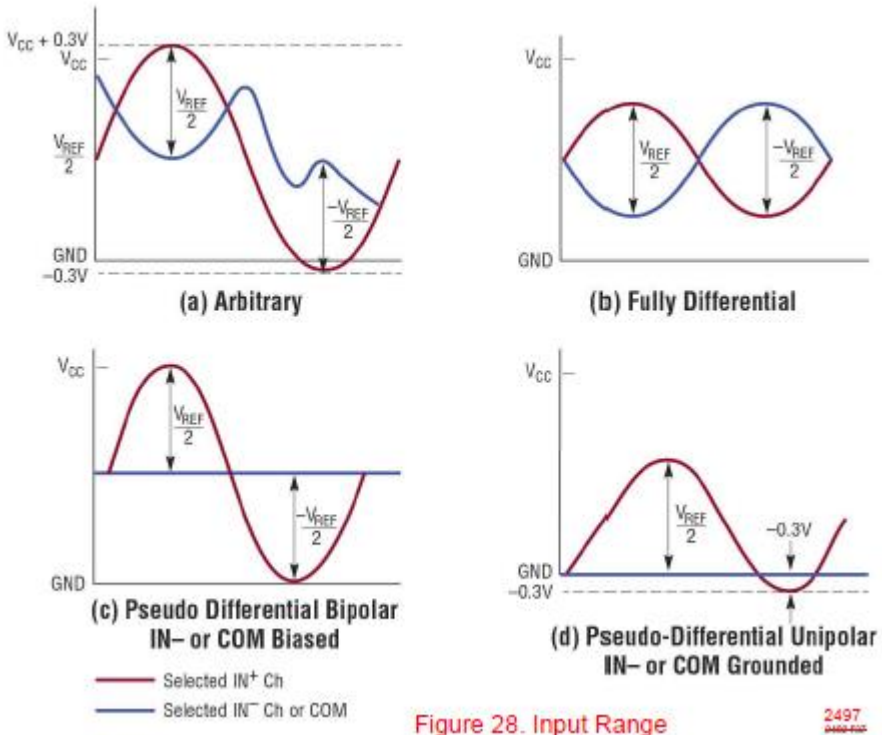

Figure 28. Input Range

2497

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10		1000 ~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		50	µs
t_{LEO}	External Oscillator Low Period		●	0.125		50	µs
t_{CONV_1}	Conversion Time for 1x Speed Mode	50Hz Mode 60Hz Mode Simultaneous 50/60Hz Mode External Oscillator	● ● ●	157.2 131 144.1	160.3 133.6 146.9 41036/f_{EOSC} (in kHz)	163.5 136.3 149.9	ms ms ms ms
t_{CONV_2}	Conversion Time for 2x Speed Mode	50Hz Mode 60Hz Mode Simultaneous 50/60Hz Mode External Oscillator	● ● ●	78.7 65.6 72.2	80.3 66.9 73.6 20556/f_{EOSC} (in kHz)	81.9 68.2 75.1	ms ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)			38.4 f_{EOSC}/8		kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 10)	●			4000	kHz
t_{LESCK}	External SCK LOW Period	(Note 10)	●	125			ns
t_{HESCK}	External SCK High Period	(Note 10)	●	125			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator External Oscillator	●	0.81	0.83 256/f_{EOSC} (in kHz)	0.85	ms ms
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 10)			32/f_{ESCK} (in kHz)		ms
t_1	$\overline{CS}$↓ to SDO Low		●	0		200	ns
t_2	$\overline{CS}$↑ to SDO Hi-Z		●	0		200	ns
t_3	$\overline{CS}$↓ to SCK↑	Internal SCK Mode	●	0		200	ns
t_4	$\overline{CS}$↓ to SCK↑	External SCK Mode	●	50			ns
t_{KQMAX}	SCK↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$↓		●			50	ns
t_7	SDI Setup Before SCK↑	(Note 5)	●	100			ns
t_8	SDI Hold After SCK↑	(Note 5)	●	100			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified.
$V_{REFCM} = V_{REF}/2$, $F_S = 0.5V_{REF}$
$V_{IN} = IN^+ - IN^-$, $V_{IN(CM)} = (IN^+ + IN^-)/2$,
where IN^+ and IN^- are the selected input channels.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless other wise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The SCK can be configured in external SCK mode or internal SCK mode. In external SCK mode, the SCK pin is used as a digital input and the driving clock is f_{ESCK}. In the internal SCK mode, the SCK pin is used as a digital output and the output clock signal during the data output is f_{ISCK}.

Note 11: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses its internal oscillator.

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: Guaranteed by design and test correlation.

Note 15: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

Note 16: Refer to Applications Information section for performance vs data rate graphs.

Note 17: The converter is in internal SCK mode of operation such that the SCK pin is used as a digital output.

Note 18: For V_{CC} < 3V, V_{IH} is 2.5V for Pin f_O.

The LTC2498 input measurement range is -0.5*VREF to +0.5*VREF in both differential and single-ended configurations as shown in Figure 39. Highest linearity is achieved with Fully Differential drive and a constant common-mode voltage (Figure 39b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

APPLICATIONS INFORMATION

enables external RC networks and high impedance sensors to directly interface to the LTC2498 without external amplifiers. The remaining common mode input current is eliminated by either balancing the differential input impedances or setting the common mode input equal to the common mode reference (see the Automatic Differential Input Current Cancellation section). This unique architecture does not require on-chip buffers thereby enabling signals to swing beyond ground or up to V_{CC}. Moreover, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full-scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2498 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2V. This feature guarantees the integrity of the conversion result, input channel selection, and serial clock mode.

When V_{CC} rises above this threshold, the converter creates an internal power-on reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channel IN^+ = CH0, IN^- = CH1, simultaneous 50Hz/60Hz rejection and 1x output rate. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel, rejection mode, speed mode, or temperature selection can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$)

The LTC2498 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front end circuits, and as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a decreased reference will improve the converter's overall INL performance.

Input Voltage Range

The analog input is truly differential with an absolute, common mode range for CH0 to CH15 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD projection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2498 converts the bipolar differential input signal $V_{IN} = IN^+ - IN^-$ (where IN^+ and IN^- are the selected input channels), from –FS = –0.5 • V_{REF} to +FS = 0.5 • V_{REF} where $V_{REF} = REF^+ – REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes.

Signals applied to the input (CH0 to CH15, COM) may extend 300mV below ground and above V_{CC}. In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

MUXOUT/ADCIN

The output of the multiplexer (MUXOUT) and the input to the ADC (ADCIN) can be used to perform input signal conditioning on any of the selected input channels or simply shorted together for direct digitization. If an external amplifier is used, the LTC2498 automatically calibrates both the offset and drift of this circuit and the Easy Drive sampling scheme enables a wide variety of amplifiers to be used.

In order to achieve optimum performance, if an external amplifier is not used, short these pins directly together (ADCINP to MUXOUTP and ADCINN to MUXOUTN) and minimize their capacitance to ground.

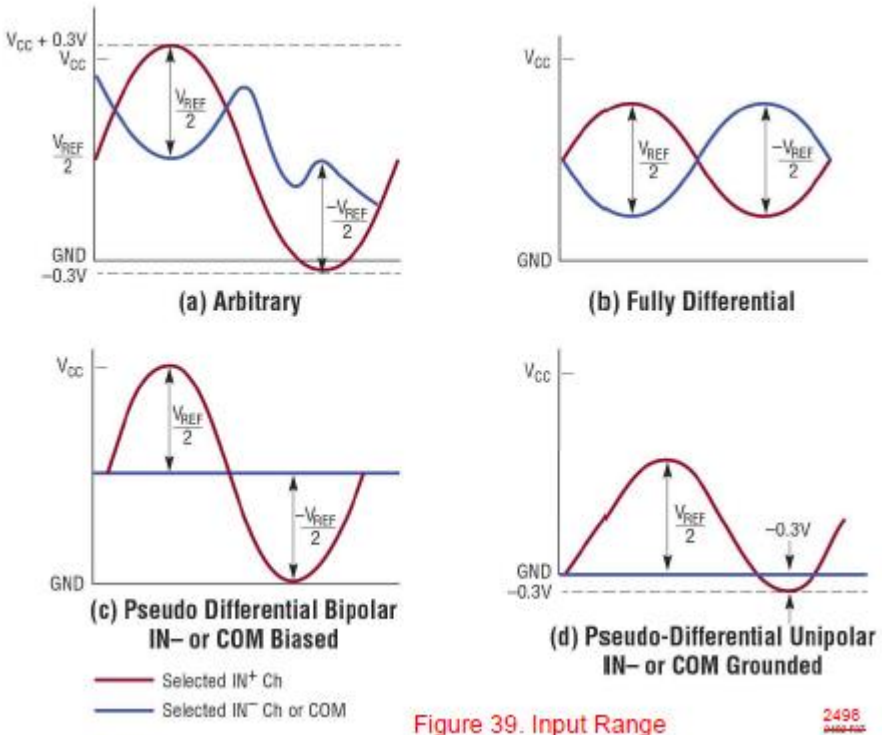

Figure 39. Input Range

2496

APPLICATIONS INFORMATION

Table 2. Output Data Format

Differential Input Voltage V_{IN}*	Bit 31 $\overline{EOC}$	Bit 30 DMY	Bit 29 SIG	Bit 28 MSB	Bit 27	Bit 26	Bit 25	...	Bit 0
V_{IN}* ≥ 0.5 • V_{REF}**	0	0	1	1	0	0	0	...	0
0.5 • V_{REF}** – 1LSB	0	0	1	0	1	1	1	...	1
0.25 • V_{REF}**	0	0	1	0	1	0	0	...	0
0.25 • V_{REF}** – 1LSB	0	0	1/0***	0	0	1	1	...	1
0	0	0	1	0	0	0	0	...	0
–1LSB	0	0	0	1	1	1	1	...	1
–0.25 • V_{REF}**	0	0	0	1	1	0	0	...	0
–0.25 • V_{REF}** – 1LSB	0	0	0	1	0	1	1	...	1
–0.5 • V_{REF}**	0	0	0	1	0	0	0	...	0
V_{IN}* < –0.5 • V_{REF}**	0	0	0	0	1	1	1	...	1 X ****

*The differential input voltage V_{IN} = IN+ – IN–. **The differential reference voltage V_{REF} = REF+ – REF–.

***The sign bit changes state during the 0 output code when the device is operating in the 2x speed mode.

****The underrange code is 0x0FFFFXXX in 2x mode

INPUT DATA FORMAT

The LTC2498 serial input word is 13 bits long and contains two distinct sets of data. The first set (SGL, ODD, A2, A1, A0) is used to select the input channel. The second set of data (IM, FA, FB, SPD) is used to select the frequency rejection, speed mode (1x, 2x), and temperature measurement.

After power-up, the device initiates an internal reset cycle which sets the input channel to CH0 – CH1 (IN^+ = CH0, IN^- = CH1), the frequency rejection to simultaneous 50Hz/60Hz, and 1x output rate (auto-calibration enabled). The first conversion automatically begins at power-up using this default configuration. Once the conversion is complete, a new word may be written into the device.

The first 3 bits shifted into the device consist of two preenable bits and one enable bit. As demonstrated in Figure 3, the first three bits shifted into the device enable the device configuration and input channel selection. Valid settings for these three bits are 000, 100 and 101. Other combinations should be avoided. If the first three bits are 000 or 100, the following data is ignored (don't care) and the previously selected input channel and configuration remain valid for the next conversion.

If the first 3 bits shifted into the device are 101, then the next 5 bits select the input channel for the next conversion cycle, see Table 3.

The first input bit following the 101 sequence (SGL) determines if the input selection is differential (SGL = 0) or single-ended (SGL = 1). For SGL = 0, two adjacent channels can be selected to form a differential input. For SGL = 1, one of 16 channels is selected as the positive input. The negative input is COM for all single ended operations. The remaining 4 bits (ODD, A2, A1, A0) determine which channel(s) is/are selected and the polarity (for a differential input).

The next serial input bit immediately following the input channel selection is the enable bit for the conversion configuration (EN2). If this bit is set to 0, then the next conversion is performed using the previously selected converter configuration. This is useful in systems using the same rejection/speed for all input channels and for backward compatibility with the LTC2418/LTC2414 families of delta sigma ADCs.

A new configuration can be loaded into the device by setting EN2 = 1, see Table 4. The first bit (IM) is used to select the internal temperature sensor. If IM = 1, the following conversion will be performed on the internal temperature sensor rather than the selected input channel. The next 2 bits (FA and FB) are used to set the rejection frequency. The final bit (SPD) is used to select either the 1x output rate if SPD = 0 (auto-calibration is enabled and the offset is continuously calibrated and removed from

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10		1000 ~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV_1}	Conversion Time for 1x Speed Mode	50Hz Mode	●	157.2	160.3	163.5	ms
		60Hz Mode	●	131	133.6	136.3	ms
		Simultaneous 50Hz/60Hz Mode	●	144.1	146.9	149.9	ms
		External Oscillator (Note 10)			41036/f_{EOSC} (in kHz)		ms
t_{CONV_2}	Conversion Time for 2x Speed Mode	50Hz Mode	●	78.7	80.3	81.9	ms
		60Hz Mode	●	65.6	66.9	68.2	ms
		Simultaneous 50Hz/60Hz Mode	●	72.2	73.6	75.1	ms
		External Oscillator (Note 10)			20556/f_{EOSC} (in kHz)		ms

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3, 15)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(SDA)}$	Hold Time (Repeated) START Condition		●	0.6			µs
t_{LOW}	LOW Period of the SCL Pin		●	1.3			µs
t_{HIGH}	HIGH Period of the SCL Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated START Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for SDA Signals	(Note 14)	●	20 + 0.1C_B		300	ns
t_f	Fall Time for SDA Signals	(Note 14)	●	20 + 0.1C_B		300	ns
$t_{SU(STO)}$	Set-Up Time for STOP Condition		●	0.6			µs
t_{BUF}	Bus Free Time Between a Second START Condition		●	1.3			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: Unless otherwise specified: V_{CC} = 2.7V to 5.5V

$V_{REFCM} = V_{REF}/2$, $F_S = 0.5V_{REF}$

$V_{IN} = IN^+ – IN^–$, $V_{IN(CM)} = (IN^+ – IN^–)/2$,

where IN^+ and $IN^–$ are the selected input channels.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 11: The converter uses its internal oscillator.

Note 12: The output noise includes the contribution of the internal calibration operations.

Note 13: Guaranteed by design and test correlation.

Note 14: C_B = capacitance of one bus line in pF (10pF ≤ C_B ≤ 400pF).

Note 15: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 16: Refer to Applications Information section for Performance vs Data Rate graphs.

The LTC2499 input measurement range is -0.5*VREF to +0.5*VREF in both differential and single-ended configurations as shown in Figure 38. Highest linearity is achieved with Fully Differential drive and a constant common-mode voltage (Figure 38b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

APPLICATIONS INFORMATION

cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2499 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2.0V. This feature guarantees the integrity of the conversion result and input channel selection.

When V_{CC} rises above this threshold, the converter creates an internal power-on reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channel IN^+ = CH0, IN^- = CH1 with simultaneous 50Hz/60Hz rejection and 1x output rate. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel, rejection mode, speed mode, or temperature selection can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$).

The LTC2499 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front-end circuits and, as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a decreased reference will improve the converter's overall INL performance.

Input Voltage Range

The analog inputs are truly differential with an absolute, common mode range for the CH0-CH15 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2499 converts the bipolar differential input signal $V_{IN} = IN^+ – IN^-$ (where IN^+ and IN^- are the selected input channels), from – FS = – 0.5 • V_{REF} to + FS = 0.5 • V_{REF} where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes (see Table 1).

Signals applied to the input (CH0-CH15, COM) may extend 300mV below ground and above V_{CC}. In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

MUXOUT/ADCIN

The outputs of the multiplexer (MUXOUTP/MUXOUTN) and the inputs to the ADC (ADCINP/ADCINN) can be used to perform input signal conditioning on any of the selected input channels or simply shorted together for direct digitization. If an external amplifier is used, the LTC2499 automatically calibrates both the offset and drift of this circuit and the Easy Drive sampling scheme enables a wide variety of amplifiers to be used.

In order to achieve optimum performance, if an external amplifier is not used, short these pins directly together (ADCINP to MUXOUTP and ADCINN to MUXOUTN) and minimize their capacitance to ground.

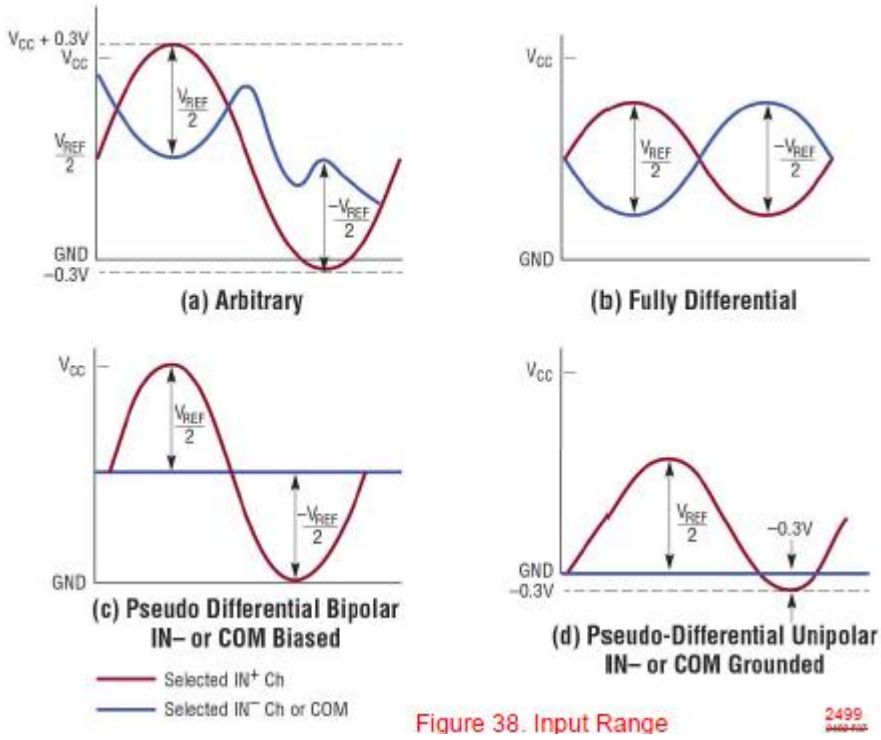

Figure 38. Input Range

2499

APPLICATIONS INFORMATION

matches the hard wired LTC2499's address (one of 27 pin-selectable addresses) the device is selected. When the device is addressed during the conversion state, it will not acknowledge R/W requests and will issue a NACK by leaving the SDA line HIGH. If the conversion is complete, the LTC2499 issues an ACK by pulling the SDA line LOW.

The LTC2499 has two registers. The output register (32 bits long) contains the last conversion result. The input register (16 bits long) sets the input channel, selects the temperature sensor, rejection mode, and speed mode.

DATA OUTPUT FORMAT

The output register contains the last conversion result. After each conversion is completed, the device automatically enters the sleep state where the supply current is reduced to 1µA. When the LTC2499 is addressed for a read operation, it acknowledges (by pulling SDA LOW) and acts as a transmitter. The master/receiver can read up to four bytes from the LTC2499. After a complete read operation (4 bytes), a new conversion is initiated. The device will NACK subsequent read operations while a conversion is being performed.

The data output stream is 32 bits long and is shifted out on the falling edges of SCL (see Figure 3a). The first bit is the conversion result sign bit (SIG) (see Tables 1 and 2). This bit is HIGH if $V_{IN} \geq 0$ and LOW if $V_{IN} < 0$ (where V_{IN} corresponds to the selected input signal $IN^+ - IN^-$). The second bit is the most significant bit (MSB) of the result. The first two bits (SIG and MSB) can be used to indicate over and under range conditions (see Table 2). If both bits are HIGH, the differential input voltage is equal to or above +FS. If both bits are set LOW, the input voltage is below –FS. The function of these bits is summarized in Table 2. The 24 bits following the MSB bit are the conversion result in binary two's, complement format. The remaining six bits are sub LSBs below the 24-bit level.

As long as the voltage on the selected input channels (IN^+ and IN^-) remains between –0.3V and V_{CC} + 0.3V (absolute maximum operating range) a conversion result is generated for any differential input voltage V_{IN} from –FS = –0.5 • V_{REF} to +FS = 0.5 • V_{REF}. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to +FS. For differential input voltages below –FS, the conversion result is clamped to the value –FS – 1LSB.

Table 1. Output Data Format

DIFFERENTIAL INPUT VOLTAGE V_{IN}*	BIT 31 SIG	BIT 30 MSB	BIT 29	BIT 28	BIT 27	...	BIT 6 LSB	BITs 5-0 Sub LSBs
V_{IN}* ≥ FS**	1	1	0	0	0	...	0	00000
FS** – 1LSB	1	0	1	1	1	...	1	XXXXX
0.5 • FS**	1	0	1	0	0	...	0	XXXXX
0.5 • FS** – 1LSB	1	0	0	1	1	...	1	XXXXX
0	1/0†	0	0	0	0	...	0	XXXXX
–1LSB	0	1	1	1	1	...	1	XXXXX
–0.5 • FS**	0	1	1	0	0	...	0	XXXXX
–0.5 • FS** – 1LSB	0	1	0	1	1	...	1	XXXXX
–FS**	0	1	0	0	0	...	0	XXXXX
V_{IN}* < –FS**	0	0	1	1	1	...	~~1~~ X	~~11111~~ XXXXX ***

*The differential input voltage $V_{IN} = IN^+ - IN^-$.
**The full-scale voltage FS = 0.5 • V_{REF}. Sub LSBs are below the 24-bit level. They may be included in averaging, or discarded without loss of resolution.
†The sign bit changes state during the 0 output code when the device is operating in the 2x speed mode.

***The underrange code is 0x3FFFFXXX in 2x mode.