Virtex-6 FPGA CX75T, CX130T, CX195T, and CX240T Production Errata

EN149 (v1.3) May 8, 2013 **Errata Notification**

Introduction

Thank you for designing with the Xilinx Virtex®-6 family of devices. Although Xilinx has made every effort to ensure the highest possible quality, the devices listed in Table 1 are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in Table 1.

Table 1: **Devices Affected by These Errata**

Devices	XC6VCX75T	JTAG ID (Revision Code): 2, or later
	XC6VCX130T	JTAG ID (Revision Code): 2, or later
	XC6VCX195T	JTAG ID (Revision Code): 2, or later
	XC6VCX240T	JTAG ID (Revision Code): 2, or later
Packages	All	
Speed Grades	All	

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

MMCM

Restriction of Frequency Range for Bandwidth = HIGH or OPTIMIZED

When the Phase Frequency Detector (PFD) frequency (FIN/D) is lower than 135 MHz and the BANDWIDTH attribute of the MMCM is set to HIGH or OPTIMIZED, a phase error between MMCM output clocks can occur, making the output clock signals invalid. This condition can also cause the fractional output counter to fail.

The ISE® software v12.4 and later provides appropriate warnings for possible violations of this restriction.

The ISE software v12.4 and later correctly handles designs set to OPTIMIZED bandwidth for all valid PFD frequencies.

This issue will not be fixed in the devices listed in Table 1.

Work-around

PFD frequencies lower than 135 MHz must use LOW bandwidth mode to ensure correct operation. See Answer Record 38132 for more information.

Restriction of Clock Divider Values

The input clock divider (DIVCLK_DIVIDE) cannot have a value of 3 or 4 when the input clock frequency (F_{IN}) of the MMCM is above 315 MHz.

The ISE software v12.4 and later provides appropriate warnings for possible violations of this restriction.

This issue will not be fixed in the devices listed in Table 1.

Work-around

In all designs in which F_{IN} is above 315 MHz and DIVCLK_DIVIDE is set to 3 or 4, double the CLKFBOUT_MULT_F and DIVCLK_DIVIDE values. See Answer Record 38133 for more information.

Block RAM

Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode

When using the block RAM in True Dual Port (TDP) Read_First mode, Simple Dual Port (SDP) mode, or ECC mode with different clocks on ports A and B, the user must ensure certain addresses do not occur simultaneously on both ports when both ports are enabled and one port is being written to. Failure to observe this restriction can result in read and/or memory array corruption.

The description is found in the Conflict Avoidance section in v1.3.1 (or later) of UG363, *Virtex-6 FPGA Memory Resources User Guide*.

This description was originally added in UG363 (v1.1), published 9/16/09. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. The ISE v12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in the devices listed in Table 1.

Work-around

See Answer Record 34859.

GTX Transceivers

GTX Transceiver Initialization for Proper TXOUTCLK Functionality

TXOUTCLK can operate at an incorrect frequency or can remain in a static state when the TXPLL_DIVSEL_OUT attribute is set to 2 or 4 and the TXOUTCLK_CTRL attribute is set to "TXOUTCLKPCS", "TXOUTCLKPMA_DIV1", or "TXOUTCLKPMA_DIV2".

An updated reset sequence that ensures proper functionality is documented in version 2.4 of UG366, Virtex-6 *FPGA GTX Transceiver User Guide*. Also see Answer Record 35681 for more information.

RXRECCLK Static Operating Behavior

The RXRECCLK output port might operate at reduced frequency in buffer bypass mode if conditions (1) and (2) persist for more than 15,000 cumulative hours at 65°C Tj, 2,500 cumulative hours at 85°C Tj, or 800 cumulative hours at 100°C Tj:

1. Power has been applied to V_{CCINT}.
2. The device is in one of the following states:
   a. The FPGA is not configured
   b. The FPGA is configured, but the transceiver is uninstantiated
   c. The transceiver is instantiated, but no reference clock is toggling
   d. The transceiver is instantiated, but is held in reset or power-down

Work-around

Transceivers Uninstantiated in User Design but are Planned to be Used in the Future

For transceivers that are not instantiated in the user design but are planned to be used in the future, power must be applied to MGTAVCC, and the user design must be implemented using ISE v12.1 (or later) software for automatic insertion of the work-around circuit.

Transceivers Uninstantiated in User Design but are Not Planned to be Used in the Future

Automatic insertion of the work-around circuit can be disabled for uninstantiated transceivers that will not be used.

Transceivers Instantiated in User Design

Transceivers instantiated in user design do not require a work-around circuit if the reference clock is toggling and the transceiver is not held in reset or power-down.

See Answer Record 35055 for more information.

GTX Transceiver Delay Aligner

The GTX Transceiver Delay Aligner circuit is used when the TX Buffer and/or RX Elastic Buffer are bypassed.

The Transmitter Delay Aligner is no longer supported; additionally, the use model of the Receiver Delay Aligner must be changed.

Applications that use the TX Buffer and RX Elastic Buffer are not affected by this errata item.

Applications currently bypassing the TX Buffer and/or RX Elastic Buffer, including XAUI, RXAUI, CPRI, OBSAI, and PLBv46 RC/EP Bridge for PCI Express® IP cores and the Integrated Block for PCIe, must implement the following work-around.

Work-around

The TX Buffer and RX Elastic Buffer can still be bypassed using work-arounds described in Answer Record 39430 to maximize system margin.

Operational Guidelines

Design Software Requirements

The devices listed in Table 1, unless otherwise specified, require the following Xilinx development software installations.

- Xilinx ISE Design Suite 12.1 (or later).
- See Known Issues in Answer Record 32929.

Traceability

The XC6VCX130T is marked as shown in Figure 1. The other devices listed in Table 1 are marked similarly.

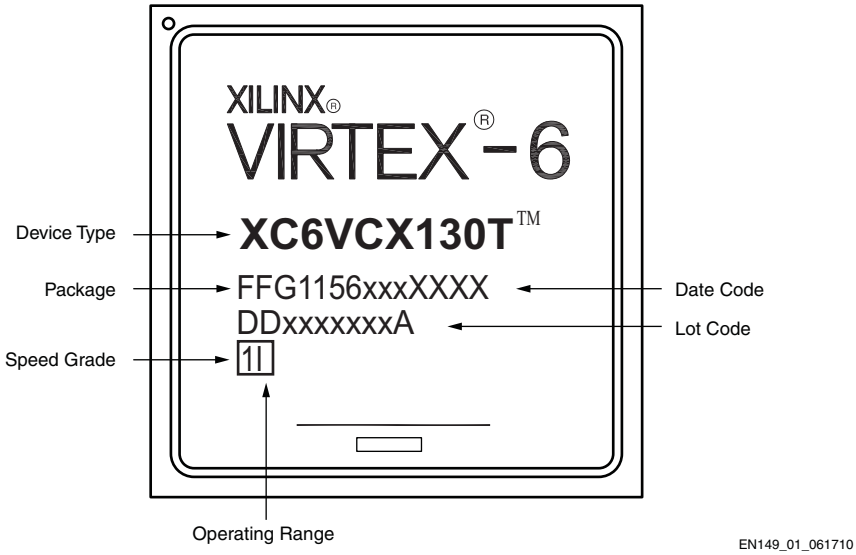

Figure 1: **Example Device Top Mark**

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Revision History

Date	Version	Description
06/18/10	1.0	Initial Xilinx release.
07/01/10	1.1	Added CX75T and CX195T devices. Removed System Monitor errata; it does not apply to the devices listed in Table 1.
01/17/11	1.2	Added Restriction of Frequency Range for Bandwidth = HIGH or OPTIMIZED and Restriction of Clock Divider Values. Updated TXOUTCLK and RXRECCLK Static Operating Behavior; no longer applicable to TXOUTCLK. Added GTX Transceiver Initialization for Proper TXOUTCLK Functionality. Added GTX Transceiver Delay Aligner per Xilinx Customer Notice XCN11009.
05/08/13	1.3	Updated JTAG ID (Revision Code) in Table 1.

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