



PSMN3R7-100BSE

N-channel 100 V, 3.95 mΩ, standard level MOSFET in D2PAK

3 September 2018

Product data sheet

1. General description

Standard level gate drive N-channel enhancement mode MOSFET in a D2PAK package qualified to 175 °C. Part of Nexperia's "NextPower Live" portfolio, the PSMN3R7-100BSE delivers very low $R_{DS(on)}$ and a very strong linear-mode (SOA) performance.

PSMN3R7-100BSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn on, low $R_{DS(on)}$ to minimize I^2R losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low $R_{DS(on)}$ for low I^2R conduction losses

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

4. Quick reference data

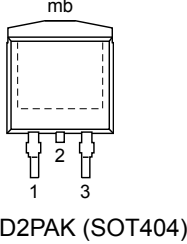
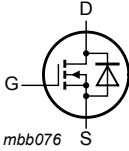
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	120	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	-	780	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	405	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	-	3.36	3.95	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 14 ; Fig. 15	-	45.2	77	nC
$Q_{G(tot)}$	total gate charge		-	176	246	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 4	-	-	542	mJ

[1] Continuous current is limited by package

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>D2PAK (SOT404)</p>	 <p>mbb076</p>
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2.

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN3R7-100BSE	D2PAK	plastic, single-ended surface-mounted package (D2PAK); 3 terminals (one lead cropped); 2.54 mm pitch; 11 mm x 10 mm x 4.3 mm body	SOT404

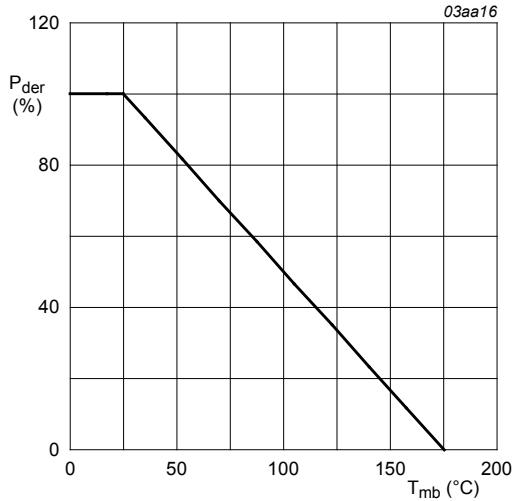
7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

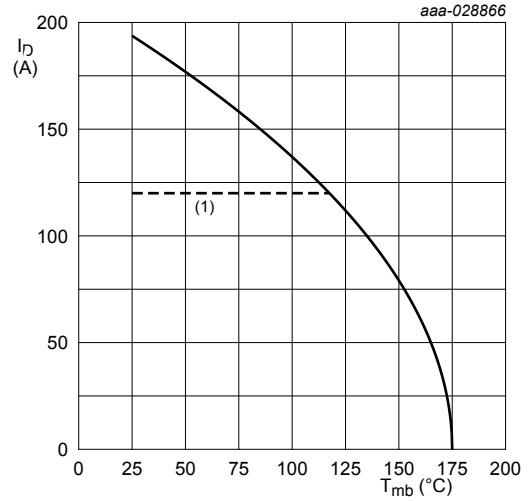
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	405	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	120	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	[1]	120	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	780	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	120	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	780	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 4	-	542	mJ

[1] Continuous current is limited by package



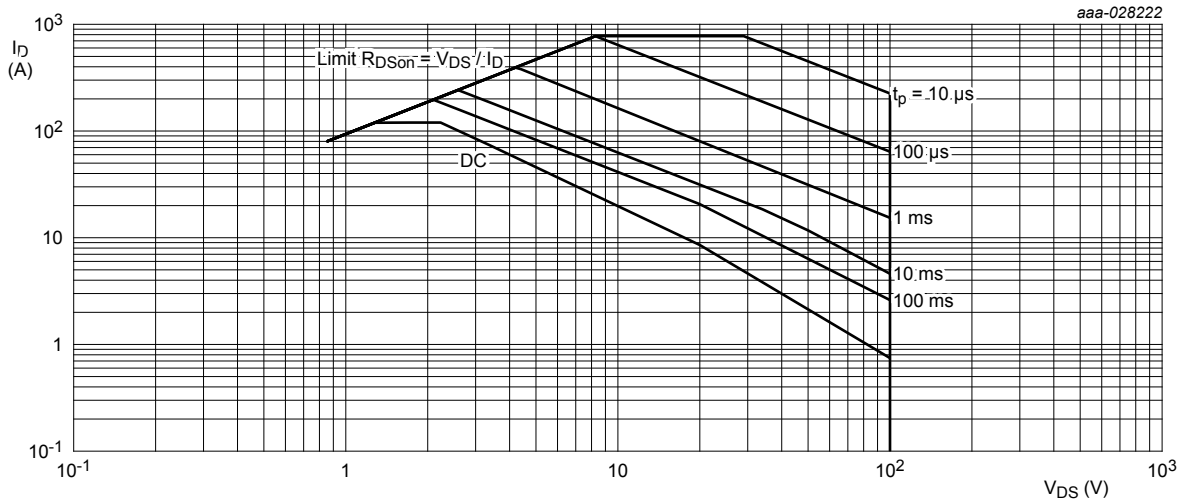
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



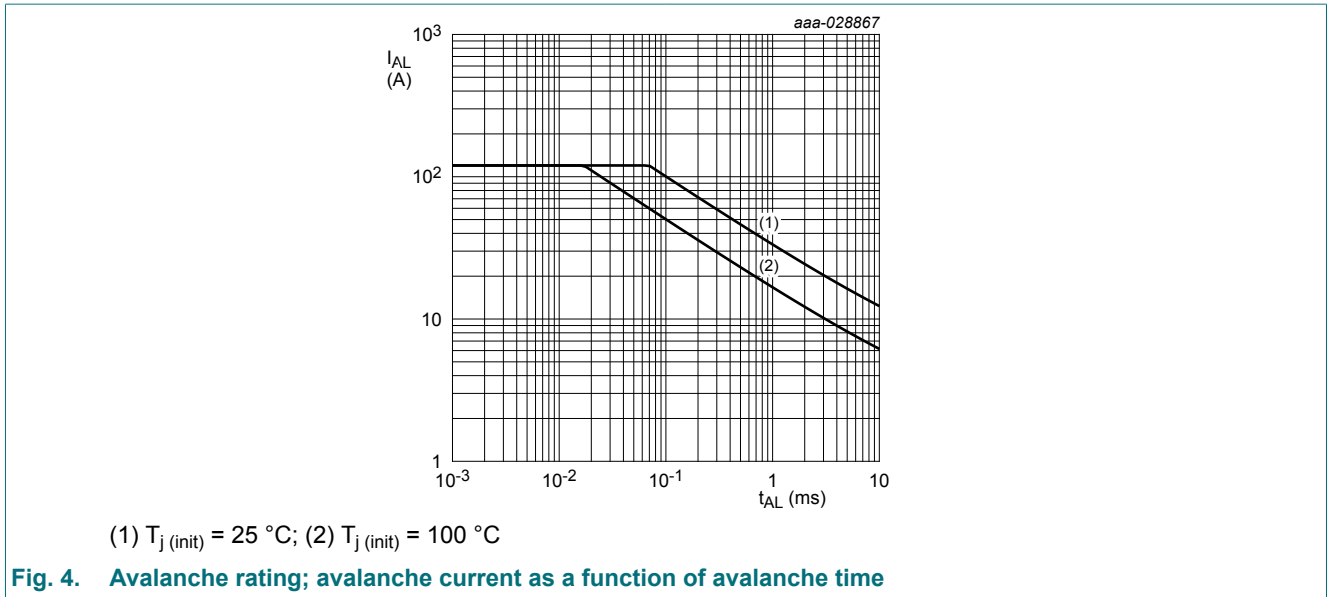
$V_{GS} \geq 10\text{ V}$
 (1) Capped at 120A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature



$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

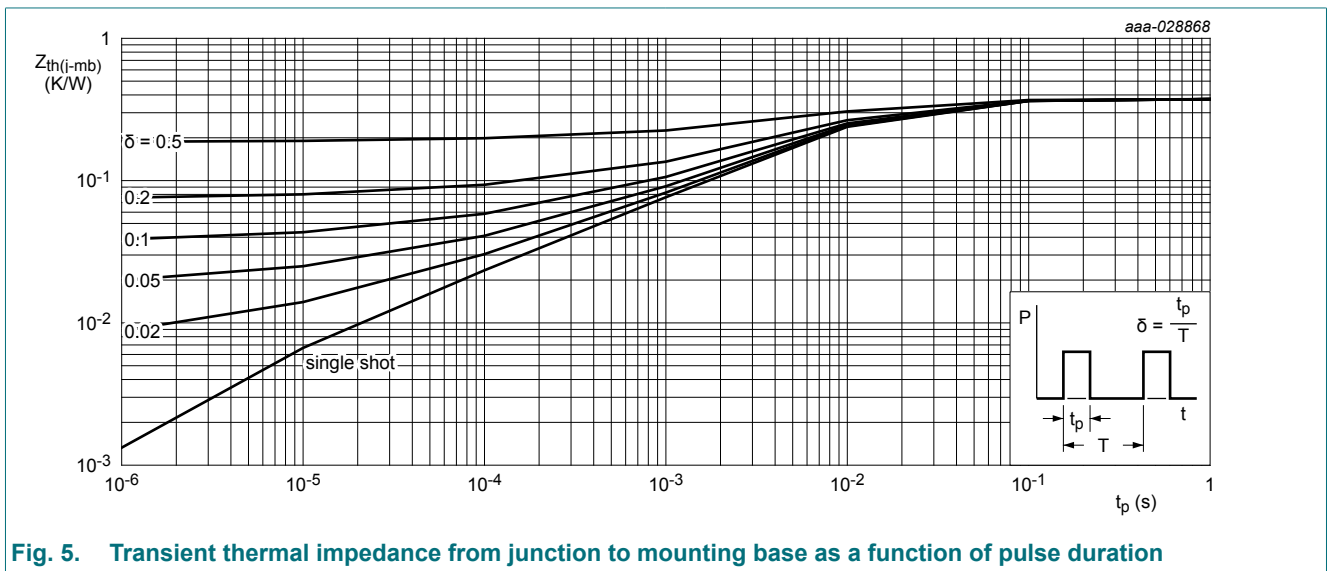
Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.3	0.37	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	50	-	K/W



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						

N-channel 100 V, 3.95 mΩ, standard level MOSFET in D2PAK

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$; Fig. 10 ; Fig. 11	2	2.66	4	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$; Fig. 11	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$; Fig. 11	-	-	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.026	2	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 12	-	3.36	3.95	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ C$; Fig. 13	-	-	7.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$; Fig. 13	-	-	10.7	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	0.49	0.98	1.96	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V}$; Fig. 14 ; Fig. 15	-	176	246	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	71	99	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V}$; Fig. 14 ; Fig. 15	-	49.5	74	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	30	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	19.7	-	nC
Q_{GD}	gate-drain charge		-	45.2	77	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}$; Fig. 14 ; Fig. 15	-	4.9	-	V
C_{iss}	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; Fig. 16	-	11692	16370	pF
C_{oss}	output capacitance		-	657	887	pF
C_{rss}	reverse transfer capacitance		-	353	494	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 2 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega$	-	40	60	ns
t_r	rise time		-	64	97	ns
$t_{d(off)}$	turn-off delay time		-	98	147	ns
t_f	fall time		-	69	104	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 17	-	0.79	1.2	V
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu s; V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V}$; Fig. 18	-	70	91	ns
Q_r	recovered charge		-	195	254	nC

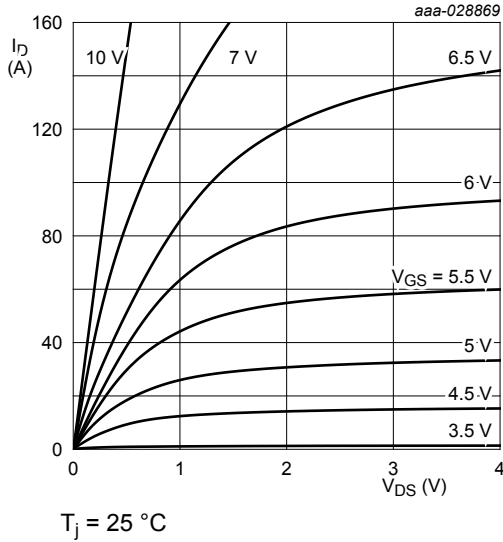


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

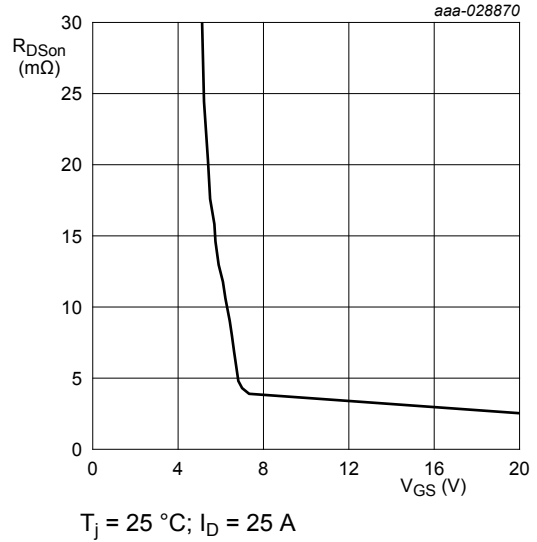


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

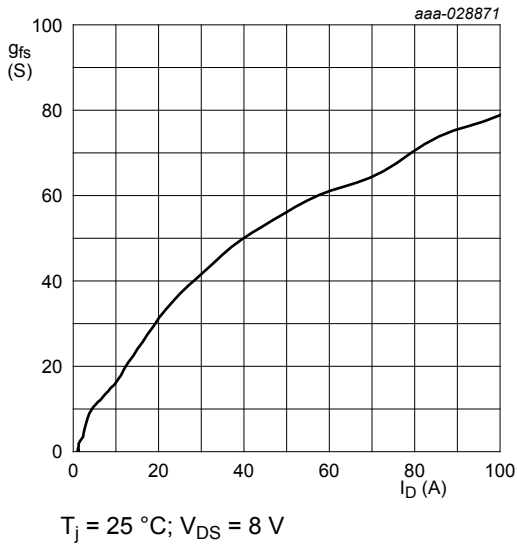


Fig. 8. Forward transconductance as a function of drain current; typical values

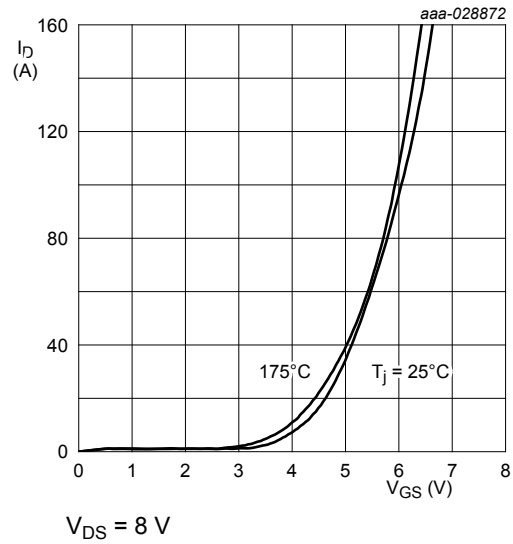


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

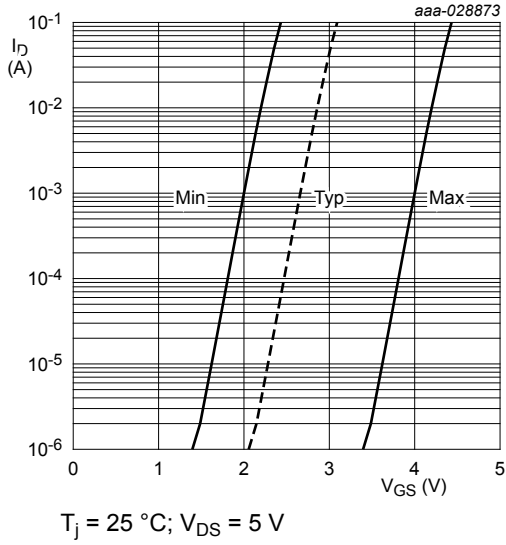


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

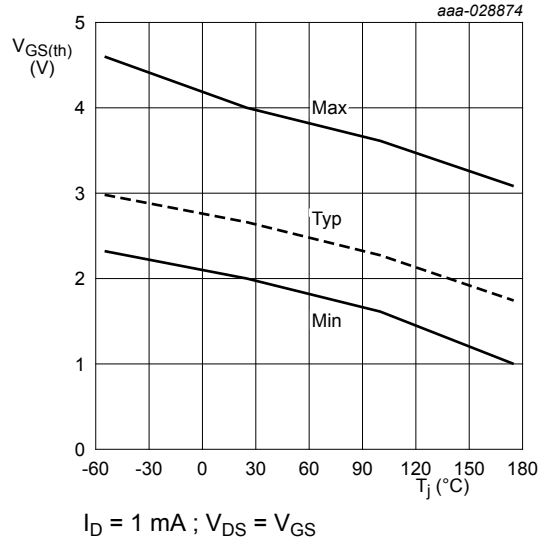


Fig. 11. Gate-source threshold voltage as a function of junction temperature

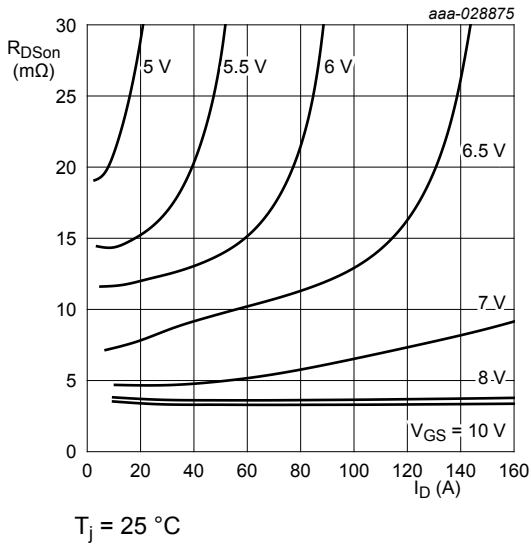


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

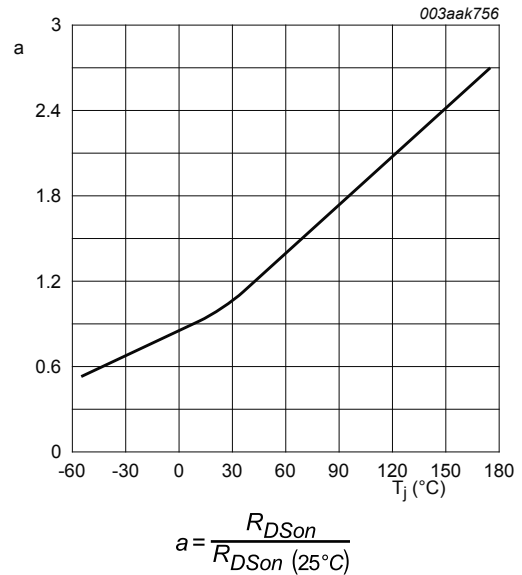


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

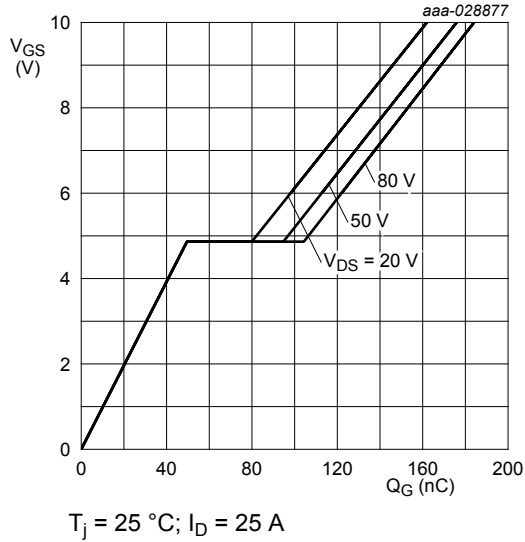


Fig. 14. Gate-source voltage as a function of gate charge; typical values

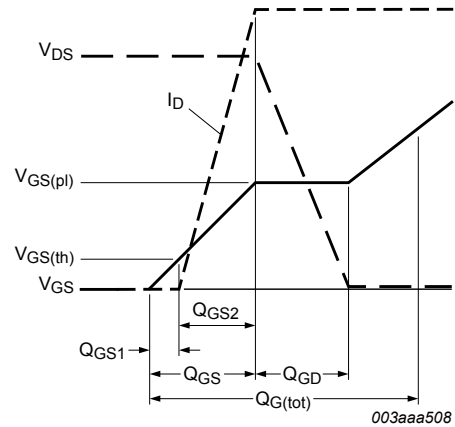


Fig. 15. Gate charge waveform definitions

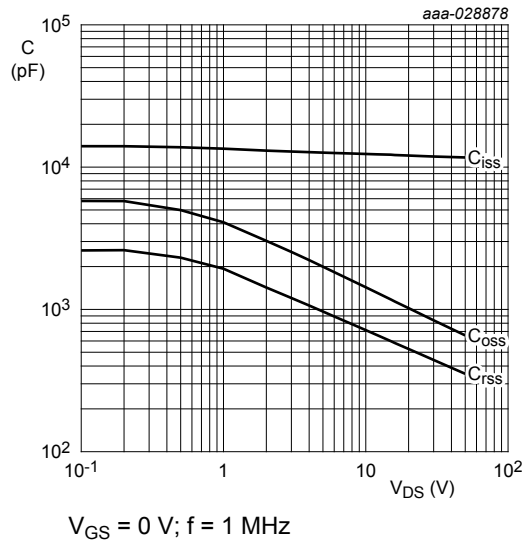


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

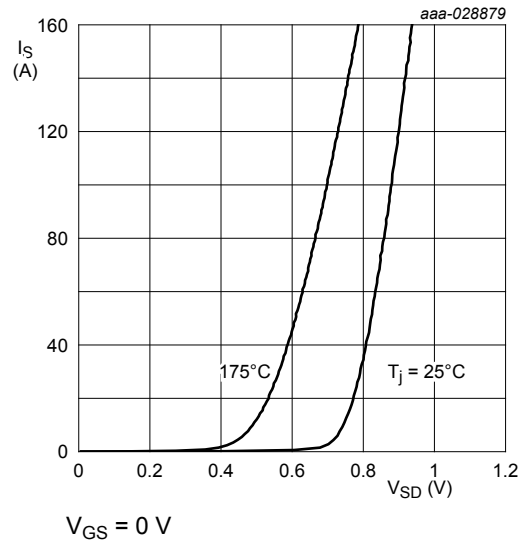


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

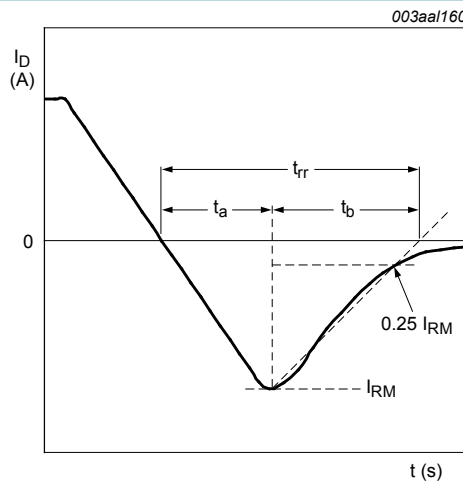


Fig. 18. Reverse recovery timing definition

10. Package outline

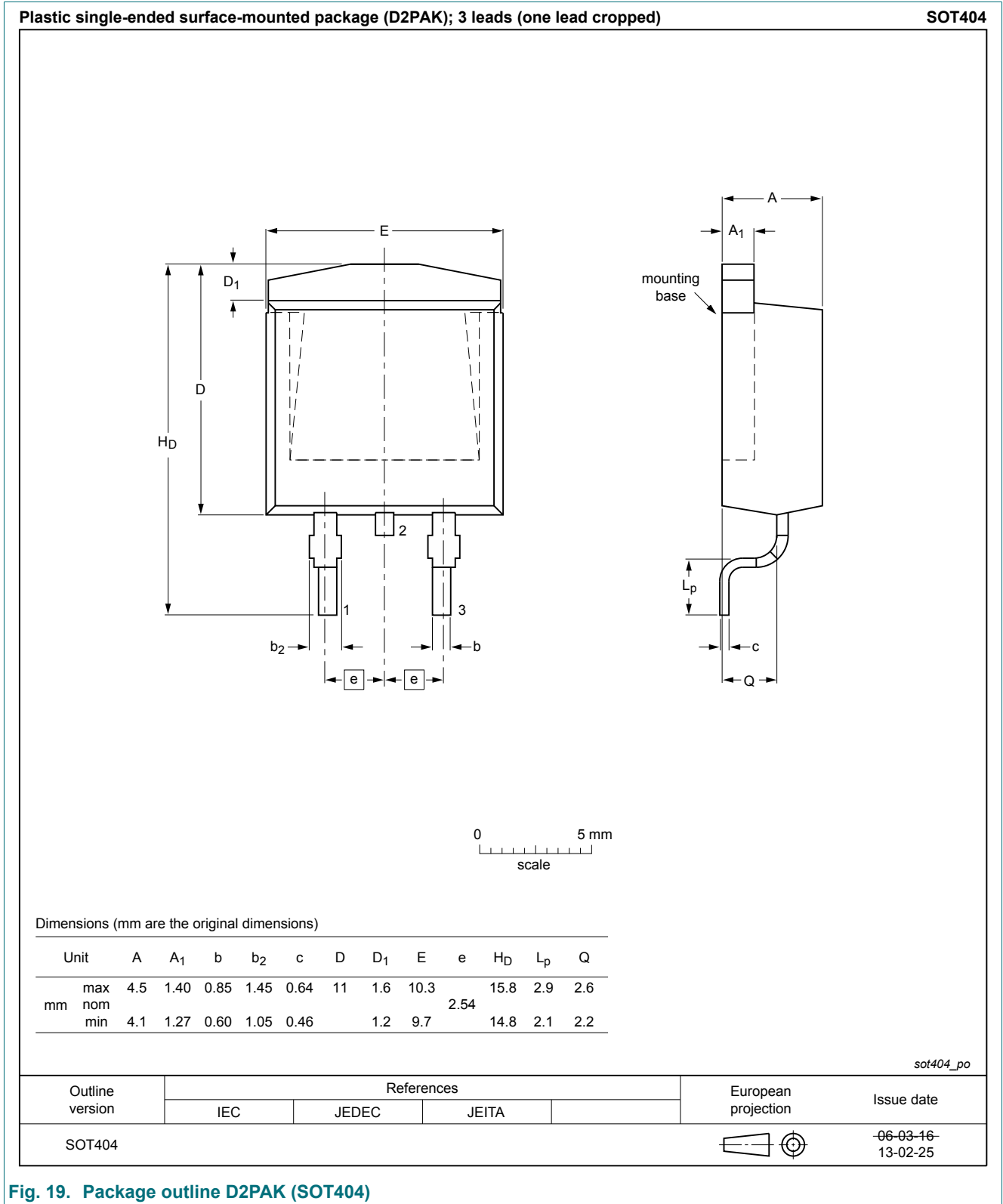


Fig. 19. Package outline D2PAK (SOT404)

11. Soldering

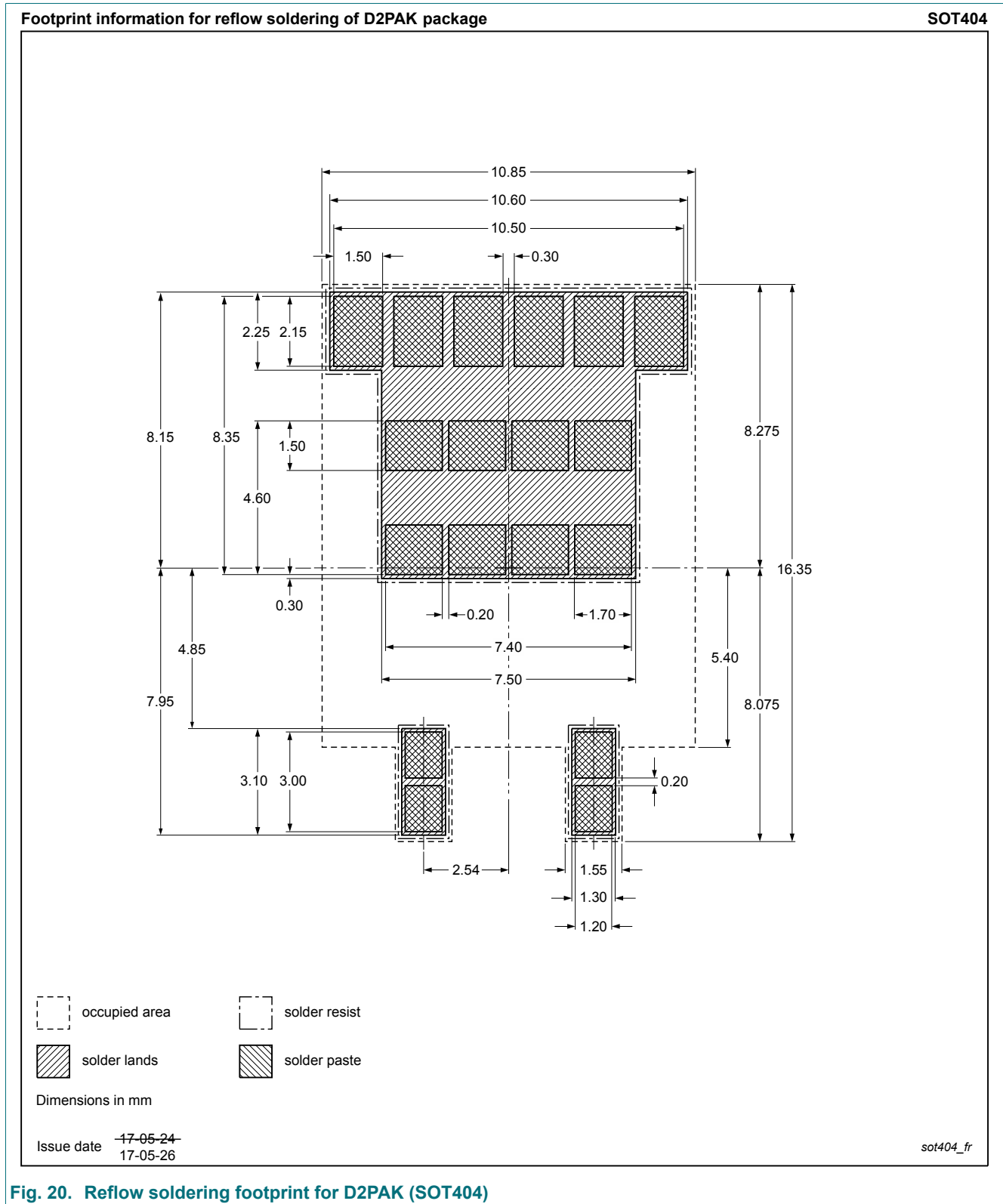


Fig. 20. Reflow soldering footprint for D2PAK (SOT404)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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