MICREL
The Infinite Bandwidth Company™

5V/3.3V ÷2, ÷4, ÷8 CLOCK GENERATION CHIP

ClockWorks™
SY10EL34/L
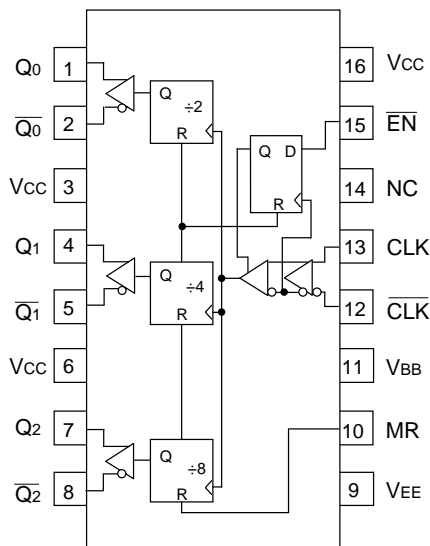**SY100EL34/L**
FINAL

FEATURES

- **3.3V and 5V power supply options**
- **50ps output-to-output skew**
- **Synchronous enable/disable**
- **Master Reset for synchronization**
- **Internal 75KΩ input pull-down resistors**
- **Available in 16-pin SOIC package**

PIN CONFIGURATION/BLOCK DIAGRAM

SOIC
TOP VIEW

DESCRIPTION

The SY10/100EL34/L are low skew ÷2, ÷4, ÷8 clock generation chips designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the V_{BB} output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01μF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EL34/L under single-ended input conditions. As a result, this pin can only source/ sink up to 0.5mA of current.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple EL34/Ls in a system.

PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
$\overline{EN}$	Synchronous Enable
MR	Master Reset
V_{BB}	Reference Output
Q_0	Differential ÷2 Outputs
Q_1	Differential ÷4 Outputs
Q_2	Differential ÷8 Outputs

TRUTH TABLE

CLK	EN	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q$_{0-2}$
X	X	H	Reset Q$_{0-2}$

NOTE:

Z = LOW-to-HIGH transition

ZZ = HIGH-to-LOW transition

DC ELECTRICAL CHARACTERISTICS[1]

V$_{EE}$ = V$_{EE}$ (Min.) to V$_{EE}$ (Max.); V$_{CC}$ = GND

Symbol	Parameter		T$_A$ = −40°C			T$_A$ = 0°C			T$_A$ = +25°C			T$_A$ = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I$_{EE}$	Power Supply 10EL	—	—	49	—	—	49	—	—	49	—	—	49	mA
	Current 100EL	—	—	49	—	—	49	—	—	49	—	—	54	
V$_{BB}$	Output Reference 10EL	−1.43	—	−1.30	−1.38	—	−1.27	−1.35	—	−1.25	−1.31	—	−1.19	V
	Voltage 100EL	−1.38	—	−1.26	−1.38	—	−1.26	−1.38	—	−1.26	−1.38	—	−1.26	
I$_{IH}$	Input High Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

NOTE:

1. Parametric values specified at: 5 volt Power Supply Range   100EL34 Series: -4.2V to -5.5V.

                                                      10EL34 Series   -4.75V to -5.5V.

   3 volt Power Supply Range   10/100EL34L Series: -3.0V to -3.8V.

AC ELECTRICAL CHARACTERISTICS[1]

V$_{EE}$ = V$_{EE}$ (Min.) to V$_{EE}$ (Max.); V$_{CC}$ = GND

Symbol	Parameter		T$_A$ = −40°C			T$_A$ = 0°C			T$_A$ = +25°C			T$_A$ = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t$_{PLH}$ t$_{PHL}$	Propagation Delay to Output CLK	960	1100	1200	960	1100	1200	960	1100	1200	960	1100	1200	ps
	MR	650	800	1010	650	800	1010	650	800	1010	650	800	1010	
t$_{skew}$	Within-Device Skew[2]	—	—	50	—	—	50	—	—	50	—	—	50	ps
t$_S$	Set-up Time EN	400	—	—	400	—	—	400	—	—	400	—	—	ps
t$_H$	Hold Time EN	200	—	—	200	—	—	200	—	—	200	—	—	ps
V$_{PP}$	Minimum Input Swing[3]	250	—	—	250	—	—	250	—	—	250	—	—	mV
V$_{CMR}$	Common Mode Range[4]	−1.3	—	−0.4	−1.4	—	−0.4	−1.4	—	−0.4	−1.4	—	−0.4	V
t$_r$ t$_f$	Output Rise/Fall Times Q (20% − 80%)	275	400	525	275	400	525	275	400	525	275	400	525	ps

NOTES:

1. Parametric values specified at: 5 volt Power Supply Range   100EL34 Series: -4.2V to -5.5V.

                                                      10EL34 Series   -4.75V to -5.5V.

                 3 volt Power Supply Range   10/100EL34L Series: -3.0V to -3.8V.

2. Skew is measured between outputs under identical transitions.

3. Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.

4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V$_{PP}$ min. and 1V. The lower end of the CMR range varies 1:1 with V$_{EE}$. The numbers in the spec table assume a nominal V$_{EE}$ = −3.3V. Note for PECL operation, the V$_{CMR}$ (min) will be fixed at 3.3V − |V$_{CMR}$ (min)|.

TIMING DIAGRAM
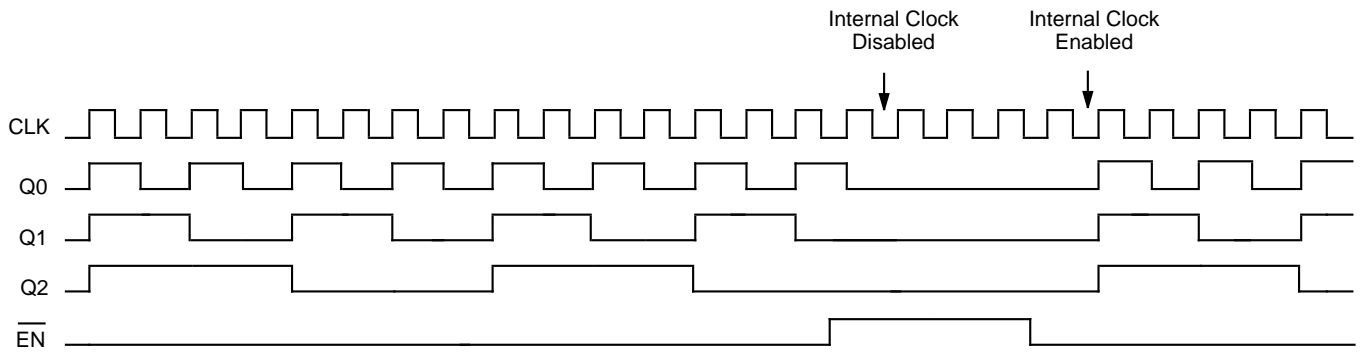
The $\overline{EN}$ signal will freeze the internal clocks to the flip-flops on the first falling edge of CLK after its assertion. The internal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time and relationship as they would have had the $\overline{EN}$ signal not been asserted.
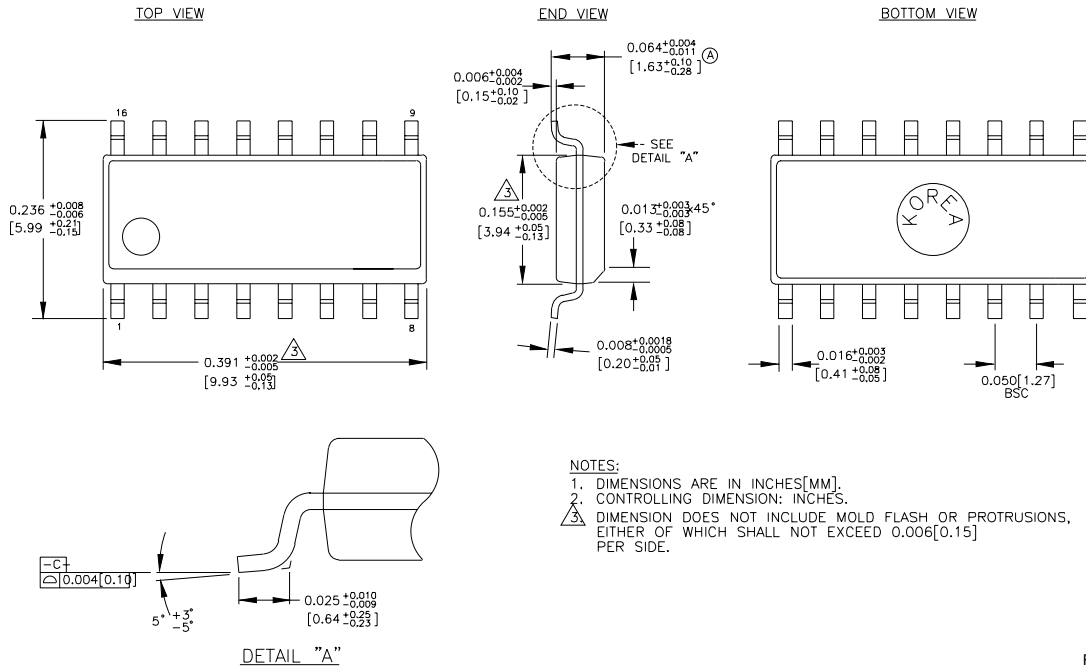
PRODUCT ORDERING CODE

3.3V

Ordering Code	Package Type	Operating Range	V$_{EE}$ Range (V)
SY10EL34LZC	Z16-2	Commercial	-3.0 to -3.8
SY10EL34LZCTR	Z16-2	Commercial	-3.0 to -3.8
SY100EL34LZC	Z16-2	Commercial	-3.0 to -3.8
SY100EL34LZCTR	Z16-2	Commercial	-3.0 to -3.8

5V

Ordering Code	Package Type	Operating Range	V$_{EE}$ Range (V)
SY10EL34ZC	Z16-2	Commercial	-4.75 to -5.5
SY10EL34ZCTR	Z16-2	Commercial	-4.75 to -5.5
SY100EL34ZC	Z16-2	Commercial	-4.2 to -5.5
SY100EL34ZCTR	Z16-2	Commercial	-4.2 to -5.5

16 LEAD SOIC .150" WIDE (Z16-2)

TOP VIEW

END VIEW

BOTTOM VIEW

$0.236 {}^{+0.008}_{-0.006}$
$[5.99 {}^{+0.21}_{-0.15}]$

$0.391 {}^{+0.002}_{-0.005}$
$[9.93 {}^{+0.05}_{-0.13}]$

$0.064 {}^{+0.004}_{-0.011}$ Ⓐ
$[1.63 {}^{+0.10}_{-0.28}]$

$0.006 {}^{+0.004}_{-0.002}$
$[0.15 {}^{+0.10}_{-0.02}]$

SEE DETAIL "A"

$0.155 {}^{+0.002}_{-0.005}$
$[3.94 {}^{+0.05}_{-0.13}]$

$0.013 {}^{+0.003}_{-0.003}$ × 45°
$[0.33 {}^{+0.08}_{-0.08}]$

$0.008 {}^{+0.0018}_{-0.0005}$
$[0.20 {}^{+0.05}_{-0.01}]$

$0.016 {}^{+0.003}_{-0.002}$
$[0.41 {}^{+0.08}_{-0.05}]$

0.050[1.27]
BSC

KOREA

NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.

−C−
⬡ 0.004[0.10]

5° ${}^{+3°}_{-5°}$

$0.025 {}^{+0.010}_{-0.009}$
$[0.64 {}^{+0.25}_{-0.23}]$

DETAIL "A"

Rev. 02