

FEATURES

- 3 MHz switch mode charger**
- 1.25 A charge current from dedicated charger**
- Up to 680 mA charging current from 500 mA USB host**
- Operating input voltage from 4.0 V up to 5.5 V**
- Tolerant input voltage -0.5 V to +20 V (USB VBUS)**
- Dead battery isolation FET between battery and charger output**
- Battery thermistor input with automatic charger shutdown for when battery temperature exceeds limits**
- Compliant with the JEITA Li-Ion battery charging temperature specification**
- SYS_EN_OK flag to hold off system turn-on until battery is at minimum required level for guaranteed system startup due to minimum battery voltage and/or minimum battery charge level requirements**
- EOC programming with C/20, C/10 and specific current level selection**

APPLICATIONS

- Digital still cameras**
- Digital video cameras**
- Single cell Li-Ion portable equipment**
- PDA, audio, GPS devices**
- Mobile phones**

GENERAL DESCRIPTION

The [ADP5065](#) charger is fully compliant with the USB 2.0, USB 3.0, and USB Battery Charging Specification 1.1 and enables charging via the mini USB VBUS pin from a wall charger, car charger, or USB host port.

The [ADP5065](#) operates from a 4 V to 5.5 V input voltage range but is tolerant of voltages of up to 20 V. This alleviates the concerns about the USB bus spiking during disconnect or connect scenarios.

The [ADP5065](#) also features an internal FET between the dc-to-dc charger output and the battery. This permits battery isolation and, hence, system powering under a dead battery or no battery scenario, which allows for immediate system function on connection to a USB power supply.

FUNCTIONAL BLOCK DIAGRAM

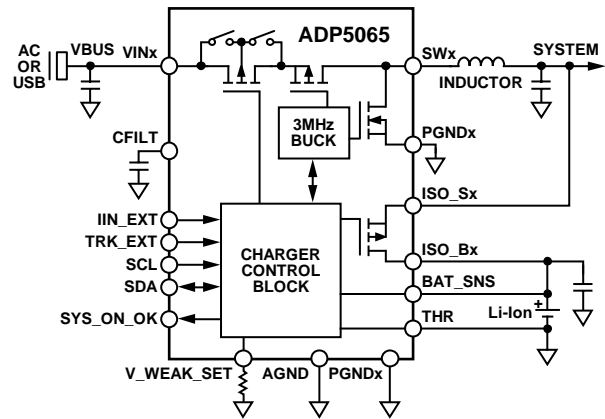


Figure 1.

09370-001

Based on the type of USB source, which is detected by an external USB detection chip, the [ADP5065](#) can be set to apply the correct current limit for optimal charging and USB compliance.

The [ADP5065](#) comes in a very small and low profile 20-lead WLCSP (0.5 mm pitch spacing) package.

The overall solution requires only five small, low profile external components consisting of four ceramic capacitors (one of which is the battery filter capacitor), one multilayer inductor. In addition to these components, there is one optional dead battery situation default setting resistor. This configuration enables a very small PCB area to provide an integrated and performance enhancing solution to USB battery charging and power rail provision.

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REVISION HISTORY

2/13—Rev. C to Rev. D

| | |
|--|----|
| Changed Maximum Duty Cycle from 93% to 96% | 3 |
| Changed Bit[3:0] Default Value from 0100 to 0101, Table 16 .. | 26 |
| Changed Bit 5 and Bit 2 Default Values from 1 to 0, Table 21 | 29 |
| Deleted Disconnecting Supply Voltage at VINx Section | 34 |

9/12—Rev. B to Rev. C

| | |
|--|----|
| Changed Bit[3:0] Default Value from 0011 to 0100, Table 16 | 27 |
| Added Disconnecting Supply Voltage at VINx Section | 34 |

4/12—Rev. A to Rev. B

| | |
|--|----|
| Changes to Features Section and General Description Section..... | 1 |
| Changes to Table 1..... | 3 |
| Changes to VIN1, VIN2 to PGND1, PGND2 Parameter, Table 4... 7 | 7 |
| Changes to Introduction Section..... | 15 |

11/11—Rev. 0 to Rev. A

| | |
|---|----|
| Changes to Figure 10..... | 10 |
| Changes to Figure 17 and Figure 18..... | 11 |
| Changes to Figure 41 | 36 |

10/11—Revision 0: Initial Version

SPECIFICATIONS

$-40^{\circ}\text{C} < T_j < 125^{\circ}\text{C}$, $V_{\text{IN}} = 5.0\text{ V}$, $V_{\text{ISO}_S} > 3.0\text{ V}$, $V_{\text{HOT}} < V_{\text{THR}} < V_{\text{COLD}}$, $V_{\text{BAT_SNS}} = 3.6\text{ V}$, $C_{\text{VIN}} = 2.2\text{ }\mu\text{F}$, $C_{\text{DCDC}} = 22\text{ }\mu\text{F}$, $C_{\text{BAT}} = 22\text{ }\mu\text{F}$, $C_{\text{CFILT}} = 4.7\text{ }\mu\text{F}$, $L_{\text{OUT}} = 1\text{ }\mu\text{H}$, all registers are at default values, unless otherwise noted.

Table 1.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-------------------------------|-------------------|---------------------------|--------------------|------------------|---|
| GENERAL PARAMETERS | | | | | | |
| Undervoltage Lockout | V_{UVLO} | 2.25 50 | 2.35 100 | 2.45 150 | V mV | Falling threshold, higher of V_{CFILT} and $V_{\text{BAT_SNS}}$ Hysteresis, higher of V_{CFILT} and $V_{\text{BAT_SNS}}$ rising |
| Total Input Current | I_{VIN} | 86 | 92 | 100 150 300 | mA mA mA | Nominal USB initialized current level ¹ USB super speed USB enumerated current level (specification for China) |
| Current Consumption | | 460 | 475 | 500 900 1500 | mA mA mA | USB enumerated current level Dedicated charger input Dedicated wall charger |
| VINx | I_{QVIN} | | 15 | | mA | No battery, no ISO_Sx load, switching 3 MHz |
| Battery, Standby | I_{QISO_B} | | 0.22 | 2 | μA | $T_j = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ |
| SWxPin Leakage Current | $-I_{\text{OUT}}$ | | | 2 | μA | $V_{\text{IN}} = 0\text{ V}$, $T_j = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ |
| CHARGING PARAMETERS | | | | | | |
| Fast Charge Current, CC Mode (Battery Voltage $> V_{\text{TRK_DEAD}}$) | I_{CHG} | | 1250 | | mA | $V_{\text{CFILT}} > V_{\text{BAT_SNS}} + V_{\text{CCDROP}}^{1,2}$ |
| Fast Charge Current Accuracy | $I_{\text{CHG(TOL)}}$ | -7 -8 | | +5 +8 | % % | $T_j = 25^{\circ}\text{C}$, $I_{\text{CHG}} = 550\text{ mA}$ to 1250 mA $I_{\text{CHG}} = 550\text{ mA}$ to 1150 mA , fast charge current accuracy is guaranteed at temperatures from $T_j = 0^{\circ}\text{C}$ to isothermal regulation limit (typically $T_j = 115^{\circ}\text{C}$) |
| Trickle Charge Current ^{1,2} | $I_{\text{TRK_DEAD}}$ | -17 | | +8 | % | $I_{\text{CHG}} = 1250\text{ mA}$, $T_j = 0^{\circ}\text{C}$ to isothermal regulation limit (typically $T_j = 115^{\circ}\text{C}$) |
| Weak Charge Current | $I_{\text{CHG_WEAK}}$ | | $I_{\text{CHG}} + 20$ | | mA | When $V_{\text{TRK_DEAD}} < V_{\text{BAT_SNS}} < V_{\text{WEAK}}^{1,3}$ |
| Dead Battery | | | | | | |
| Trickle to Weak Charge Threshold | $V_{\text{TRK_DEAD}}$ | 2.4 | 2.5 | 2.6 | V | On BAT_SNS^1 |
| Trickle to Weak Charge Threshold Hysteresis | $\Delta V_{\text{TRK_DEAD}}$ | | 90 | | mV | |
| Weak Battery | | | | | | |
| Weak to Fast Charge Threshold | V_{WEAK} | 2.9 | 3.0 | 3.1 | V | On $\text{BAT_SNS}^{1,3}$ |
| Weak Battery Threshold Hysteresis | ΔV_{WEAK} | | 90 | | mV | |
| Battery Termination Voltage | V_{TRM} | 4.158 | 4.200 | 4.242 | V | On BAT_SNS , $T_j = 0^{\circ}\text{C}$ to 115°C^1 |
| Battery Termination Voltage Accuracy | | -0.3 | | +0.3 | % | On BAT_SNS , $T_j = 25^{\circ}\text{C}$, $I_{\text{END}} = 52.5\text{ mA}^1$ |
| Battery Overvoltage Threshold | V_{BATOVS} | | $V_{\text{CFILT}} - 0.15$ | | V | Relative to CFILT voltage, BAT_SNS rising |
| Charge Complete Current | I_{END} | | 52.5 | | mA | $V_{\text{BAT_SNS}} = V_{\text{TRM}}^1$ |
| Charge Complete Current Threshold Accuracy | | -25 -35 -55 | | +25 +35 +55 | % % % | $I_{\text{END}} = 72.5\text{ mA}$ or 92.5 mA , $T_j = 0^{\circ}\text{C}$ to 115°C $I_{\text{END}} = 52.5\text{ mA}$, $T_j = 0^{\circ}\text{C}$ to 115°C $I_{\text{END}} = 32.5\text{ mA}$, $T_j = 0^{\circ}\text{C}$ to 115°C |
| Recharge Voltage Differential | V_{RCH} | | 260 | | mV | Relative to V_{TRM} , BAT_SNS falling ¹ |
| Battery Node Short Threshold Voltage ¹ | $V_{\text{BAT_SHR}}$ | 2.3 | 2.4 | 2.5 | V | |
| CHARGER DC-to-DC CONVERTER | | | | | | |
| Switching Frequency | f_{SWCHG} | 2.8 | 3 | 3.2 | MHz | |
| Maximum Duty Cycle | D_{MAX} | | 96 | | % | |
| Peak Inductor Current | $I_{\text{L(PK)}}$ | 1500 | 1750 | 2000 | mA | |
| Regulated System Voltage | $V_{\text{ISO_STRK}}$ | 3.21 | 3.3 | 3.39 | V | $V_{\text{BAT_SNS}} < V_{\text{TRK_DEAD}}$, trickle charging mode |
| Load Regulation | | | 5 | | mV/A | |
| DC-to-DC Power | | | | | | |
| PMOS On Resistance | $R_{\text{DS(ON)P}}$ | | 220 | 285 | $\text{m}\Omega$ | |
| NMOS On Resistance | $R_{\text{DS(ON)N}}$ | | 160 | 210 | $\text{m}\Omega$ | |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------------------------|--------|--------|--------|------|---|
| BATTERY ISOLATION FET | | | | | | |
| Bump to Bump Resistance Between ISO_Bx and ISO_Sx Bumps | R _{DSONISO} | | 76 | 115 | mΩ | Includes bump resistances and battery isolation PMOS on resistance; on battery supplement mode, V _{IN} = 0 V, V _{ISO_B} = 3.6 V, I _{ISO_B} = 500 mA V _{TRK_DEAD} < V _{BAT_SNS} , fast charging CC mode V _{ISO_S[1:2]} < V _{ISO_B[1:2]} , V _{SYS} rising |
| Regulated System Voltage | V _{ISO_SFC} | 3.15 | 3.3 | 3.45 | V | |
| Battery Supplementary Threshold | V _{THISO} | 0 | 5 | 10 | mV | |
| HIGH VOLTAGE BLOCKING FET | | | | | | |
| VINx Input | | | | | | |
| High Voltage Blocking FET On Resistance | R _{DSONHV} | | 340 | 455 | mΩ | I _{IN} = 500 mA |
| Current, Suspend Mode | I _{SUSPEND} | | 1.3 | 2.5 | mA | EN_CHG = low |
| Input Voltage | | | | | | |
| Good Threshold | | | | | | |
| Rising | V _{VIN_OK_RISE} | 3.78 | 3.9 | 4.0 | V | |
| Falling | V _{VIN_OK_FALL} | | 3.6 | 3.67 | V | |
| Overshoot Threshold | V _{VIN_OV} | 5.35 | 5.42 | 5.5 | V | |
| Overshoot Threshold Hysteresis | | | 75 | | mV | |
| VINx Transition Timing | | | | | | |
| Minimum Rise Time for VINx from 5 V to 20 V | t _{VIN_RISE} | 10 | | | μs | |
| Minimum Fall Time for VINx from 4 V to 0 V | t _{VIN_FALL} | 10 | | | μs | |
| THERMAL CONTROL | | | | | | |
| Isothermal Charging Temperature | T _{LIM} | | 115 | | °C | |
| Thermal Early Warning Temperature | T _{SDL} | | 130 | | °C | |
| Thermal Shutdown Temperature | T _{SD} | | 140 | | °C | T _J rising |
| | | | 110 | | °C | T _J falling |
| THERMISTOR CONTROL | | | | | | |
| Thermistor Current | | | | | | |
| 10,000 NTC | I _{NTC_10k} | | | 400 | μA | |
| 100,000 NTC | I _{NTC_100k} | | | 40 | μA | |
| Thermistor Capacitance | C _{NTC} | | | 100 | pF | |
| Cold Temperature Threshold | T _{NTC_COLD} | | 0 | | °C | No battery charging occurs |
| Resistance Thresholds | | | | | | |
| Cool to Cold Resistance | R _{COLD_FALL} | 24,050 | 27,300 | 30,600 | Ω | |
| Cold to Cool Resistance | R _{COLD_RISE} | 23,100 | 26,200 | 29,400 | Ω | |
| Hot Temperature Threshold | T _{NTC_HOT} | | 60 | | °C | No battery charging occurs |
| Resistance Thresholds | | | | | | |
| Hot to Typical Resistance | R _{HOT_FALL} | 2990 | 3310 | 3640 | Ω | |
| Typical to Hot Resistance | R _{HOT_RISE} | 2730 | 3030 | 3330 | Ω | |
| JEITA SPECIFICATION⁴ | | | | | | |
| JEITA Cold Temperature | T _{JEITA_COLD} | | 0 | | °C | No battery charging occurs |
| Resistance Thresholds | | | | | | |
| Cool to Cold Resistance | R _{COLD_FALL} | 24,050 | 27,300 | 30,600 | Ω | |
| Cold to Cool Resistance | R _{COLD_RISE} | 23,100 | 26,200 | 29,400 | Ω | |
| JEITA Cool Temperature | T _{JEITA_COOL} | | 10 | | °C | Battery charging occurs at 50% of programmed level |
| Resistance Thresholds | | | | | | |
| Typical to Cool Resistance | R _{TYP_FALL} | 15,200 | 17,800 | 20,400 | Ω | |
| Cool to Typical Resistance | R _{TYP_RISE} | 14,500 | 17,000 | 19,500 | Ω | |
| JEITA Typical Temperature | T _{JEITA_TYP} | | | | °C | Normal battery charging occurs at default/programmed levels |
| Resistance Thresholds | | | | | | |
| Warm to Typical Resistance | R _{WARM_FALL} | 4710 | 5400 | 6100 | Ω | |
| Typical to Warm Resistance | R _{WARM_RISE} | 4320 | 4950 | 5590 | Ω | |
| JEITA Warm Temperature | T _{JEITA_WARM} | | 45 | | °C | Battery termination voltage (V _{TRM}) is reduced by 100 mV |
| Resistance Thresholds | | | | | | |
| Hot to Warm Resistance | R _{HOT_FALL} | 2990 | 3310 | 3640 | Ω | |
| Warm to Hot Resistance | R _{HOT_RISE} | 2730 | 3030 | 3330 | Ω | |
| JEITA Hot Temperature | T _{JEITA_HOT} | | 60 | | °C | No battery charging occurs |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---------------------------------------|----------------------|-----|-----|-----|------|--|
| BATTERY DETECTION | | | | | | |
| Sink Current | I _{SINK} | 13 | 20 | 34 | mA | |
| Source Current | I _{SOURCE} | 7 | 10 | 13 | mA | |
| Battery Threshold | | | | | | |
| Low | V _{BATL} | 1.8 | 1.9 | 2.0 | V | |
| High | V _{BATH} | | 3.4 | | V | |
| No Battery Threshold | V _{NOBAT} | | 3.3 | | V | |
| | | | 3.0 | | V | V _{TRM} ≥ 3.7 V, valid after charge complete (see Figure 38) V _{TRM} < 3.7 V, valid after charge complete (see Figure 38) |
| Battery Detection Timer | t _{BATOK} | | 333 | | ms | |
| TIMERS | | | | | | |
| Start Charging Delay Timer | t _{START} | | 1 | | sec | |
| Trickle Charge Timer | t _{TRK} | | 60 | | min | |
| Fast Charge Timer | t _{CHG} | | 600 | | min | |
| Charge Complete Timer | t _{END} | | 7.5 | | min | |
| Deglintch Timer | t _{DG} | | 31 | | ms | |
| Watchdog Timer ¹ | t _{WD} | | 32 | | sec | |
| Safety Timer | t _{SAFE} | 36 | 40 | 44 | min | |
| Battery Node Short Timer ¹ | t _{BAT_SHR} | | 30 | | sec | |
| LOGIC INPUTS | | | | | | |
| Maximum Voltage on Digital Inputs | V _{DIN,MAX} | | | 5.5 | V | |
| Maximum Logic Low Input Voltage | V _{IL} | | | 0.5 | V | |
| Minimum Logic High Input Voltage | V _{IH} | 1.2 | | | V | |
| Pull-Down Resistance | | 215 | 350 | 610 | kΩ | |

¹ These values are programmable via I²C. Values are given with default register values.

² The output current during charging can be limited by I_{BUS} or by the isothermal charging mode.

³ Programmable via external resistor programming, if required.

⁴ JEITA can be enabled or disabled in I²C.

RECOMMENDED INPUT AND OUTPUT CAPACITANCE

Table 2.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--------------------------------------|-----|-----|-----|------|--------------------------|
| CAPACITANCE | | | | | |
| VINx Capacitance | 1.0 | | | μF | Effective capacitance |
| CFILT Pin Total External Capacitance | 2.0 | 4.7 | 5.0 | μF | Effective capacitance |
| ISO_Sx Pin Total Capacitance | 10 | | 50 | μF | Effective capacitance |
| ISO_Bx Pin Total Capacitance | 10 | | | μF | Effective capacitance |

I²C-COMPATIBLE INTERFACE TIMING SPECIFICATIONS

Table 3.

| Parameter ¹ | Symbol | Min | Typ | Max | Unit |
|--|--------------------|-----|-----|-----|------|
| I ² C-COMPATIBLE INTERFACE ² | | | | | |
| Capacitive Load, Each Bus Line | C _S | | | 400 | pF |
| SCL Clock Frequency | f _{SCL} | | | 400 | kHz |
| SCL High Time | t _{HIGH} | 0.6 | | | μs |
| SCL Low Time | t _{LOW} | 1.3 | | | μs |
| Data Setup Time | t _{SUDAT} | 100 | | | ns |
| Data Hold Time | t _{HDDAT} | 0 | | 0.9 | μs |
| Setup Time for Repeated Start | t _{SUSTA} | 0.6 | | | μs |
| Hold Time for Start/Repeated Start | t _{HDSTA} | 0.6 | | | μs |
| Bus Free Time Between a Stop and a Start Condition | t _{BUF} | 1.3 | | | μs |
| Setup Time for Stop Condition | t _{SUSTO} | 0.6 | | | μs |
| Rise Time of SCL/SDA | t _R | 20 | | 300 | ns |
| Fall Time of SCL/SDA | t _F | 20 | | 300 | ns |
| Pulse Width of Suppressed Spike | t _{SP} | 0 | | 50 | ns |

¹ Guaranteed by design.

² A master device must provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL. See Figure 2, the I²C timing diagram.

Timing Diagram

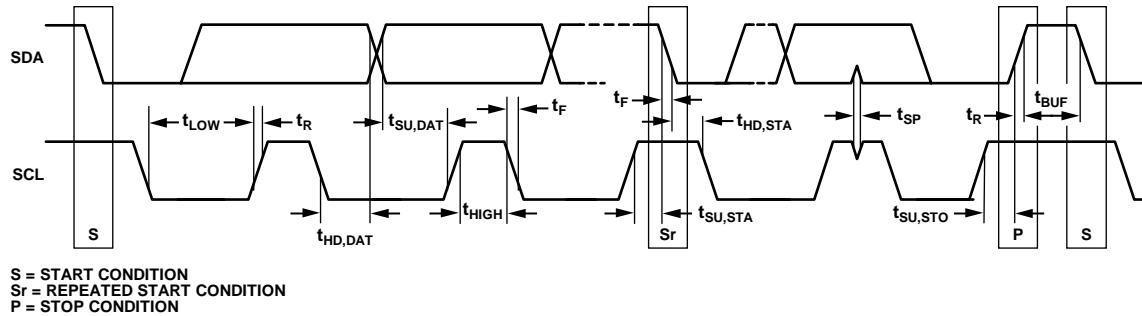


Figure 2. I²C Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

Table 4.

| Parameter | Rating |
|---|-----------------------------------|
| VIN1, VIN2 to PGND1, PGND2 All Other Pins to AGND | –0.5 V to +20 V –0.3 V to +6 V |
| Continuous Drain Current, Battery Supple- mentary Mode, from ISO_Bx to ISO_Sx T _J ≤ 85°C | 2.2 A |
| T _J = 125°C | 1.1 A |
| Storage Temperature Range | –65°C to +150°C |
| Operating Junction Temperature Range | –40°C to +125°C |
| Soldering Conditions | JEDEC J-STD-020 |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

| Package Type | θ_{JA} | θ_{JC} | θ_{JB} | Unit |
|----------------------------|---------------|---------------|---------------|------|
| 20-Lead WLCSP ¹ | 46.8 | 0.7 | 9.2 | °C/W |

¹ 5 × 4 array, 0.5 mm pitch (2.75 mm × 2.08 mm); based on a JEDEC, 2S2P, 4-layer board with 0 m/sec airflow.

Maximum Power Dissipation

The maximum safe power dissipation in the [ADP5065](#) package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the [ADP5065](#). Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices that potentially cause failure.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

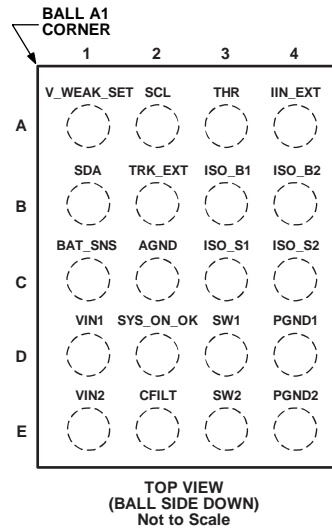


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

| Pin No. | Mnemonic | Type ¹ | Description |
|---------|----------------|-------------------|---|
| D3, E3 | SW1, SW2 | I/O | DC-to-DC Converter Inductor Connection. These pins are high current outputs when in charging mode. |
| D1, E1 | VIN1, VIN2 | I/O | Power Connection to USB VBUS. These pins are high current inputs when in charging mode. |
| D4, E4 | PGND1, PGND2 | G | Charger Power Ground. These pins are high current inputs when in charging mode. |
| C2 | AGND | G | Analog Ground. |
| E2 | CFILT | I/O | 4.7 μ F Filter Capacitor Connection. This pin is a high current input/output when in charging mode. |
| C3, C4 | ISO_S1, ISO_S2 | I/O | Charger Supply Side Input to Internal Isolation FET/Battery Current Regulation FET. |
| B3, B4 | ISO_B1, ISO_B2 | I/O | Battery Supply Side Input to Internal Isolation FET/Battery Current Regulation FET. |
| A2 | SCL | I | I ² C-Compatible Interface Serial Clock. |
| B1 | SDA | I/O | I ² C-Compatible Interface Serial Data. |
| A4 | IIN_EXT | I | Set Input Current Limit. This pin sets the input current limit directly. When IIN_EXT = low or high-Z, the input limit is 100 mA. When IIN_EXT = high, the input limit is 500 mA. |
| B2 | TRK_EXT | I | Enable Trickle Charge Function. When TRK_EXT = low or high-Z, the trickle charge is enabled. When TRK_EXT = high, the trickle charge is disabled. |
| A3 | THR | I | Battery Pack Thermistor Connection. If not used, connect a dummy 10 k Ω resistor from THR to GND. |
| C1 | BAT_SNS | I | Battery Voltage Sense Pin. |
| D2 | SYS_ON_OK | O | Battery Okay Open-Drain Output Flag. Active low. This pin enables the system when the battery reaches V _{WEAK} . |
| A1 | V_WEAK_SET | I/O | External Resistor Setting Pin for V_WEAK threshold. The use of this pin is optional. When not in use, connect to GND. |

¹ I is input, O is output, I/O is input/output, and G is ground.

TYPICAL PERFORMANCE CHARACTERISTICS

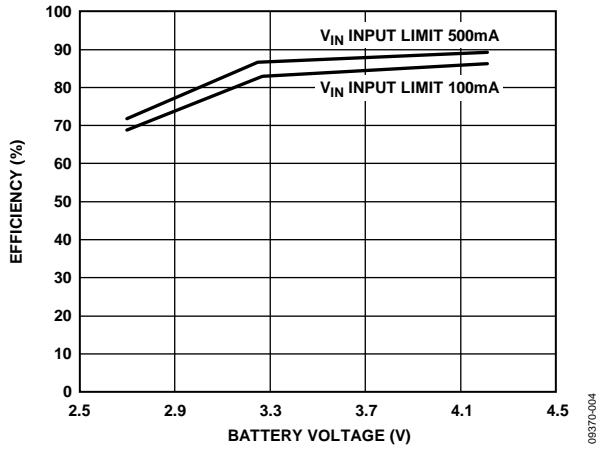


Figure 4. Battery Charger Efficiency vs. Battery Voltage, $V_{IN} = 5.0\text{ V}$

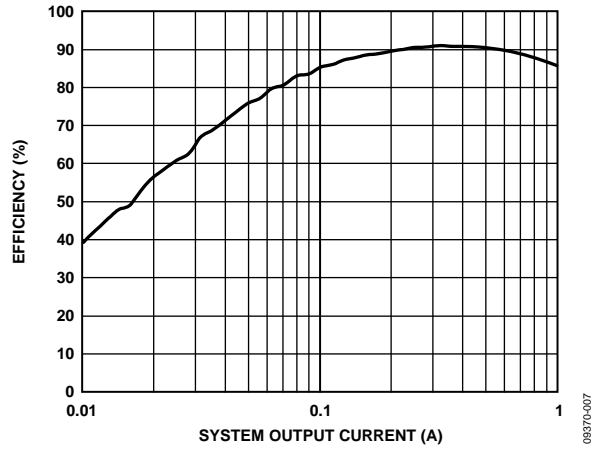


Figure 7. System Voltage Efficiency vs. Output Current, $V_{IN} = 5.0\text{ V}$

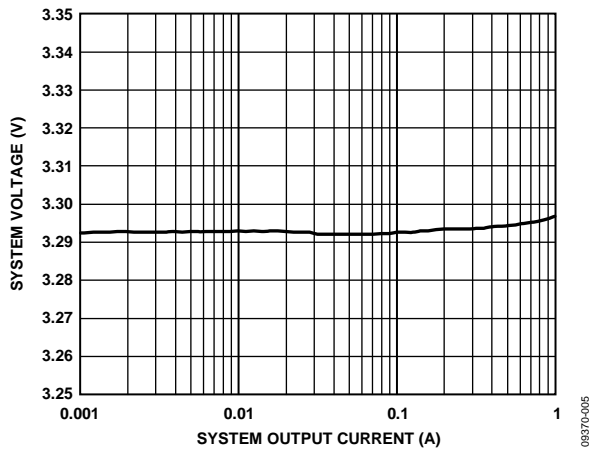


Figure 5. System Voltage Regulation vs. Output Current, $V_{IN} = 5.0\text{ V}$

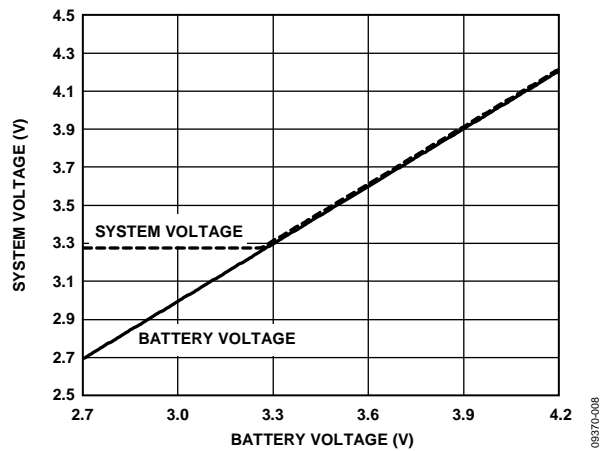


Figure 8. System Voltage vs. Battery Voltage, $V_{IN} = 5.0\text{ V}$, $I_{LIM} = 100\text{ mA}$

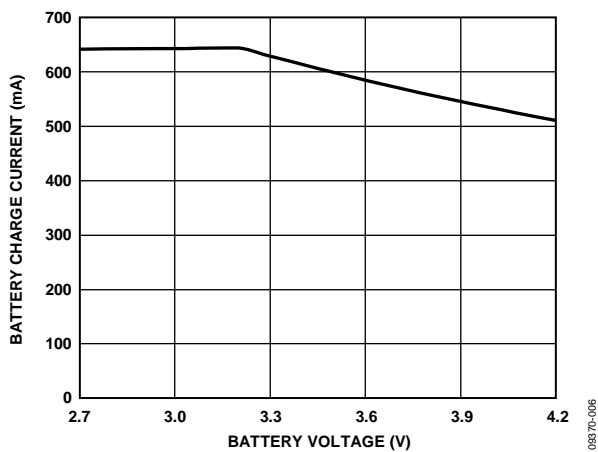


Figure 6. USB Compliant Charge Current vs. Battery Voltage, $V_{IN} = 5.0\text{ V}$, $I_{LIM} = 500\text{ mA}$

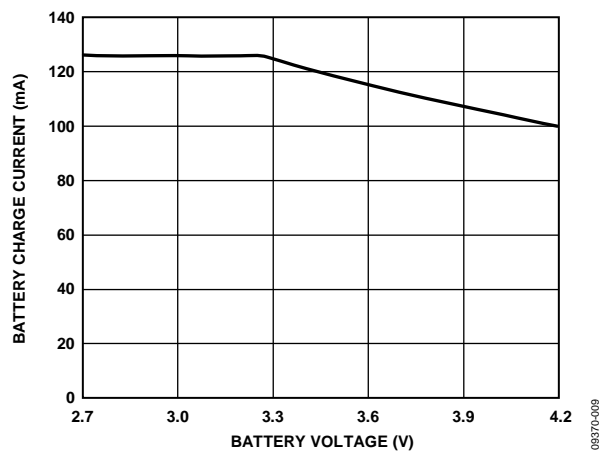


Figure 9. USB Limited Battery Charge Current vs. Battery Voltage, $V_{IN} = 5.0\text{ V}$, $I_{LIM} = 100\text{ mA}$

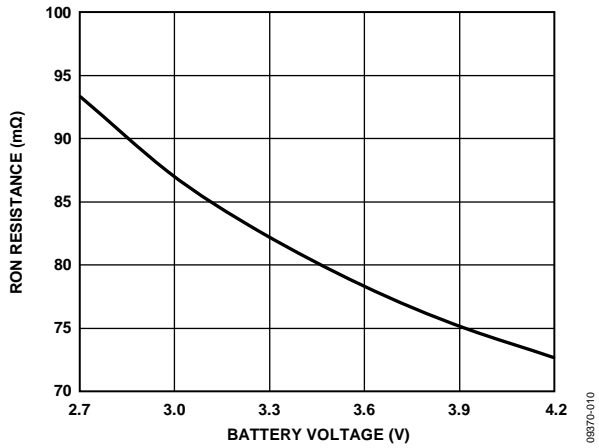


Figure 10. Battery Isolation FET Resistance vs. Battery Voltage, $V_{IN} = 5.0\text{ V}$, Load Current = 1.0 A

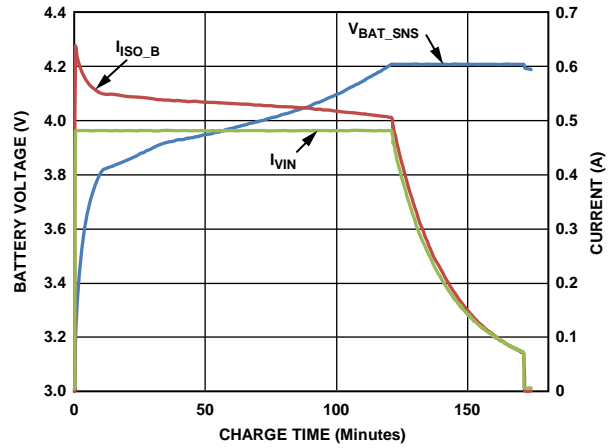


Figure 12. Charge Profile, $V_{IN} = 5.0\text{ V}$, $I_{LIM} = 500\text{ mA}$, Battery Capacity = 1320 mAh

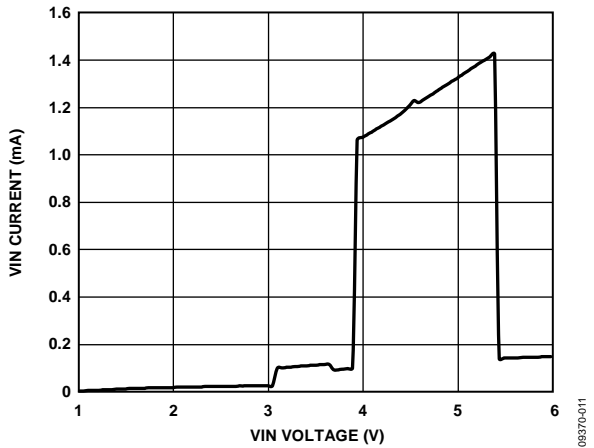


Figure 11. V_{INx} Current vs. V_{INx} Voltage, Suspend Mode ($EN_CHG = 0$)

TEMPERATURE CHARACTERISTICS

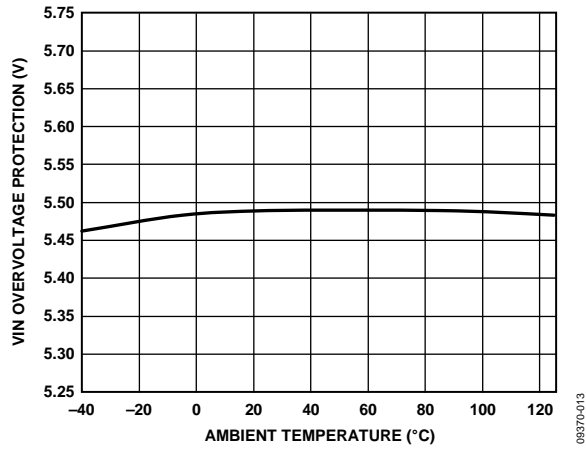


Figure 13. VINx Overvoltage Protection Rising Threshold vs. Ambient Temperature

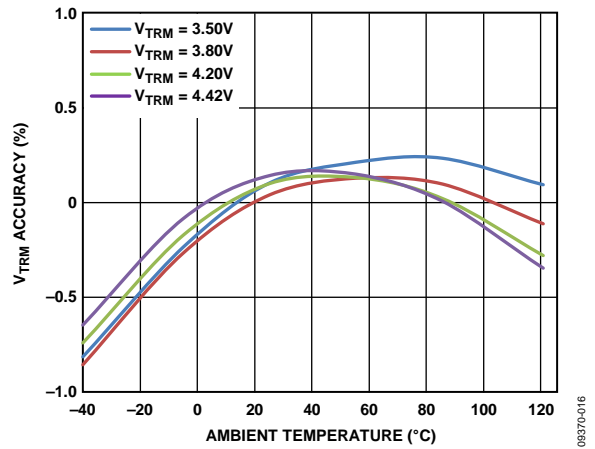


Figure 16. Termination Voltage vs. Ambient Temperature, VIN = 5.0 V, VTRM Programming 3.50 V, 3.80 V, 4.20 V, and 4.42 V

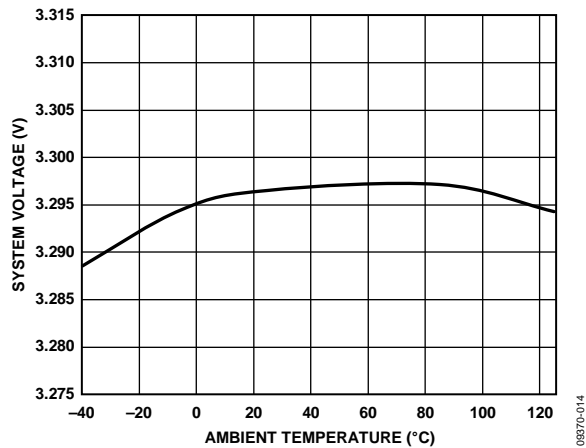


Figure 14. System Voltage vs. Ambient Temperature, VIN = 5.0 V, RLOAD = 33 Ω

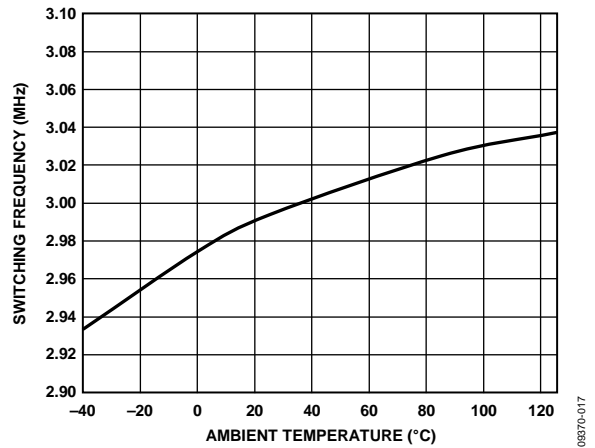


Figure 17. Switching Frequency vs. Ambient Temperature, VIN = 5.0 V

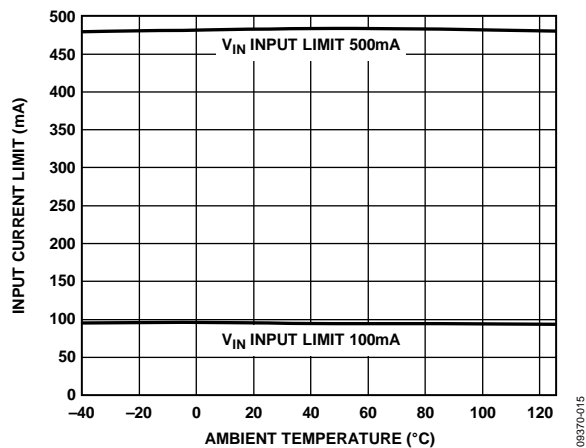


Figure 15. Input Current Limit vs. Ambient Temperature, VIN = 5.0 V

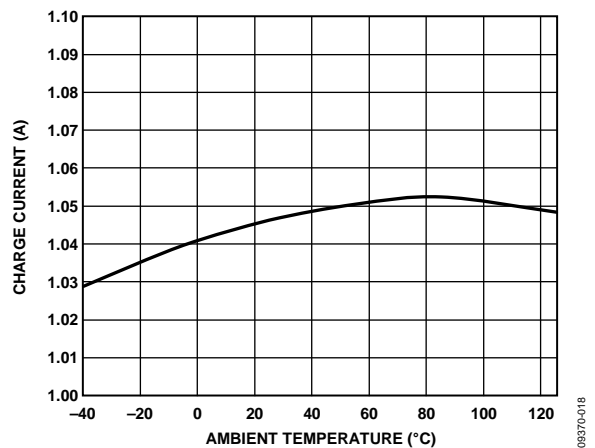


Figure 18. Fast Charge Current vs. Ambient Temperature, VIN = 5.0 V, VISO_B = 3.6 V, ICHG = 1050 mA

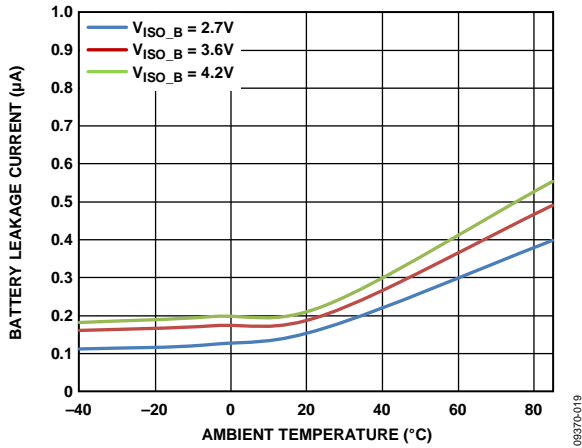


Figure 19. Battery Leakage Current vs. Ambient Temperature

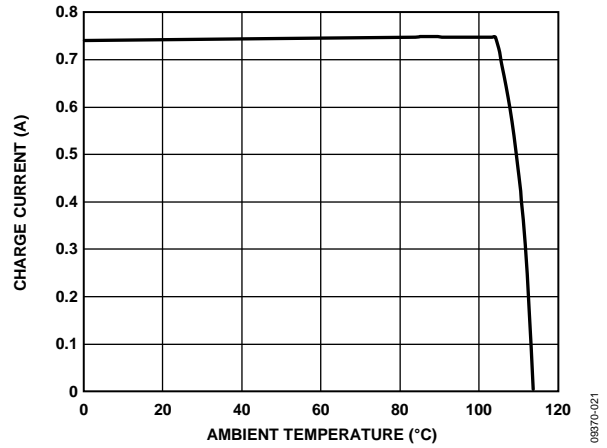


Figure 21. Isothermal Regulation of Charge Current vs. Ambient Temperature, $I_{CHG} = 750\text{ mA}$, $V_{IN} = 5.0\text{ V}$, $V_{ISO_B} = 3.6\text{ V}$

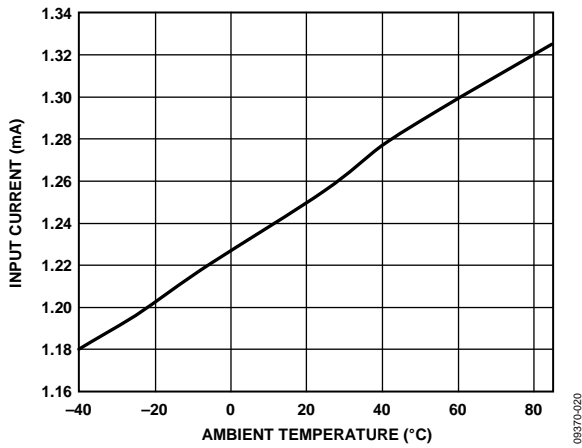


Figure 20. V_{INx} Quiescent Current vs. Temperature, $V_{IN} = 5.0\text{ V}$, Suspend Mode ($EN_CHG = 0$)

TYPICAL WAVEFORMS

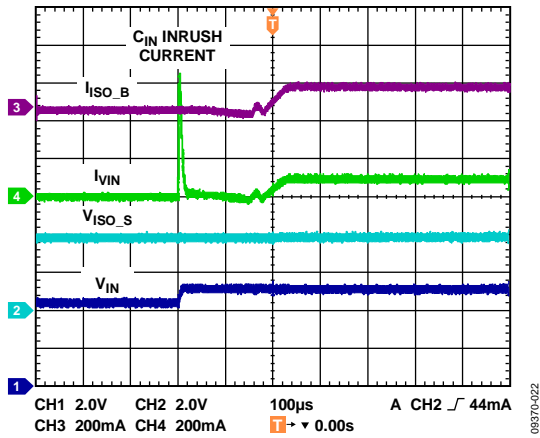


Figure 22. Typical Waveforms, VINx Connect From High Impedance to VBUS, ILIM = 100 mA

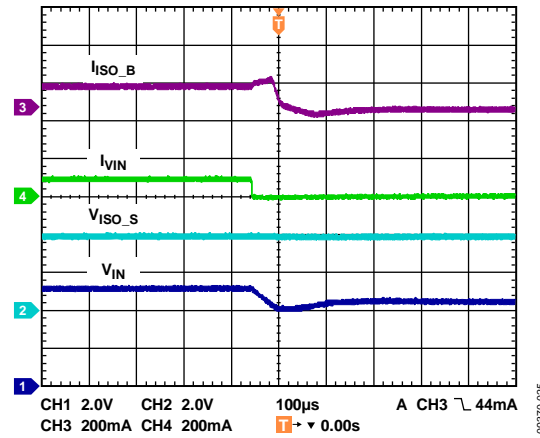


Figure 25. Typical Waveforms, VINx Disconnect from VBUS to High Impedance, ILIM = 100 mA

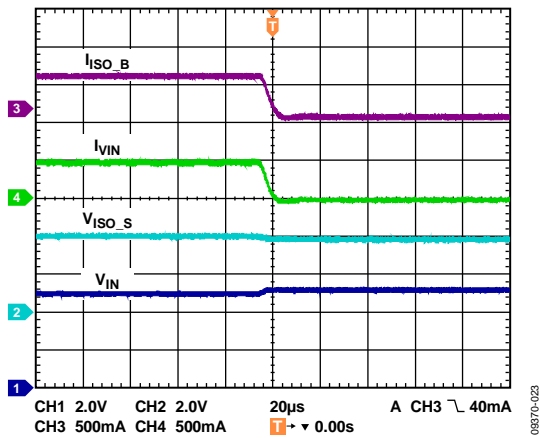


Figure 23. Mode Change, Fast Charge to Suspend (EN_CHG from High to Low), ILIM = 500 mA, R_LOAD = 33 Ω

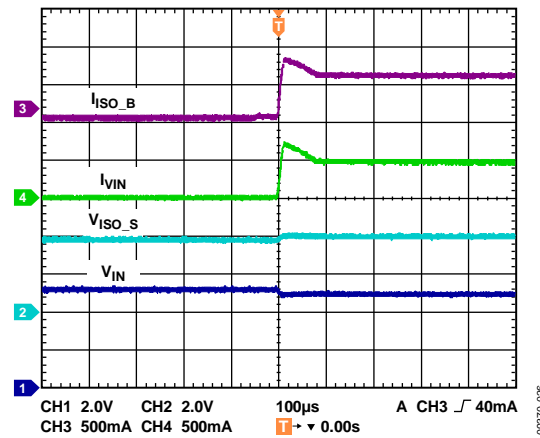


Figure 26. Mode Change, Suspend to Fast Charge (EN_CHG from Low to High), ILIM = 500 mA, R_LOAD = 33 Ω

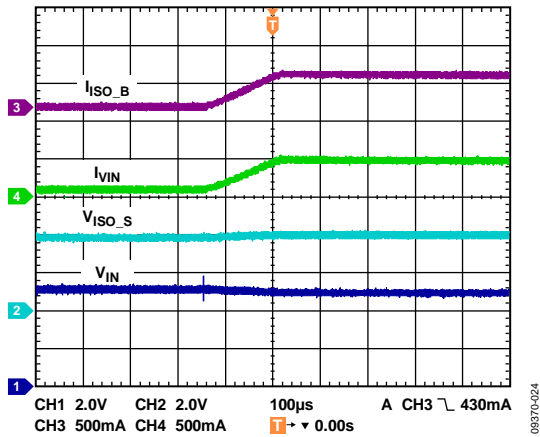


Figure 24. VINx Current Limit Change from 100 mA to 500 mA, EN_CHG = High, V_IN = 5.0 V, R_LOAD = 33 Ω

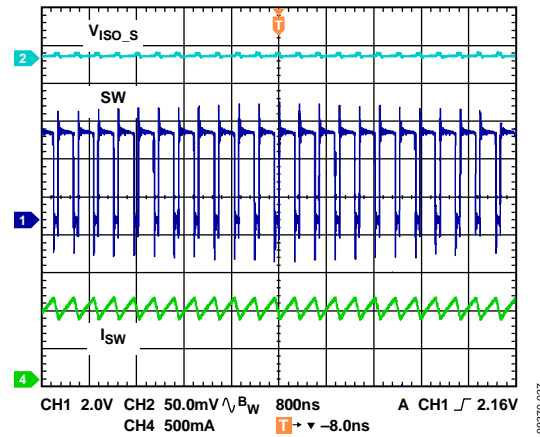


Figure 27. Typical Waveforms, Heavy Load, V_IN = 5.0 V, I_ISO_S = 1000 mA

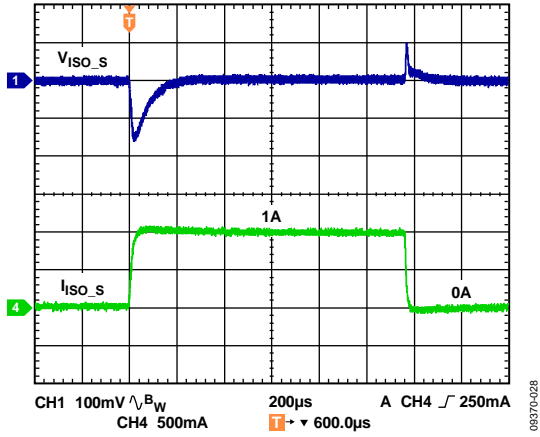


Figure 28. System Voltage Load Transient, $V_{IN} = 5.0V$, No Battery

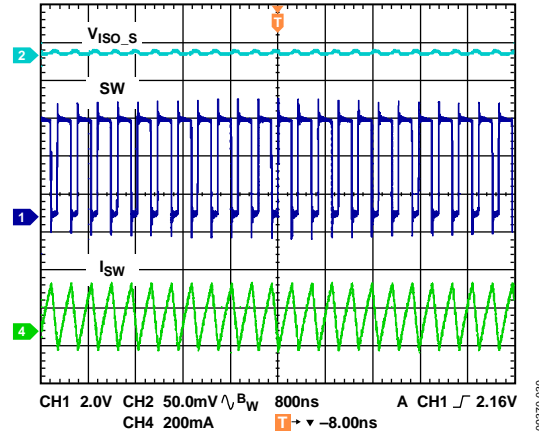


Figure 30. Typical Waveforms, Light Load, $V_{IN} = 5.0V$, $I_{ISO_S} = 100mA$

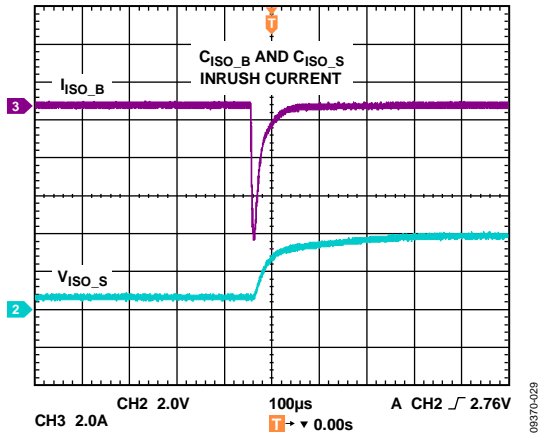


Figure 29. Battery Connect

THEORY OF OPERATION

INTRODUCTION

The [ADP5065](#) is a fully I²C-programmable charger for single-cell lithium-ion or lithium-polymer batteries suitable for a wide range of portable applications.

The highly efficient switcher dc-to-dc architecture enables higher charging currents as well as a lower temperature charging operation that results in faster charging times because of the following features:

- 3 MHz switch mode charger.
- 1.25 A charge current from dedicated charger.
- Up to 680 mA of charging current from a 500 mA USB host.

The [ADP5065](#) operates from an input voltage from 4 V to 5.5 V but is tolerant of voltages of up to 20 V. This alleviates the concern about USB bus spiking during disconnection or connection scenarios.

The [ADP5065](#) features an internal FET between the dc-to-dc charger output and the battery. This permits battery isolation and, hence, system powering in a dead battery or no battery scenario, which allows for immediate system function on connection to a USB power supply.

The [ADP5065](#) is fully compliant with the USB 3.0 battery charging specification and enables charging via the mini USB VBUS pin from a wall charger, car charger, or USB host port. Based on the type of USB source, which is detected by an external USB detection device, the [ADP5065](#) can be set to apply the correct current limit for optimal charging and USB compliance. The USB charger permits correct operation under all USB compliant sources such as, wall chargers, host chargers, hub chargers, and standard hosts and hubs.

A processor is able to control the USB charger using the I²C to program the charging current and numerous other parameters including

- Trickle charge current level.
- Trickle charge voltage threshold.
- Weak charge (constant current) charge current level.
- Fast charge (constant current) charge current level.
- Fast charge (constant voltage) charge voltage level at 1% accuracy.
- Fast charge safety timer period.
- Watchdog safety timer parameters.
- Weak battery threshold detection.
- Charge complete threshold.
- Recharge threshold.
- Charge enable/disable.
- Battery pack temperature detection and automatic charger shutdown.

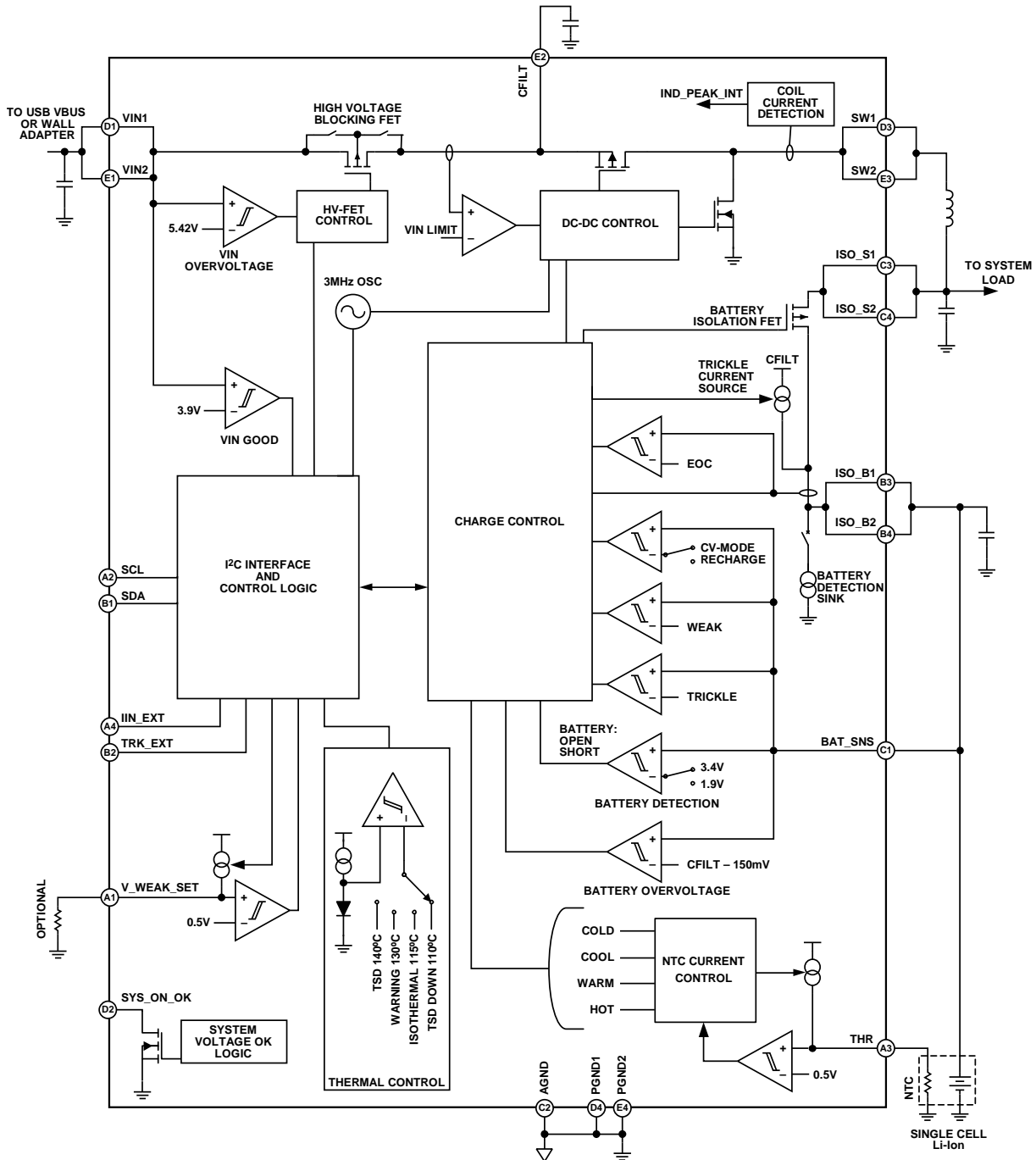


Figure 31. Block Diagram

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The ADP5065 also includes a number of significant features to optimize charging and functionality, including

- Thermal regulation for maximum performance.
- USB host current-limit accuracy: $\pm 5\%$.
- Termination voltage accuracy: $\pm 1\%$.
- Battery thermistor input with automatic charger shutdown in the event that the battery temperature exceeds limits. (Compliant with the JEITA Li-Ion battery charging temperature specification.)
- Offloads processor to manage external pin (TRK_EXT) control to enable/disable trickle charging.
- Direct external pin (IIN_EXT) control of 100 mA or 500 mA input current limit.
- Optional external resistor programming input, V_WEAK_SET, which is used for setting the V_{WEAK} threshold. When the battery reaches the V_{WEAK} threshold, the ADP5065 pulls down the SYS_EN_OK open-drain output flag. The flag can be used to hold off system turn on until the battery is at the minimum required level for a guaranteed system startup.

CHARGER MODES

Input Current Limit

The VINx input current limit is controlled via an internal I²C ILIM register. The input current limit can also be controlled via the IIN_EXT pin as outlined in Table 7. Any change in the I²C default from 100 mA dominates over the pin setting.

Table 7. IIN_EXT Operation

| IIN_EXT | Function |
|---------|--|
| 0 | 100 mA input current limit or I ² C programmed value |
| 1 | 500 mA input current limit or I ² C programmed value (or reprogrammed I ² C value from 100 mA default) |

USB Compatibility

The ADP5065 charger provides support for the following connections through the single connector VINx pin.

The ADP5065 features a programmable input current limit to ensure compatibility with the requirements listed in Table 8. The current limit defaults to 100 mA to allow compatibility with a USB host or hub that is not configured.

The I²C register default is 100 mA. An I²C write command to the ILIM register overrides the IIN_EXT pin and the I²C register default value can be reprogrammed for alternative requirements.

When the input current limiting feature is used, the available input current may be too low for the charger to meet the programmed charging current, I_{CHG}, and the rate of charge is reduced. In this case, the VIN_ILIM flag is set.

When connecting voltage to VINx without having the proper voltage level on the battery side, the HV blocking part is in a state wherein it draws only 1.3 mA (typical) of current until the V_{IN} has reached the VIN_OK level.

Table 8. Input Current Compatibility with Standard USB Limits

| Mode | Standard USB Limit | ADP5065 Function |
|-------------------|---|--|
| USB (China Only) | 100 mA limit for standard USB host or hub | 100 mA input current limit or I ² C programmed value |
| | 300 mA limit for Chinese USB specification | 300 mA input current limit or I ² C programmed value |
| USB 2.0 | 100 mA limit for standard USB host or hub | 100 mA input current limit or I ² C programmed value |
| | 500 mA limit for standard USB host or hub | 500 mA input current limit or I ² C programmed value |
| USB 3.0 | 150 mA limit for super speed USB 3.0 host or hub | 150 mA input current limit or I ² C programmed value |
| | 900 mA limit for super speed, high speed USB host or hub charger | 900 mA input current limit or I ² C programmed value |
| Dedicated Charger | 1500 mA limit for dedicated charger or low/full speed USB host or hub charger | 1500 mA input current limit or I ² C programmed value |

Trickle Charge Mode

A deeply discharged Li-Ion cell may exhibit a very low cell voltage making it unsafe to charge the cell at high current rates. The ADP5065 charger uses a trickle charge mode to reset the battery pack protection circuit and lift the cell voltage to a safe level for fast charging. A cell with a voltage below V_{TRK_DEAD} is charged with the trickle mode current, I_{TRK_DEAD}. During trickle charging mode, the CHARGER_STATUS register is set.

During trickle charging, the ISO_Sx node is regulated to V_{ISO_STRK} by the dc-to-dc converter and the battery isolation FET is off, which means the battery is isolated from the system power supply.

Trickle charging can be controlled via the TRK_EXT external pin (see Table 9). Note that any change in the I²C EN_TRK bit dominates over the pin setting.

Table 9. TRK_EXT Operation

| TRK_EXT | Function |
|---------|-------------------------|
| 0 | Trickle charge enabled |
| 1 | Trickle charge disabled |

Trickle Charge Mode Timer

The duration of trickle charge mode is monitored to ensure the battery is revived from its deeply discharged state. If trickle charge mode runs for longer than 60 minutes without the cell voltage reaching V_{TRK_DEAD}, a fault condition is assumed and charging stops. The fault condition is asserted on the CHARGER_STATUS register, allowing the user to initiate the fault recovery procedure specified in the Fault Recovery section.

Weak Charge Mode (Constant Current)

When the battery voltage exceeds V_{TRK_DEAD} but is less than V_{WEAK} , the charger switches to the intermediate charge mode.

During the weak charge mode, the battery voltage is too low to allow the full system to power-up. Due to the low level of the battery, the USB transceiver cannot be powered and, therefore, cannot enumerate for more current from a USB host.

Consequently, the USB limit remains at 100 mA.

The system microcontroller may or may not be powered by the charger output voltage (V_{ISO_SFC}) depending upon the amount of current required by the microcontroller and/or the system architecture. In this case, the battery charge current (I_{CHG_WEAK}) cannot be increased above 20 mA to ensure the microcontroller can still operate (if doing so) nor increased above the 100 mA USB limit. Thus, set the battery charging current as follows:

- Set the default 20 mA via the linear trickle charger branch (to ensure that the microprocessor remains alive if powered by the main switching charger output, ISO_Sx). Any residual current on the main switching charger output, ISO_Sx, is used to charge the battery at up to the preprogrammed level in the I²C for I_{CHG} (fast charge current limit) or I_{LIM} (input current limit).
- During weak current mode, other features may prevent the actual programmed weak charging current from reaching its full programmed value. Isothermal charging mode or input current limiting for USB compatibility may affect the programmed weak charging current value under certain operating conditions. During weak charging, the ISO_Sx node is regulated to V_{ISO_SFC} by the battery isolation FET.

Fast Charge Mode (Constant Current)

When the battery voltage exceeds V_{TRK_DEAD} and V_{WEAK} , the charger switches to fast charge mode, charging the battery with the constant current, I_{CHG} . During fast charge mode (constant current), the CHARGER_STATUS register is set.

During constant current mode, other features may prevent the current, I_{CHG} , from reaching its full programmed value.

Isothermal charging mode or input current limiting for USB compatibility may affect the value of I_{CHG} under certain operating conditions. The voltage on ISO_Sx is regulated to stay at V_{ISO_SFC} by the battery isolation FET when $V_{ISO_B} < V_{ISO_SFC}$.

Fast Charge Mode (Constant Voltage)

As the battery charges, its voltage rises and approaches the termination voltage, V_{TRM} . The ADP5065 charger monitors the voltage on the BAT_SNS pin to determine when charging should end. However, the internal ESR of the battery pack combined with PCB and other parasitic series resistances creates a voltage drop between the sense point at the BAT_SNS pin and the cell terminal itself. To compensate for this and ensure a fully charged cell, the ADP5065 enters a constant voltage charging mode when the termination voltage is detected on the BAT_SNS pin. The ADP5065 reduces charge current gradually as the cell continues to charge, maintaining a voltage of V_{TRM} on the BAT_SNS pin. During fast charge mode (constant voltage), the CHARGER_STATUS register is set.

Fast Charge Mode Timer

The duration of fast charge mode is monitored to ensure that the battery is charging correctly. If the fast charge mode runs for longer than t_{CHG} without the voltage at the BAT_SNS pin reaching V_{TRM} , a fault condition is assumed and charging stops. The fault condition is asserted on the CHARGER_STATUS register allowing the user to initiate the fault recovery procedure specified in the Fault Recovery section.

If the fast charge mode runs for longer than t_{CHG} , and V_{TRM} has been reached on the BAT_SNS pin but the charge current has not yet fallen below I_{END} , charging stops. No fault condition is asserted in this circumstance and charging resumes as normal if the recharge threshold is breached.

Watchdog Timer

The ADP5065 charger features a programmable watchdog timer function to ensure charging is under the control of the processor. The watchdog timer starts running when the ADP5065 charger determines that the processor should be operational, that is, when the processor sets the RESET_WD bit for the first time or when the battery voltage is greater than the weak battery threshold, V_{WEAK} . When the watchdog timer has been triggered, it must be reset regularly within the watchdog timer period, t_{WD} .

If the watchdog timer expires without being reset while in charger mode, the ADP5065 charger assumes there is a software problem and triggers the safety timer, t_{SAFE} . For more information see the Safety Timer section.

Safety Timer

If the watchdog timer (see the Watchdog Timer section for more information) expires while in charger mode, the ADP5065 charger initiates the safety timer, t_{SAFE} . If the processor has programmed charging parameters by this time, the I_{LIM} is set to the default value. Charging continues for a period of t_{SAFE} , then the charger switches off and sets the CHARGER_STATUS register.

Charge Complete

The ADP5065 charger monitors the charging current while in constant voltage fast charge mode. If the current falls below I_{END} and remains below I_{END} for t_{END} , charging stops and the CHDONE flag is set. If the charging current falls below I_{END} for less than t_{END} and then rises above I_{END} again, the t_{END} timer resets.

Recharge

After the detection of charge complete, and the cessation of charging, the ADP5065 charger monitors the BAT_SNS pin as the battery discharges through normal use. If the BAT_SNS pin voltage falls to V_{RCH} , the charger reactivates charging. Under most circumstances, triggering the recharge threshold results in the charger starting directly into fast charge constant voltage mode.

Battery Charging Enable/Disable

The ADP5065 charging function can be disabled by setting the I²C EN_CHG bit to low.

THERMAL MANAGEMENT**Isothermal Charging**

To assist with the thermal management of the ADP5065 charger, the battery charger provides an isothermal charging function. As the on-chip power dissipation and die temperature increase, the ADP5065 charger monitors die temperature and limits output current when the temperature reaches T_{LIM} (typically at 115°C). The die temperature is maintained at T_{LIM} through the control of the charging current into the battery. A reduction in power dissipation or ambient temperature may allow the charging current to return to its original value, and the die temperature subsequently drops below T_{LIM} . During isothermal charging, the THERM_LIM flag is set to high.

Thermal Shutdown and Thermal Early Warning

The ADP5065 switching charger features a thermal shutdown threshold detector. If the die temperature exceeds T_{SD} , the ADP5065 charger is disabled, and the TSD 140°C bit is set. The ADP5065 charger can be reenabled when the die temperature drops below the T_{SD} falling limit and the TSD 140°C bit is reset. To reset the TSD 140°C bit, write to the I²C Fault Register 0x0D or cycle the power.

Before die temperature reaches T_{SD} , the early warning bit is set if T_{SDL} is exceeded. This allows the system to accommodate power consumption before thermal shutdown occurs.

Fault Recovery

Before performing the following operation, it is important to ensure that the cause of the fault has been rectified.

To recover from a charger fault (when the CHARGER_STATUS equals 110), cycle power on VINx or write high to reset the I²C fault bits in the fault register.

BATTERY ISOLATION FET

The ADP5065 charger features an integrated battery isolation FET for power path control. The battery isolation FET isolates a deeply discharged Li-Ion cell from the system power supply in both trickle and fast charge modes, thereby allowing the system to be powered at all times.

When VINx is below V_{VIN_OK} , the battery isolation FET is in full conducting mode.

The battery isolation FET is off during trickle charge mode. When the battery voltage exceeds V_{TRK} , the battery isolation FET switches to the system voltage regulation mode. During system voltage regulation mode, the battery isolation FET maintains the V_{ISO_SFC} voltage on the ISO_Sx pins. When the battery voltage exceeds V_{ISO_SFC} , the battery isolation FET is in full conducting mode.

The battery isolation FET supplements the battery to support high current functions on the system power supply.

When voltage on ISO_Sx drops below ISO_Bx, the battery isolation FET enters into full conducting mode.

When voltage on ISO_Sx rises above ISO_Bx, the isolation FET enters regulating mode or full conduction mode, depending on the Li-Ion cell voltage and the dc-to-dc charger mode.

BATTERY DETECTION

Battery Level Detection

The ADP5065 charger features a battery detection mechanism to detect an absent battery. The charger actively sinks and sources current into the ISO_Bx/BAT_SNS node, and voltage vs. time is detected. The sink phase is used to detect a charged battery, whereas the source phase is used to detect a discharged battery.

The sink phase (see Figure 32) sinks I_{SINK} current from the ISO_Bx/ BAT_SNS pins for a time, t_{BATOK} . If the BAT_SNS pin is below V_{BATL} when the t_{BATOK} timer expires, the charger assumes no battery is present, and starts the source phase. If the BAT_SNS exceeds the V_{BATL} voltage when the t_{BATOK} timer expires, the charger assumes the battery is present, and begins a new charge cycle.

The source phase sources I_{SOURCE} current to ISO_Bx or the BAT_SNS pins for a time, t_{BATOK} . If the BAT_SNS pin exceeds V_{BATH} before the t_{BATOK} timer expires, the charger assumes that no battery is present. If the BAT_SNS does not exceed the V_{BATH} voltage when the t_{BATOK} timer expires, the charger assumes that a battery is present, and begins a new charge cycle.

Battery (ISO_Bx) Short Detection

A battery short occurs under a damaged battery condition or when the battery protection circuitry is enabled.

On commencing trickle charging, the ADP5065 charger monitors the battery voltage. If this battery voltage does not exceed V_{BAT_SHR} within the specified timeout period, t_{BAT_SHR} , a fault is declared and the charger is stopped by turning the battery isolation FET off but the system voltage is maintained at V_{ISO_STRK} by the linear regulator.

The trickle charge branch is active during the battery short scenario, and trickle charge current to the battery is maintained until the 60 minute trickle charge mode timer expires.

After source phase, if the ISO_Bx or BAT_SNS level remains below V_{BATH} , either the battery voltage is low or the battery node can be shorted. As a result of the battery voltage being low, trickle charging mode is initiated (see Figure 33). If the BAT_SNS level remains below V_{BAT_SHR} after t_{BAT_SHR} has elapsed, the ADP5065 assumes that the battery node is shorted.

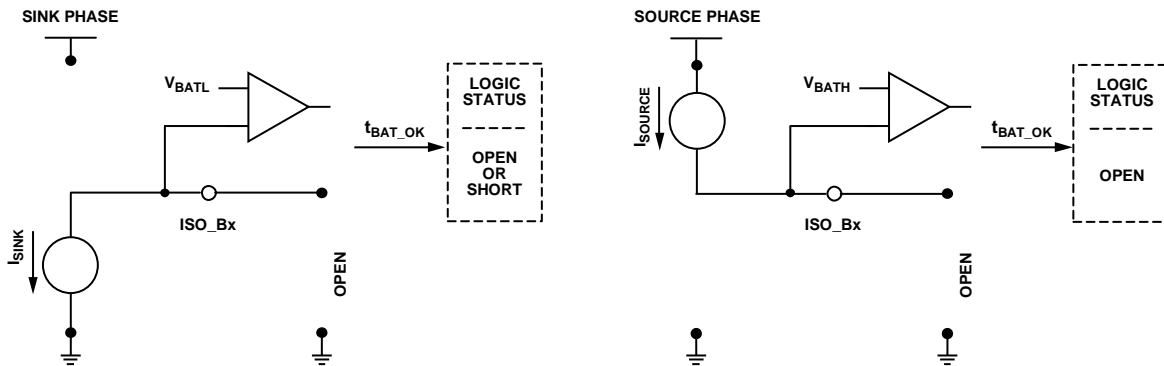


Figure 32. Battery Detection Sequence

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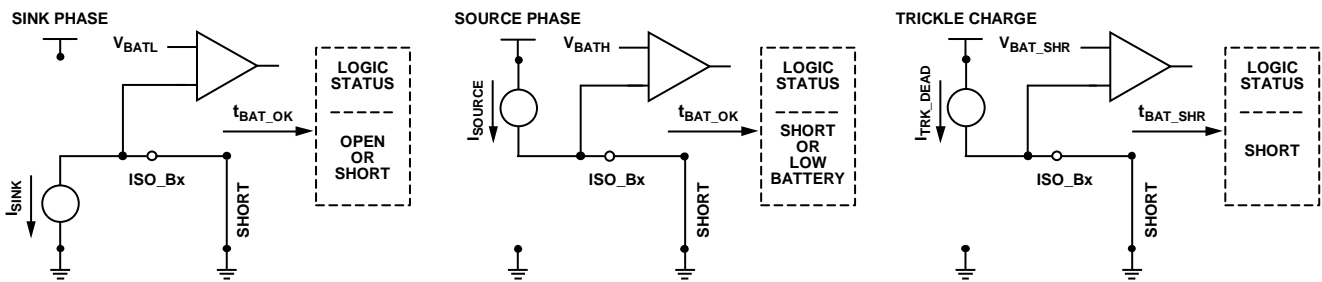


Figure 33. Battery Short Detection Sequence

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BATTERY PACK TEMPERATURE SENSING

Battery Thermistor Input

The ADP5065 charger features battery pack temperature sensing that precludes charging when the battery pack temperature is outside the specified range. The THR pin provides an on and off switching current source, which should be connected directly to the battery pack thermistor terminal. The activation interval of the THR current source is 167 ms.

The battery pack temperature sensing can be controlled by I²C using the conditions shown in Table 10. Note that the I²C register default setting for EN_THR (Register 0x07) is 0 = temperature sensing off.

Table 10. THR Input Function

| Conditions | | THR Function |
|--------------------------------------|--------------------|-------------------------------------|
| VINx | V _{ISO_B} | |
| Open or V _{IN} = 0V to 4.0V | <2.5V | Off |
| Open or V _{IN} = 0V to 4.0V | >2.5V | Off, controlled by I ² C |
| 4.0V to 5.5V | Don't care | Always on |

If the battery pack thermistor is not connected directly to the ADP5065 THR pin, a 10 kΩ (tolerance ±20%) dummy resistor must be connected between the THR input and GND. Leaving the THR pin open results in a false detection of the battery temperature being <0°C and charging is disabled.

The ADP5065 charger monitors the voltage in the THR pin and suspends charging if the current is outside the range of less than 0°C or greater than 60°C. For temperatures greater than 0°C, the THR_STATUS register is set accordingly, and for temperatures lower than 60°C, the THR_STATUS register is, likewise, set accordingly.

The ADP5065 charger is designed for use with an NTC thermistor in the battery pack with a nominal room temperature value of either 10 kΩ at 25°C or 100 kΩ at 25°C, which is selected by a fuse.

The ADP5065 charger is designed for use with an NTC thermistor in the battery pack with a temperature coefficient curve (beta). Fuse-selectable beta programming is supported by eight steps covering a range from 3150 to 4400 (see Table 34).

JEITA Li-Ion Battery Temperature Charging Specification

The ADP5065 is compliant with the JEITA Li-Ion battery charging temperature specifications as outlined in Table 11.

The JEITA function can be enabled via the I²C interface. When the ADP5065 detects a JEITA cool condition, charging current is reduced according to Table 12.

When the ADP5065 identifies a hot or cold battery condition, the ADP5065 takes the following actions:

- Stops charging the battery.
- Connects/enables the battery isolation FET such that the system power supply node is connected to the battery.

Table 11. JEITA Li-Ion Battery Charging Specification Defaults

| Parameter | Symbol | Conditions | Min | Max | Unit |
|----------------------------------|-------------------------|--|-----|-----|------|
| JEITA Cold Temperature Limits | I _{JEITA_COLD} | No battery charging occurs. | | 0 | °C |
| JEITA Cool Temperature Limits | I _{JEITA_COOL} | Battery charging occurs at approximately 50% of programmed level. See Table 12 for specific charging current reduction levels. | 0 | 10 | °C |
| JEITA Typical Temperature Limits | I _{JEITA_TYP} | Normal battery charging occurs at default/programmed levels. | 10 | 45 | °C |
| JEITA Warm Temperature Limits | I _{JEITA_WARM} | Battery termination voltage (V _{TRM}) is reduced by 100 mV from programmed value. | 45 | 60 | °C |
| JEITA Hot Temperature Limits | I _{JEITA_HOT} | No battery charging occurs. | 60 | | °C |

Table 12. JEITA Reduced Charge Current Levels

| JEITA Cool Temperature Limit—Reduced Charge Current Levels | |
|--|-----------------|
| ICHG[2:0] (Default) | ICHG JEITA (mA) |
| 000 = 550 mA | 250 |
| 001 = 650 mA | 300 |
| 010 = 750 mA | 350 |
| 011 = 850 mA | 400 |
| 100 = 950 mA | 450 |
| 101 = 1050 mA | 500 |
| 110 = 1150 mA | 550 |
| 111 = 1250 mA | 600 |

EXTERNAL RESISTOR FOR V_WEAK_SET

The ADP5065 charger features a V_{WEAK} threshold, which can be used for enabling the main PMU system. When battery voltage at the BAT_SNS pin exceeds the V_{WEAK} level, the ADP5065 pulls down the SYS_ON_OK open-drain flag.

The V_{WEAK} threshold can be programmed set either by I²C or by an external resistor connected between the V_WEAK_SET pin and GND. Recommended resistor values for each threshold are listed in Table 13.

If an external resistor is not used, it is recommended to tie the V_WEAK_SET pin to AGND for V_{WEAK} to obtain its default value.

Table 13. Resistor Values for V_WEAK_SET Pin

| Target Resistor Value E24 (k Ω) | Actual Threshold (k Ω) | V_{WEAK} Voltage (Rising Threshold) | V_{WEAK} Voltage (Falling Threshold) |
|---|--------------------------------|--|---|
| Short to GND | Not applicable | I ² C (3.0V default) | I ² C programmed – 100 mV |
| 15 | 13.2 | 2.7 V | 2.6 V |
| 20 | 17.8 | 2.8 V | 2.7 V |
| 27 | 23.5 | 2.9 V | 2.8 V |
| 36 | 31.0 | 3.0 V | 2.9 V |
| 47 | 41.3 | 3.1 V | 3.0 V |
| 68 | 56.2 | 3.2 V | 3.1 V |
| 100 | 79.7 | 3.3 V | 3.2 V |
| Open | 122.4 | 3.4 V | 3.3 V |

I²C INTERFACE

The ADP5065 includes an I²C-compatible serial interface for control of the charging and for a readback of system status registers. The I²C chip address is 0x28 in write mode and 0x29 in read mode.

Register values are reset to the default values, when the supply voltage at the VINx pin falls below the V_{VIN_OK} falling voltage threshold. The I²C registers are also reset when the battery is disconnected and V_{IN} is 0 V.

See Figure 34 for an example of the I²C write sequence to a single register. The subaddress content selects which one of the five ADP5065 registers is written to first. The ADP5065 sends an acknowledgement to the master after the 8-bit data byte has been written. The ADP5065 increments the subaddress automatically and starts receiving a data byte to the following register until the master sends an I²C stop as shown in Figure 35.

Figure 36 shows the I²C read sequence of a single register. ADP5065 sends the data from the register denoted by the subaddress and increments the subaddress automatically, sending data from the next register until the master sends an I²C stop condition as shown in Figure 37.

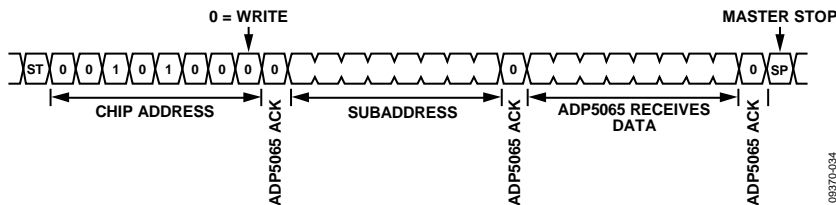


Figure 34. I²C Single Register Write Sequence

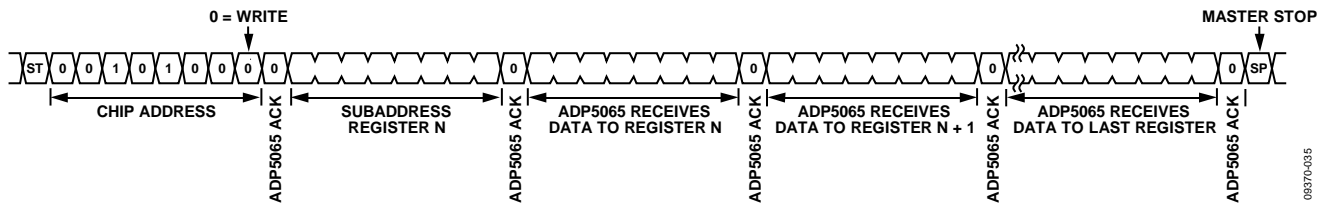


Figure 35. I²C Multiple Register Write Sequence

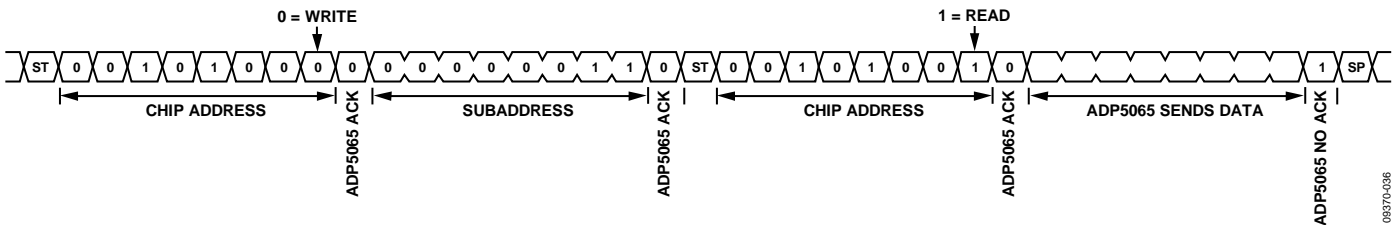


Figure 36. I²C Single Register Read Sequence

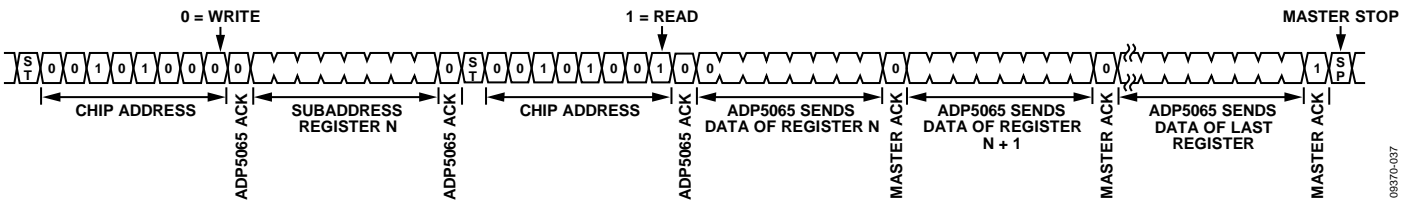


Figure 37. I²C Multiple Register Read Sequence

CHARGER OPERATIONAL FLOWCHART

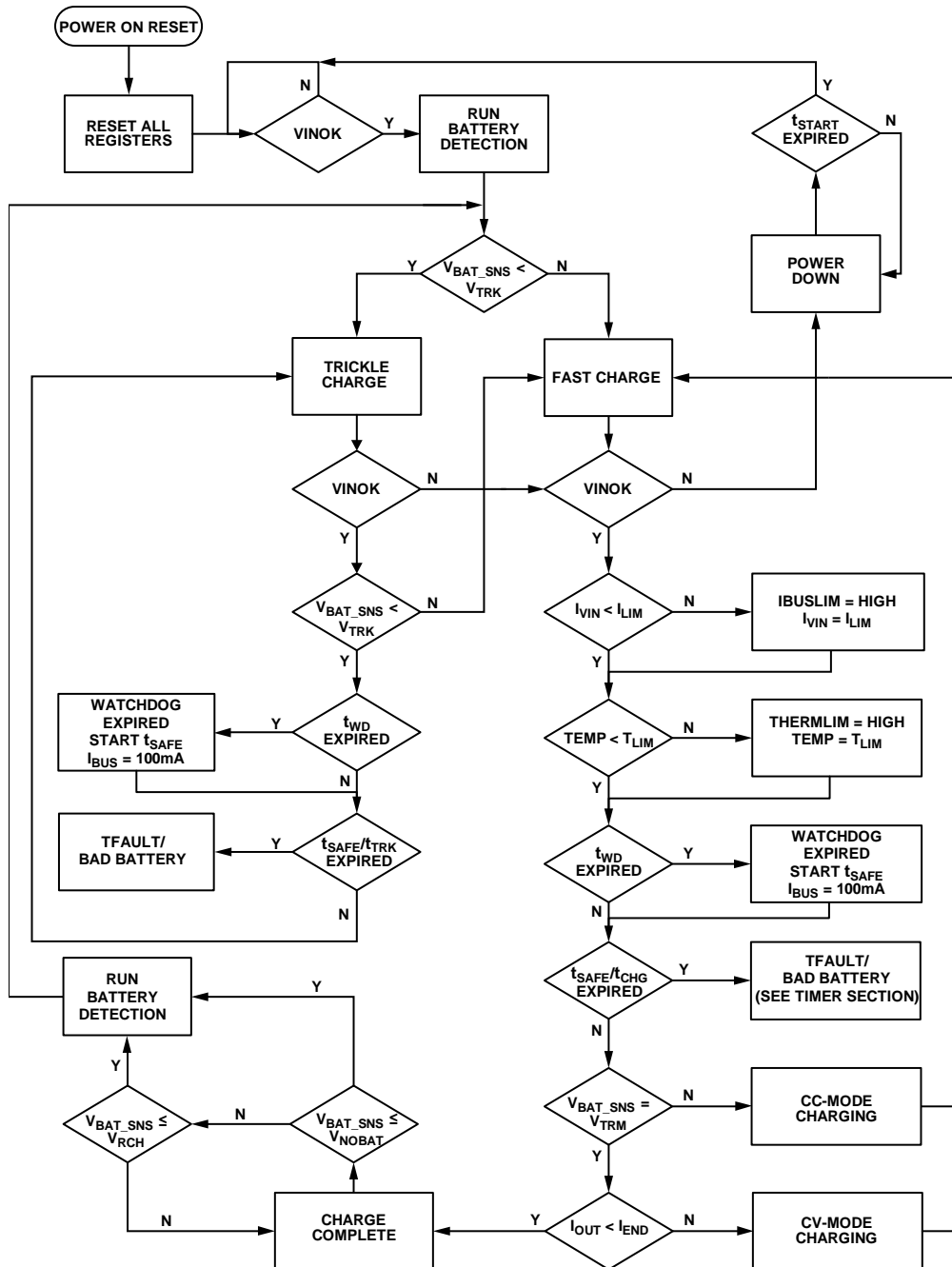


Figure 38. ADP5065 Operational Flowchart

06370-038

I²C REGISTER MAPTable 14. I²C Register Map¹

| Register | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|----------|---------------------------|-----------------|------------------|------------------|--------------|----------------|----------------|------------|------------|--|
| Addr. | Name | | | | | | | | | |
| 0x00 | Manufacturer and model ID | MANUF | | | | Model | | | | |
| 0x01 | Silicon revision | | | | | REV | | | | |
| 0x02 | VINx pins settings | | | | RFU | ILIM | | | | |
| 0x03 | Termination settings | VTRM | | | | | | | IEND | |
| 0x04 | Charging current | C/20 EOC | C/10 EOC | High (read only) | ICHG | | | ITRK_DEAD | | |
| 0x05 | Voltage threshold | | VRCH | | VTRK_DEAD | | VWEAK | | | |
| 0x06 | Timer settings | | | EN_TEND | EN_CHG_TIMER | CHG_TMR_PERIOD | EN_WD | WD PERIOD | RESET_WD | |
| 0x07 | Functional Settings1 | EN_JEITA | DIS_IPK_SD | EN_BMON | EN_THR | | EN_EOC | EN_TRK | EN_CHG | |
| 0x08 | Functional Settings2 | | | | | | | | | |
| 0x09 | Interrupt enable | EN_IND_PEAK_INT | EN_THERM_LIM_INT | EN_WD_INT | EN_TSD_INT | EN_THR_INT | EN_BAT_INT | EN_CHG_INT | EN_VIN_INT | |
| 0x0A | Interrupt active | IND_PEAK_INT | THERM_LIM_INT | WD_INT | TSD_INT | THR_INT | BAT_INT | CHG_INT | VIN_INT | |
| 0x0B | Charger Status 1 | VIN_OV | VIN_OK | VIN_ILIM | THERM_LIM | CHDONE | CHARGER_STATUS | | | |
| 0x0C | Charger Status 2 | THR_STATUS | | | IPK_STAT | | BATTERY_STATUS | | | |
| 0x0D | Fault register | | | | | BAT_SHR | IND_PEAK_INT | TSDL 130°C | TSD 140°C | |
| 0x10 | Battery short | TBAT_SHR | | | | | | VBAT_SHR | | |

¹ Each blank cell indicates a bit that is not used.

REGISTER BIT DESCRIPTIONS**Table 15. Manufacturer and Model ID, Register Address 0x00 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---------|------------|--------|---------|--|
| [7:4] | MANUF[3:0] | R | 0001 | The 4-bit manufacturer identification bus. |
| [3:0] | MODEL[3:0] | R | 1000 | The 4-bit model identification bus. |

Table 16. Silicon Revision, Register Address 0x01 Bit Descriptions

| Bit No. | Mnemonic | Access | Default | Description |
|---------|----------|--------|---------|--|
| [7:4] | Not Used | R | | |
| [3:0] | REV[3:0] | R | 0101 | The 4-bit silicon revision identification bus. |

Table 17. VINx Settings, Register Address 0x02 Bit Descriptions

| Bit No. | Mnemonic | Access | Default | Description |
|---------|-----------|--------|---------------|--|
| [7:5] | Not Used | R | | |
| 4 | RFU | R/W | 0 | Reserved for future use. |
| [3:0] | ILIM[3:0] | R/W | 0000 = 100 mA | VINx pin input current-limit programming bus. The current into VINx can be limited to the following programmed values: 0000 = 100 mA. 0001 = 150 mA. 0010 = 200 mA. 0011 = 300 mA. 0100 = 400 mA. 0101 = 500 mA. 0110 = 600 mA. 0111 = 700 mA. 1000 = 800 mA. 1001 = 900 mA. 1010 = 1000 mA. 1011 = 1100 mA. 1100 = 1200 mA. 1101 = 1300 mA. 1110 = 1400 mA. 1111 = 1500 mA. |

Table 18. Termination Settings, Register Address 0x03 Bit Descriptions

| Bit No. | Mnemonic | Access | Default | Description |
|---------|-----------|--------|-----------------|--|
| [7:2] | VTRM[5:0] | R/W | 100011 = 4.20 V | <p>Termination voltage programming bus. The values of the float voltage can be programmed as per the following values:</p> <p>000000 = 3.50 V. 000001 = 3.52 V. 000010 = 3.54 V. 000011 = 3.56 V. 000100 = 3.58 V. 000101 = 3.60 V. 000110 = 3.62 V. 000111 = 3.64 V. 001000 = 3.66 V. 001001 = 3.68 V. 001010 = 3.70 V. 001011 = 3.72 V. 001100 = 3.74 V. 001101 = 3.76 V. 001110 = 3.78 V. 001111 = 3.80 V. 010000 = 3.82 V. 010001 = 3.84 V. 010010 = 3.86 V. 010011 = 3.88 V. 010100 = 3.90 V. 010101 = 3.92 V. 010110 = 3.94 V. 010111 = 3.96 V. 011000 = 3.98 V. 011001 = 4.00 V. 011010 = 4.02 V. 011011 = 4.04 V. 011100 = 4.06 V. 011101 = 4.08 V. 011110 = 4.10 V. 011111 = 4.12 V. 100000 = 4.14 V. 100001 = 4.16 V. 100010 = 4.18 V. 100011 = 4.20 V. 100100 = 4.22 V. 100101 = 4.24 V. 100110 = 4.26 V. 100111 = 4.28 V. 101000 = 4.30 V. 101001 = 4.32 V. 101010 = 4.34 V. 101011 = 4.36 V. 101100 = 4.38 V. 101101 = 4.40 V. 101110 to 111111 = 4.42 V.</p> |

| Bit No. | Mnemonic | Access | Default | Description |
|---------|-----------|--------|--------------|---|
| [1:0] | IEND[1:0] | R/W | 01 = 52.5 mA | Termination current programming bus. The values of the termination current can be programmed as per the following values: 00 = 32.5 mA. 01 = 52.5 mA. 10 = 72.5 mA. 11 = 92.5 mA. |

Table 19. Charging Current, Register Address 0x04 Bit Descriptions

| Bit No. | Mnemonic | Access | Default | Description |
|---------|--------------------|--------|---------------|--|
| 7 | C/20 EOC | R/W | | The C/20 bit has priority over the other settings (C/10 EOC and IEND). When this bit is set to high, C/20 programming is used. 27.5 mA minimum value. |
| 6 | C/10 EOC | R/W | | The C/10 bit has priority over the other setting (END) but not C/20 EOC. When this bit is set to high, C/10 programming is used unless C/20 EOC is set to high. 27.5 mA minimum value. |
| 5 | Tied high in metal | R | 1 | |
| [4:2] | ICHG[2:0] | R/W | 111 = 1250 mA | Fast charge current programming bus. The values of the constant current charge can be programmed as per the following values: 000 = 550 mA. 001 = 650 mA. 010 = 750 mA. 011 = 850 mA. 100 = 950 mA. 101 = 1050 mA. 110 = 1150 mA. 111 = 1250 mA. |
| [1:0] | ITRK_DEAD[1:0] | R/W | 10 = 20 mA | Trickle and weak charge current programming bus. The values of the trickle and weak charge currents can be programmed as per the following values: 00 = 5 mA. 01 = 10 mA. 10 = 20 mA. 11 = 20 mA. |

Table 20. Voltage Threshold, Register Address 0x05 Bit Descriptions

| Bit No. | Mnemonic | Access | Default | Description |
|---------|----------------|--------|-------------|--|
| 7 | Not used | R | | |
| [6:5] | VRCH[1:0] | R/W | 11 = 260 mV | Recharge voltage programming bus. The values of the recharge threshold can be programmed as per the following values: 00 = 80 mV. 01 = 140 mV. 10 = 200 mV. 11 = 260 mV. |
| [4:3] | VTRK_DEAD[1:0] | R/W | 01 = 2.5 V | Trickle to fast charge dead battery voltage programming bus. The values of the trickle to fast charge threshold can be programmed as per following values: 00 = 2.4 V. 01 = 2.5 V. 10 = 2.6 V. 11 = 3.3 V. |

| Bit No. | Mnemonic | Access | Default | Description |
|---------|------------|--------|-------------|--|
| [2:0] | VWEAK[2:0] | R/W | 011 = 3.0 V | Weak battery voltage rising threshold. 000 = 2.7 V. 001 = 2.8 V. 010 = 2.9 V. 011 = 3.0 V. 100 = 3.1 V. 101 = 3.2 V. 110 = 3.3 V. 111 = 3.4 V. |

Table 21. Timer Settings, Register Address 0x06 Bit Descriptions

| Bit No. | Mnemonic | Access | Default | Description |
|---------|----------------|--------|---------|---|
| [7:6] | Not used | | | |
| 5 | EN_TEND | R/W | 0 | When low, this bit disables the charge complete timer (t_{END}), and a 31 ms deglitch timer remains on this function. |
| 4 | EN_CHG_TIMER | R/W | 1 | When high, the trickle/fast charge timer is enabled. |
| 3 | CHG_TMR_PERIOD | R/W | 1 | Trickle/fast charge timer period. 0 = 30 sec/300 minutes. 1 = 60 sec/600 minutes. |
| 2 | EN_WD | R/W | 0 | When high, the watchdog timer safety timer is enabled. When low, the watchdog timer is disabled even when BAT_SNS exceeds V_{DEAD} . |
| 1 | WD PERIOD | R/W | 0 | Watchdog safety timer period. 0 = 32 sec/40 minutes. 1 = 64 sec/40 minutes. |
| 0 | RESET_WD | W | 0 | High resets the watchdog safety timer. Bit is reset automatically. |

Table 22. Functional Settings¹, Register Address 0x07 Bit Descriptions

| Bit No. | Mnemonic | Access | Default | Description |
|---------|------------|--------|---------|--|
| 7 | EN_JEITA | R/W | 0 | When low, this bit disables the JEITA Li-Ion temperature battery charging specification. |
| 6 | DIS_IPK_SD | R/W | 1 | When high, this bit disables the automatic shutdown of the device if four peak inductor current limits are reached in succession. In addition, when high, it only flags the Status Bit IPK_STAT. |
| 5 | EN_BMON | R/W | 0 | When high, the battery monitor is enabled even when the voltage at the VINx pins is below V_{VIN_OK} . |
| 4 | EN_THR | R/W | 0 | When high, the THR current source is enabled even when the voltage at the VINx pins is below V_{VIN_OK} . |
| 3 | Not used | R/W | 0 | |
| 2 | EN_EOC | R/W | 1 | When high, end of charge is allowed. |
| 1 | EN_TRK | R/W | 1 | When low, trickle charger is disabled and the dc-to-dc converter is enabled. |
| 0 | EN_CHG | R/W | 1 | When low, the dc-to-dc converter is disabled. |

Table 23. Functional Settings², Register Address 0x08 Bit Descriptions

| Bit No. | Mnemonic | Access | Default | Description |
|---------|----------|--------|---------|-------------|
| [7:0] | Not used | R/W | | |

Table 24. Interrupt Enable, Register Address 0x09 Bit Descriptions

| Bit No. | Mnemonic | Access | Default | Description |
|---------|------------------|--------|---------|--|
| 7 | EN_IND_PEAK_INT | R/W | 0 | When high, the inductor peak current-limit interrupt is allowed. |
| 6 | EN_THERM_LIM_INT | R/W | 0 | When high, the isothermal charging interrupt is allowed. |
| 5 | EN_WD_INT | R/W | 0 | When high, the watchdog alarm interrupt is allowed. |
| 4 | EN_TSD_INT | R/W | 0 | When high, the overtemperature interrupt is allowed. |
| 3 | EN_THR_INT | R/W | 0 | When high, the THR temperature thresholds interrupt is allowed. |

| Bit No. | Mnemonic | Access | Default | Description |
|---------|------------|--------|---------|--|
| 2 | EN_BAT_INT | R/W | 0 | When high, the battery voltage thresholds interrupt is allowed. |
| 1 | EN_CHG_INT | R/W | 0 | When high, the charger mode change interrupt is allowed. |
| 0 | EN_VIN_INT | R/W | 0 | When high, the VINx pin voltage thresholds interrupt is allowed. |

Table 25. Interrupt Active, Register Address 0x0A Bit Descriptions

| Bit No. | Mnemonic | Access | Default | Description |
|---------|---------------|--------|---------|--|
| 7 | IND_PEAK_INT | R | 0 | When high, this bit indicates an interrupt caused by an inductor peak current limit. |
| 6 | THERM_LIM_INT | R | 0 | When high, this bit indicates an interrupt caused by isothermal charging. |
| 5 | WD_INT | R | 0 | When high, this bit indicates an interrupt caused by the watchdog alarm. The watchdog timer expires within 2 sec or 4 sec depending on the WDPERIOD setting of 32 sec or 64 sec, respectively. |
| 4 | TSD_INT | R | 0 | When high, this bit indicates an interrupt caused by an overtemperature fault. |
| 3 | THR_INT | R | 0 | When high, this bit indicates an interrupt caused by THR temperature thresholds. |
| 2 | BAT_INT | R | 0 | When high, this bit indicates an interrupt caused by battery voltage thresholds. |
| 1 | CHG_INT | R | 0 | When high, this bit indicates an interrupt caused by a charger mode change. |
| 0 | VIN_INT | R | 0 | When high, this bit indicates an interrupt caused by VINx voltage thresholds. |

Table 26. Charger Status 1, Register Address 0x0B Bit Descriptions

| Bit No. | Mnemonic | Access | Default | Description |
|---------|---------------------|--------|----------------|---|
| 7 | VIN_OV | R | Not applicable | When high, this bit indicates that the voltage at the VINx pins exceeds V_{VIN_OV} . |
| 6 | VIN_OK | R | Not applicable | When high, this bit indicates that the voltage at the VINx pins exceeds V_{VIN_OK} . |
| 5 | VIN_ILIM | R | Not applicable | When high, this bit indicates that the current into a VINx pin is limited by the high voltage blocking FET and the charger is not running at the full programmed I_{CHG} . |
| 4 | THERM_LIM | R | Not applicable | When high, this bit indicates that the charger is not running at the full programmed I_{CHG} but is limited by the die temperature. |
| 3 | CHDONE | R | Not applicable | When high, this bit indicates the end of charge cycle has been reached. This bit latches on, in that it does not reset to low when the V_{RCH} threshold is breached. |
| [2:0] | CHARGER_STATUS[2:0] | R | Not applicable | Charger status bus. 000 = off. 001 = trickle charge. 010 = fast charge (CC mode). 011 = fast charge (CV mode). 100 = charge complete. 101 = suspend. 110 = trickle or fast charge timer expired. 111 = battery detection. |

Table 27. Charger Status Register 2, Register Address 0x0C Bit Descriptions

| Bit No. | Mnemonic | Access | Default | Description |
|---------|---------------------|--------|----------------|--|
| [7:5] | THR_STATUS[2:0] | R | Not applicable | THR pin status. 000 = off. 001 = battery cold. 010 = battery cool. 011 = battery warm. 100 = battery hot. 111 = thermistor OK. |
| 4 | IPK_STAT | R | Not applicable | Peak current limit status bit. Set high if four or more peak inductor current limits are reached in succession. |
| 3 | Not Used | R | Not applicable | |
| [2:0] | BATTERY_STATUS[2:0] | R | | Battery status bus. 000 = battery monitor off. 001 = no battery. 010 = $BAT_SNS < V_{TRK}$. 011 = $V_{TRK} \leq BAT_SNS < V_{WEAK}$. 100 = $BAT_SNS \geq V_{WEAK}$. |

Table 28. Fault Register, Register Address 0x0D Bit Descriptions¹

| Bit No. | Mnemonic | Access | Default | Description |
|---------|--------------|--------|---------|---|
| [7:4] | Not Used | | | |
| 3 | BAT_SHR | R/W | 0 | When high, a battery short detection has occurred. |
| 2 | IND_PEAK_INT | R/W | 0 | When high, an inductor peak current-limit fault has occurred. |
| 1 | TSD 130°C | R/W | 0 | When high, the overtemperature (lower) fault has occurred. |
| 0 | TSD 140°C | R/W | 0 | When high, the overtemperature fault has occurred. |

¹ To reset the fault bits in the fault register, cycle power on VINx or write high to the corresponding I²C bit.

Table 29. Battery Short, Register Address 0x10 Bit Descriptions

| Bit No. | Mnemonic | Access | Default | Description |
|---------|---------------|--------|--------------|--|
| [7:5] | TBAT_SHR[2:0] | R/W | 100 = 30 sec | Battery short timeout timer: 000 = 1 sec 001 = 2 sec 010 = 4 sec 011 = 10 sec 100 = 30 sec 101 = 60 sec 110 = 120 sec 111 = 180 sec |
| [4:3] | Not used | R/W | | |
| [2:0] | VBAT_SHR[2:0] | R/W | 100 = 2.4 V | Battery short voltage threshold level: 000 = 2.0 V 001 = 2.1 V 010 = 2.2 V 011 = 2.3 V 100 = 2.4 V 101 = 2.5 V 110 = 2.6 V 111 = 2.7 V |

APPLICATIONS INFORMATION

EXTERNAL COMPONENTS

Inductor Selection

The high switching frequency of the ADP5065 buck converter allows for the selection of small chip inductors. Suggested inductors are shown in Table 33.

The peak-to-peak inductor current ripple is calculated using the following equation:

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where:

V_{OUT} is the ISO_Sx node output voltage.

V_{IN} is the converter input voltage at the CFILT node.

f_{SW} is the switching frequency.

L is the inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current. The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{CHG} + I_{LOAD(MAX)} + \frac{I_{RIPPLE}}{2}$$

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal dc resistance (DCR). Larger sized inductors have smaller DCR, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the bucks are high switching frequency dc-to-dc converters, shielded ferrite core material is recommended for its low core losses and low EMI.

ISO_Sx (V_{OUT}) and ISO_Bx Capacitor Selection

To safely obtain stable operation of the ADP5065, the ISO_Sx and ISO_Bx effective capacitance (including temperature and dc bias effects) must not be less than 10 μ F at any point during operation. The combined effective capacitance of the ISO_Sx capacitor and the system capacitance must not exceed 50 μ F at any point during operation.

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate enough to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL)$$

where:

C_{EFF} is the effective capacitance at the operating voltage.

$TEMPCO$ is the worst-case capacitor temperature coefficient.

TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient ($TEMPCO$) over -40°C to $+85^{\circ}\text{C}$ is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} is 16 μ F at 4.2 V, as shown in Figure 39.

Substituting these values in the equation yields

$$C_{EFF} = 16 \mu\text{F} \times (1 - 0.15) \times (1 - 0.1) \approx 12.24 \mu\text{F}$$

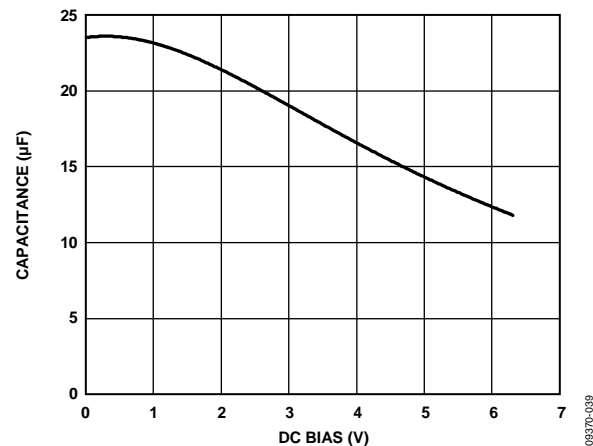


Figure 39. Murata GRM31CR60J226ME19C DC Characteristic

To guarantee the performance of the charger in various operation modes including trickle charge, constant current charge, and constant voltage charge, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using the following equation:

$$V_{RIPPLE} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}} \approx \frac{V_{IN}}{(2\pi \times f_{SW})^2 \times L \times C_{OUT}}$$

Capacitors with lower effective series resistance (ESR) are preferable to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}}$$

VINx Capacitor Selection

According to the USB 2.0 specification, USB peripherals have a detectable change in capacitance on VBUS when they are attached. The peripheral device VBUS bypass capacitance must be at least 1 μF but not larger than 10 μF . The combined capacitance for the VINx and CFILT pins must not exceed 10 μF at any temperature or dc bias condition. Suggestions for a VINx capacitor is given in Table 32.

CFILT Capacitor Selection

CFILT pin serves the ADP5065 as the step-down dc-to-dc converter input capacitor. Maximum input capacitor current is calculated using the following equation:

$$I_{CIN} \geq I_{LOAD+CHG(MAX)} \sqrt{\frac{V_{ISO_S} (V_{CFILT} - V_{ISO_S})}{V_{CFILT}}}$$

To minimize supply noise, place the input capacitor as close as possible to the CFILT pin of the charger. As with the output capacitor, a low ESR capacitor is recommended.

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 2 μF and a maximum of 5 μF . A list of suggested capacitors is shown in Table 31.

Table 30. ISO_Sx and ISO_Bx Capacitor Suggestions

| Vendor | Part Number | Value | Voltage | Size |
|-------------|-------------------|------------------|---------|------|
| Murata | GRM31CR61A226KE19 | 22 μF | 10 V | 1206 |
| Murata | GRM31CR60J226ME19 | 22 μF | 6.3 V | 1206 |
| TDK | C3216X5R0J226M | 22 μF | 6.3 V | 1206 |
| TAIYO-YUDEN | JMK316ABJ226KL | 22 μF | 6.3 V | 1206 |

Table 31. CFILT Capacitor Suggestions

| Vendor | Part Number | Value | Voltage | Size |
|-------------|-------------------|-------------------|---------|------|
| Murata | GRM219R61C475KE15 | 4.7 μF | 16 V | 0805 |
| Murata | GRM188R60J475ME84 | 4.7 μF | 6.3 V | 0603 |
| TDK | C1608X5R0J475K | 4.7 μF | 6.3 V | 0603 |
| TAIYO-YUDEN | JMK107ABJ106MA | 10 μF | 6.3 V | 0603 |

Table 32. VINx Capacitor Suggestions

| Vendor | Part Number | Value | Voltage | Size |
|-------------|-------------------|-------------------|---------|------|
| Murata | GRM21BR71E225KA73 | 2.2 μF | 25 | 0805 |
| Murata | GRM188R61E225KA12 | 2.2 μF | 25 | 0603 |
| TDK | C1608X5R1E225K | 2.2 μF | 25 | 0603 |
| TAIYO-YUDEN | TMK107ABJ225MA | 2.2 μF | 25 | 0603 |

Table 33. 1.0 μH Inductor Suggestions

| Vendor | Part Number | Saturation Current L –30% Drop | DCR (m Ω) | Size Max L x W x H (mm) |
|-----------|---------------|-----------------------------------|-------------------|-------------------------|
| Murata | LQH32PN1R0NNO | 2.3 A | 45 | 3.5 x 2.7 x 1.7 |
| Coilcraft | XFL3010-102ME | 2.4 A | 43 | 3.2 x 3.2 x 1.1 |

PCB LAYOUT GUIDELINES

Poor layout can affect ADP5065 performance, causing electro-magnetic interference (EMI) and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following guidelines:

- Place the inductor, input capacitor, and output capacitor close to the IC using short tracks. These components carry high switching frequencies, and large tracks act as antennas.

- Route the output voltage path away from both the inductor and SWxnode to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

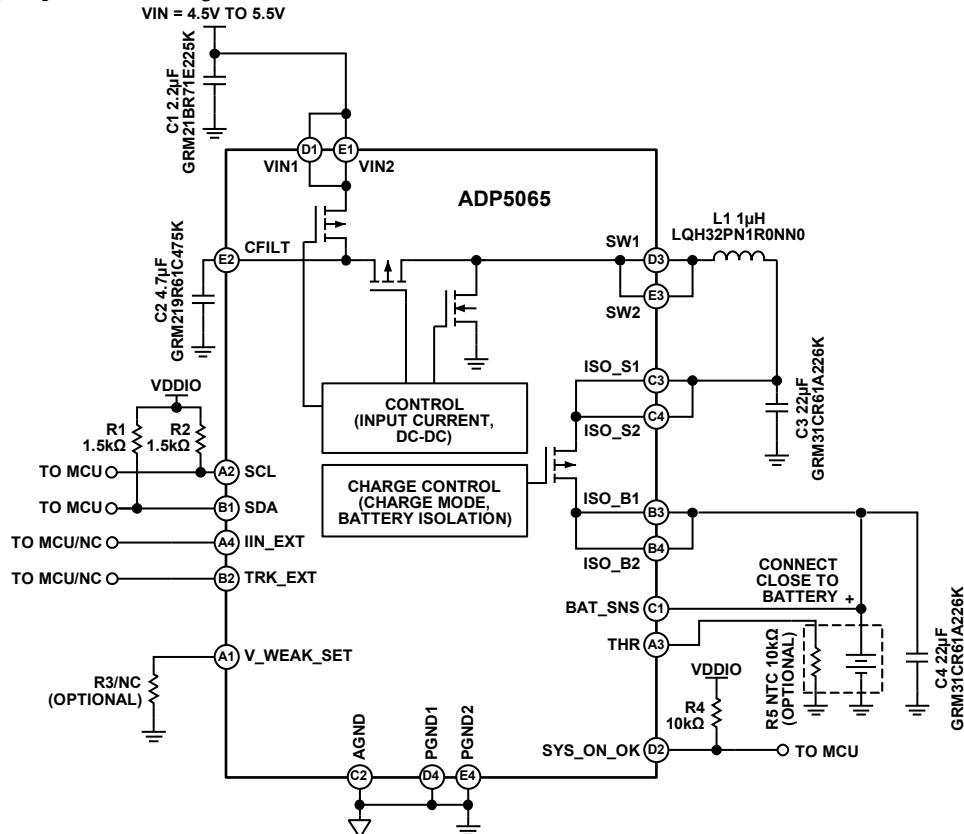


Figure 40. Reference Circuit Diagram

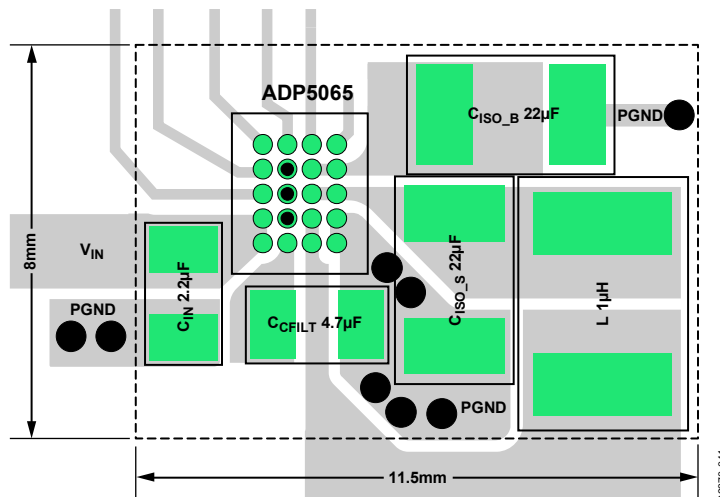


Figure 41. PCB Layout Suggestion

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The ADP5065 is a highly efficient USB compliant charger. However, if the device operates at high ambient temperatures and maximum current charging and loading conditions, the junction temperature can reach the maximum allowable operating limit (125°C).

When the temperature exceeds 140°C, the ADP5065 turns off allowing the device to cool down. When the die temperature falls below 110°C and the TSD 140°C fault bit in Register 0x0D is cleared by an I²C write, the ADP5065 resumes normal operation.

This section provides guidelines to calculate the power dissipated in the device and ensure that the ADP5065 operates below the maximum allowable junction temperature.

The output power of the ADP5065 charger is given by

$$P_{OUT} = V_{ISO_S} \times I_{LOAD} + V_{ISO_B} \times I_{CHG} \quad (1)$$

where:

P_{OUT} is the total output power to the system and battery.

V_{ISO_S} is the ISO_Sx pin voltage.

I_{LOAD} is the load current from ISO_Sx node.

V_{ISO_B} is the battery voltage.

I_{CHG} is the charge current.

The efficiency of the ADP5065 is given by

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\% \quad (2)$$

where:

η is the efficiency.

P_{IN} is the input power.

Power loss is given by

$$P_{LOSS} = P_{IN} - P_{OUT} \quad (3a)$$

or

$$P_{LOSS} = P_{OUT} (1 - \eta) / \eta \quad (3b)$$

Power dissipation can be calculated in several ways. The most intuitive and practical is to measure the power dissipated at the input and both outputs (ISO_Sx and ISO_Bx). Perform the measurements at the worst-case conditions (voltages, currents, and temperature). The difference between input and output power is dissipated in the device and the inductor. Use Equation 5 to derive the power lost in the inductor and, from this, use Equation 4 to calculate the power dissipation in the ADP5065 charger.

A second method to estimate the power dissipation uses the system voltage and charging efficiency curves provided for the ADP5065. When the efficiency is known, use Equation 3b to derive the total power lost in the dc-to-dc converter, isolation FET and inductor; use Equation 5 to derive the power lost in the inductor, and then calculate the power dissipation in the buck converter using Equation 4.

Note that the ADP5065 efficiency curves are typical values and may not be provided for all possible combinations of V_{IN} , V_{OUT} , and I_{OUT} . To account for these variations, it is necessary to include a safety margin when calculating the power dissipated in the charger.

CHARGER POWER DISSIPATION

The power loss of the step-down charger is approximated by

$$P_{LOSS} = P_{DCHG} + P_L \quad (4)$$

where:

P_{DCHG} is the power dissipation of the ADP5065 charger.

P_L is the inductor power losses.

The inductor losses are external to the device, and they do not have any effect on the die temperature. Equation 5 estimates the inductor losses without core losses. Some inductor manufacturers provide web tools to estimate power inductor core losses based on inductor type, switching frequency, and ripple current. At a switching frequency of 3 MHz, the core losses can add inductor losses significantly.

$$P_L \approx I_{OUT(RMS)}^2 \times DCR_L \quad (5)$$

where:

DCR_L is the inductor series resistance.

$I_{OUT(RMS)}$ is the summary of rms load current and charging current ($I_{LOAD(RMS)} + I_{CHG}$).

$$I_{OUT(RMS)} = I_{OUT} \times \sqrt{1 + \frac{r}{12}} \quad (6)$$

where r is the normalized inductor ripple current.

$$r = V_{OUT} \times (1 - D) / (I_{OUT} \times L \times f_{SW}) \quad (7)$$

where:

L is the inductance.

f_{SW} is the switching frequency.

D is the duty cycle.

$$D = V_{OUT} / V_{IN} \quad (8)$$

JUNCTION TEMPERATURE

In cases where the ambient temperature, T_A , is known, the thermal resistance parameter, θ_{JA} , can be used to estimate the junction temperature rise. T_J is calculated from T_A and P_D using the formula

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (9)$$

The typical θ_{JA} value for the 20-bump WLCSP is 46.8°C/W (see Table 5). A very important factor to consider is that θ_{JA} is based on a 4-layer, 4 in × 3 in, 2.5 oz copper board as per JEDEC standard, and real applications may use different sizes and layers. It is important to maximize the copper to remove the heat from the device. Copper exposed to air dissipates heat better than copper used in the inner layers.

When designing an application for a particular ambient temperature range, calculate the expected ADP5065 power dissipation (P_D). From this power calculation, the junction temperature, T_J , can be estimated using Equation 9.

Maximum junction temperature (T_J) can also be calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \theta_{JB}) \quad (10)$$

where θ_{JB} is the junction-to-board thermal resistance.

The typical value for the 20-bump WLCSP is 9.2°C/W (see Table 5). θ_{JB} is based on a 4-layer, 4 in × 3 in, 2.5 oz copper board, as per the JEDEC standard.

For a WLCSP device, where possible, remove heat from every current carrying bump (PGND_x, VIN_x, SW_x, ISO_S_x, and ISO_B_x). For example, thermal vias to the board power planes can be placed close to these pins, where available.

The reliable operation of the charger can be achieved only if the estimated die junction temperature of the ADP5065 (Equation 9) is less than 125°C. Reliability and mean time between failures (MTBF) are highly affected by increasing the junction temperature. Additional information about product reliability is available in the *ADI Reliability Handbook* at the following URL: www.analog.com/reliability_handbook.

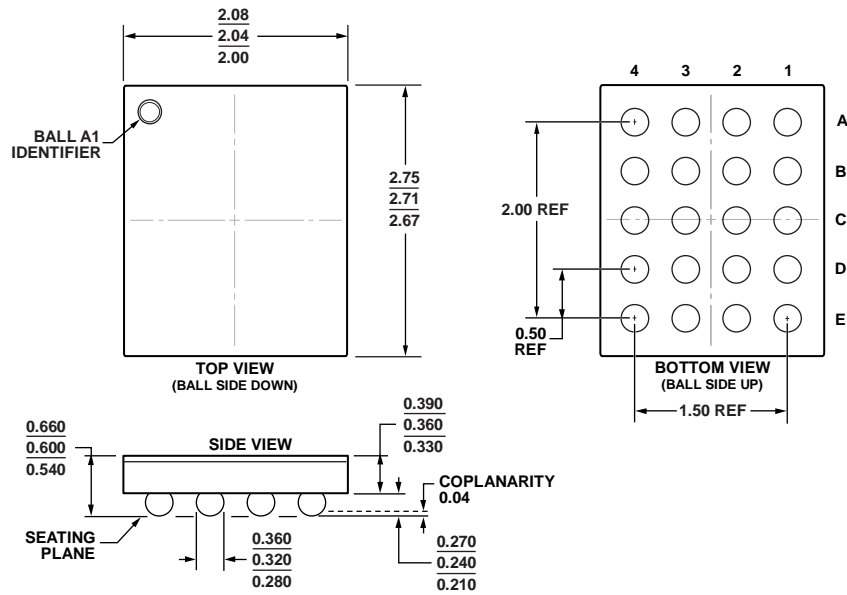
FACTORY-PROGRAMMABLE OPTIONS

Table 34. ADP5065 Fuse-Selectable Trim Options

| Parameter | Value | ADP5065ACBZ-1-R7 Trim Setting |
|---------------------|----------------|-------------------------------|
| NTC Thermistor Type | 10 k Ω | 10 k Ω |
| | 100 k Ω | |
| NTC Beta | 3150 | 3350 |
| | 3350 | |
| | 3500 | |
| | 3650 | |
| | 3850 | |
| | 4000 | |
| | 4200 | |
| 4400 | | |

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS



10-30-2012-A

Figure 42. 20-Ball Wafer Level Chip Scale Package [WLCSP] (CB-20-8)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range (Junction) | Package Description | Package Option |
|--------------------|------------------------------|--|----------------|
| ADP5065ACBZ-1-R7 | -40°C to +125°C | 20-Ball Wafer Level Chip Scale Package [WLCSP] | CB-20-8 |
| ADP5065CB-EVALZ | | ADP5065 Evaluation Board | |

¹ Z = RoHS Compliant Part.

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).