

## 1K x 8 Dual-Port Static RAM

### Features

- True dual-ported memory cells, which allow simultaneous reads of the same memory location
- 1K x 8 organization
- 0.65 micron CMOS for optimum speed and power
- High speed access: 15 ns
- Low operating power:  $I_{CC} = 110$  mA (maximum)
- Fully asynchronous operation
- Automatic power down
- Master CY7C130/130A/CY7C131/131A easily expands data bus width to 16 or more bits using slave CY7C140/CY7C141
- $\overline{BUSY}$  output flag on CY7C130/130A/CY7C131/131A;  $\overline{BUSY}$  input on CY7C140/CY7C141
- $\overline{INT}$  flag for port-to-port communication
- Available in 48-pin DIP (CY7C130/130A/140), 52-pin PLCC, 52-pin TQFP
- Pb-free packages available

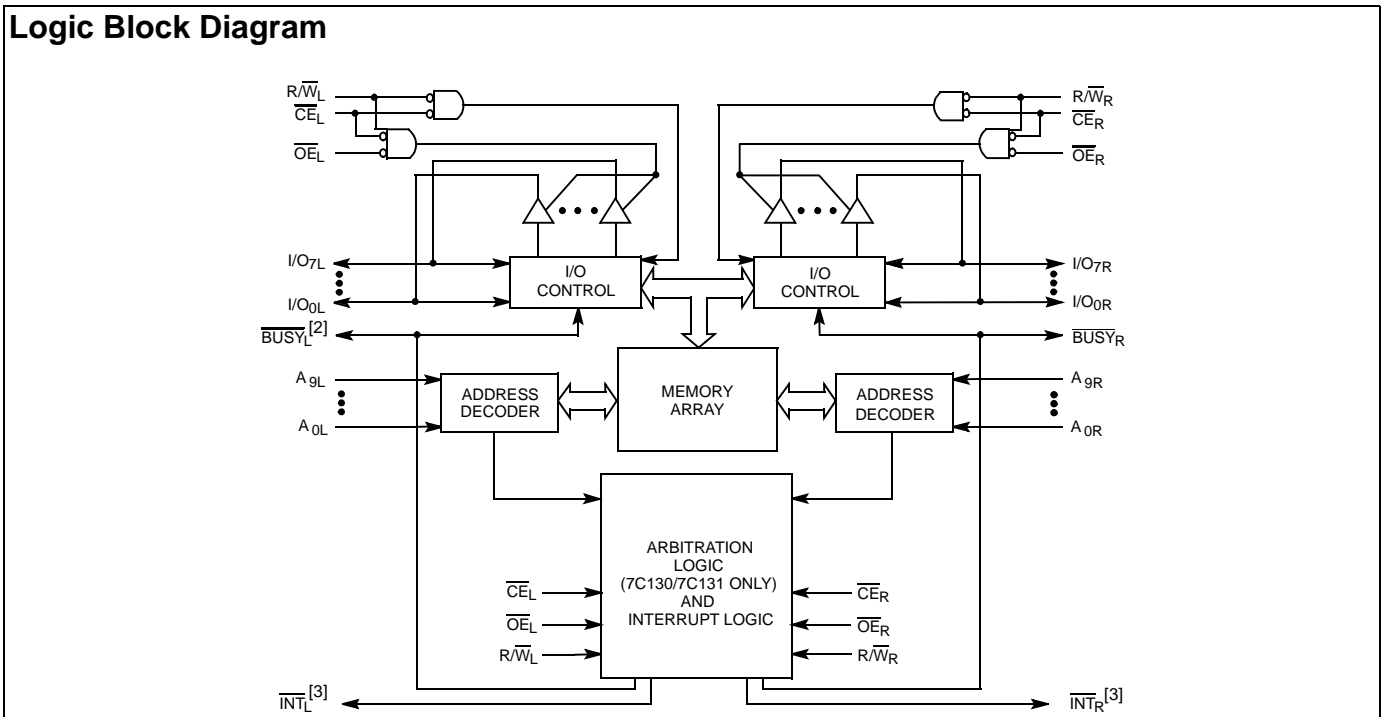
### Functional Description

The CY7C130/130A/CY7C131/131A/CY7C140<sup>[1]</sup> and CY7C141 are high speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/130A/ CY7C131/131A can be used as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multi-processor designs.

Each port has independent control pins; chip enable ( $\overline{CE}$ ), write enable (R/W), and output enable ( $\overline{OE}$ ). Two flags are provided on each port,  $\overline{BUSY}$  and  $\overline{INT}$ .  $\overline{BUSY}$  signals that the port is trying to access the same location currently being accessed by the other port.  $\overline{INT}$  is an interrupt flag indicating that data is placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power down feature is controlled independently on each port by the chip enable ( $\overline{CE}$ ) pins.

The CY7C130/130A and CY7C140 are available in 48-pin DIP. The CY7C131/131A and CY7C141 are available in 52-pin PLCC, 52-pin Pb-free PLCC, 52-pin PQFP, and 52-pin Pb-free PQFP.

### Logic Block Diagram



#### Notes

1. CY7C130 and CY7C130A are functionally identical; CY7C131 and CY7C131A are functionally identical.
2. CY7C130/130A/CY7C131/131A (Master):  $\overline{BUSY}$  is open drain output and requires pull-up resistor.  
CY7C140/CY7C141 (Slave):  $\overline{BUSY}$  is input.
3. Open drain outputs: pull-up resistor required.

## Pin Configurations

Figure 1. Pin Diagram - DIP (Top View)

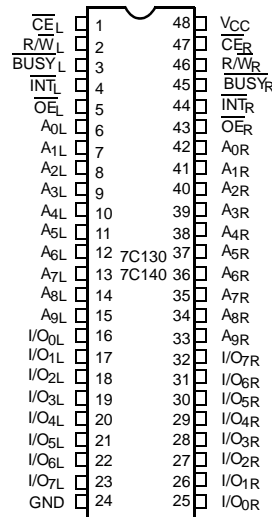


Figure 2. Pin Diagram - PLCC (Top View)

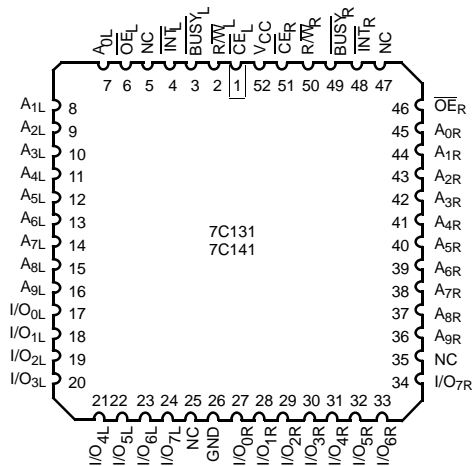
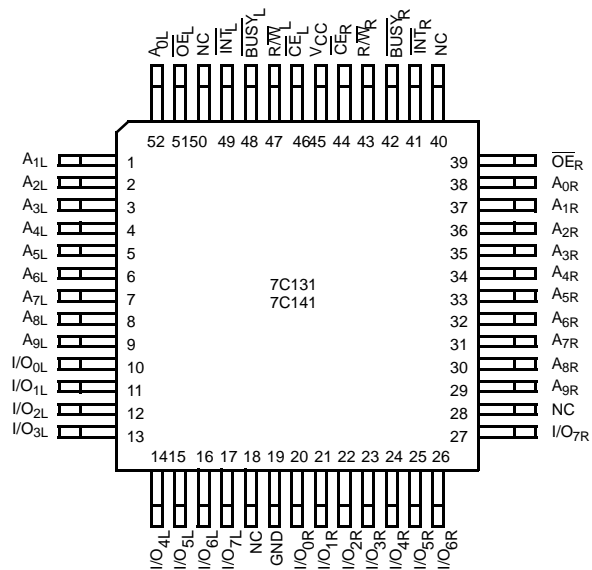


Figure 3. Pin Diagram - PQFP (Top View)



## Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L}-A_{11/12L}$	$A_{0R}-A_{11/12R}$	Address
$I/O_{0L}-I/O_{15/17L}$	$I/O_{0R}-I/O_{15/17R}$	Data Bus Input/Output
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$V_{CC}$		Power
GND		Ground

## Selection Guide

Parameter		7C131-15 <sup>[4]</sup> 7C131A-15 7C141-15	7C131-25 <sup>[4]</sup> 7C141-25	7C130-30 7C130A-30 7C131-30 7C140-30 7C141-30	7C130-35 7C131-35 7C140-35 7C141-35	7C130-45 7C131-45 7C140-45 7C141-45	7C130-55 7C131-55 7C140-55 7C141-55	Unit
Maximum Access Time		15	25	30	35	45	55	ns
Maximum Operating Current	Com/I/Ind	190	170	170	120	120	110	mA
Maximum Standby Current	Com/I/Ind	75	65	65	45	45	35	mA

Shaded areas contain preliminary information.

### Note

4. 15 and 25 ns version available only in PLCC/PQFP packages.

## Maximum Ratings<sup>[5]</sup>

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 48 to Pin 24) .....	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State .....	-0.5V to +7.0V

DC Input Voltage .....	-3.5V to +7.0V
Output Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage .....	>2001V (per MIL-STD-883, Method 3015)
Latch Up Current .....	>200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military <sup>[6]</sup>	-55°C to +125°C	5V ± 10%

## Electrical Characteristics Over the Operating Range<sup>[7]</sup>

Parameter	Description	Test Conditions	7C131-15 <sup>[4]</sup> 7C131A-15 7C141-15		7C130-30 <sup>[4]</sup> 7C130A-30 7C131-25,30 7C140-30 7C141-25,30		7C130-35,45 7C131-35,45 7C140-35,45 7C141-35,45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
			V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4	
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 4.0 mA		0.4		0.4		0.4		0.4	V
		I <sub>OL</sub> = 16.0 mA <sup>[8]</sup>		0.5		0.5		0.5		0.5	V
V <sub>IH</sub>	Input HIGH Voltage		2.2		2.2		2.2		2.2		V
V <sub>IL</sub>	Input LOW Voltage			0.8		0.8		0.8		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[9, 10]</sup>	V <sub>CC</sub> = Max, V <sub>OUT</sub> = GND		-350		-350		-350		-350	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	CE = V <sub>IL</sub> , Outputs Open, f = f <sub>MAX</sub> <sup>[11]</sup>	Com'l	190		170		120		110	mA
I <sub>SB1</sub>	Standby Current Both Ports, TTL Inputs	CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub> <sup>[11]</sup>	Com'l	75		65		45		35	mA
I <sub>SB2</sub>	Standby Current One Port, TTL Inputs	CE <sub>L</sub> or CE <sub>R</sub> ≥ V <sub>IH</sub> , Active Port Outputs Open f = f <sub>MAX</sub> <sup>[11]</sup>	Com'l	135		115		90		75	mA
I <sub>SB3</sub>	Standby Current Both Ports, CMOS Inputs	Both Ports CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0	Com'l	15		15		15		15	mA
I <sub>SB4</sub>	Standby Current One Port, CMOS Inputs	One Port CE <sub>L</sub> or CE <sub>R</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[11]</sup>	Com'l	125		105		85		70	mA

Shaded areas contain preliminary information.

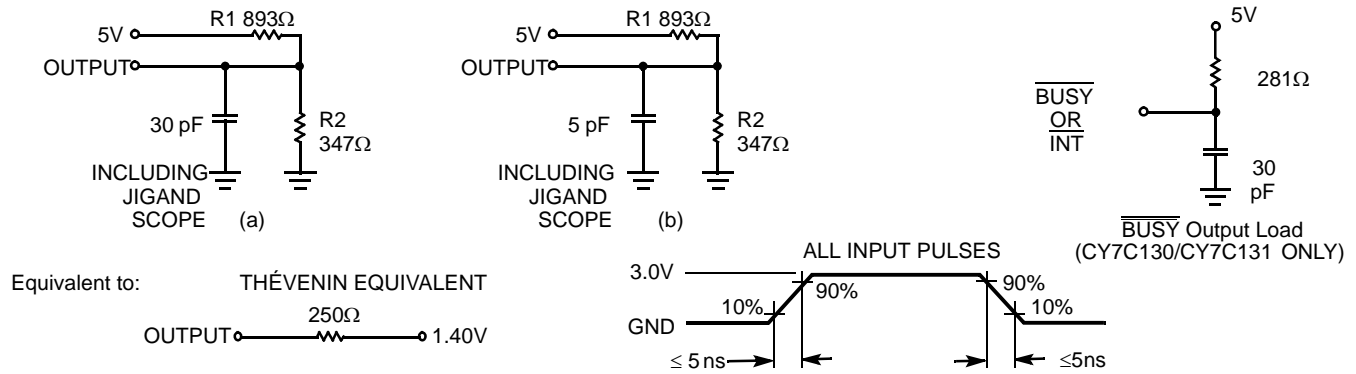
### Notes

- The voltage on any input or I/O pin cannot exceed the power pin during power up.
- T<sub>A</sub> is the "instant on" case temperature
- See the last page of this specification for Group A subgroup testing information.
- BUSY and INT pins only.
- Duration of the short circuit should not exceed 30 seconds.
- This parameter is guaranteed but not tested.
- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency of read cycle of 1/t<sub>RC</sub> and using AC Test Waveforms input levels of GND to 3V.

### Capacitance<sup>[10]</sup>

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{V}$	15	pF
$C_{OUT}$	Output Capacitance		10	pF

**Figure 4. AC Test Loads and Waveforms**



**Switching Characteristics** Over the Operating Range<sup>[7, 12]</sup>

Parameter	Description	7C131-15 <sup>[4]</sup> 7C131A-15 7C141-15		7C130-25 <sup>[4]</sup> 7C131-25 7C140-25 7C141-25		7C130-30 7C130A-30 7C131-30 7C140-30 7C141-30		Unit
		Min	Max	Min	Max	Min	Max	
<b>Read Cycle</b>								
t <sub>RC</sub>	Read Cycle Time	15		25		30		ns
t <sub>AA</sub>	Address to Data Valid <sup>[13]</sup>		15		25		30	ns
t <sub>OHA</sub>	Data Hold from Address Change	0		0		0		ns
t <sub>ACE</sub>	CE LOW to Data Valid <sup>[13]</sup>		15		25		30	ns
t <sub>DOE</sub>	OE LOW to Data Valid <sup>[13]</sup>		10		15		20	ns
t <sub>LZOE</sub>	OE LOW to Low Z <sup>[10, 14, 15]</sup>	3		3		3		ns
t <sub>HZOE</sub>	OE HIGH to High Z <sup>[10, 14, 15]</sup>		10		15		15	ns
t <sub>LZCE</sub>	CE LOW to Low Z <sup>[10, 14, 15]</sup>	3		5		5		ns
t <sub>HZCE</sub>	CE HIGH to High Z <sup>[10, 14, 15]</sup>		10		15		15	ns
t <sub>PU</sub>	CE LOW to Power Up <sup>[10]</sup>	0		0		0		ns
t <sub>PD</sub>	CE HIGH to Power Down <sup>[10]</sup>		15		25		25	ns
<b>Write Cycle<sup>[16]</sup></b>								
t <sub>WC</sub>	Write Cycle Time	15		25		30		ns
t <sub>SCE</sub>	CE LOW to Write End	12		20		25		ns
t <sub>AW</sub>	Address Setup to Write End	12		20		25		ns
t <sub>HA</sub>	Address Hold from Write End	2		2		2		ns
t <sub>SA</sub>	Address Setup to Write Start	0		0		0		ns
t <sub>PWE</sub>	R/W Pulse Width	12		15		25		ns
t <sub>SD</sub>	Data Setup to Write End	10		15		15		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>HZWE</sub>	R/W LOW to High Z <sup>[15]</sup>		10		15		15	ns
t <sub>LZWE</sub>	R/W HIGH to Low Z <sup>[15]</sup>	0		0		0		ns

Shaded areas contain preliminary information.

**Notes**

12. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
13. AC Test Conditions use V<sub>OH</sub> = 1.6V and V<sub>OL</sub> = 1.4V.
14. At any given temperature and voltage condition for any given device, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> and t<sub>HZOE</sub> is less than t<sub>LZOE</sub>.
15. t<sub>LZCE</sub>, t<sub>LZWE</sub>, t<sub>HZOE</sub>, t<sub>LZOE</sub>, t<sub>HZCE</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
16. The internal write time of the memory is defined by the overlap of CS LOW and R/W LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

**Switching Characteristics** Over the Operating Range<sup>[7, 12]</sup> (continued)

Parameter	Description	7C131-15 <sup>[4]</sup> 7C131A-15 7C141-15		7C130-25 <sup>[4]</sup> 7C131-25 7C140-25 7C141-25		7C130-30 7C130A-30 7C131-30 7C140-30 7C141-30		Unit
		Min	Max	Min	Max	Min	Max	
<b>Busy/Interrupt Timing</b>								
t <sub>BLA</sub>	BUSY LOW from Address Match		15		20		20	ns
t <sub>BHA</sub>	BUSY HIGH from Address Mismatch <sup>[17]</sup>		15		20		20	ns
t <sub>BLC</sub>	BUSY LOW from CE LOW		15		20		20	ns
t <sub>BHC</sub>	BUSY HIGH from CE HIGH <sup>[17]</sup>		15		20		20	ns
t <sub>PS</sub>	Port Set Up for Priority	5		5		5		ns
t <sub>WB</sub> <sup>[18]</sup>	R/W LOW after BUSY LOW	0		0		0		ns
t <sub>WH</sub>	R/W HIGH after BUSY HIGH	13		20		30		ns
t <sub>BDD</sub>	BUSY HIGH to Valid Data		15		25		30	ns
t <sub>DDD</sub>	Write Data Valid to Read Data Valid		Note 19		Note 19		Note 19	ns
t <sub>WDD</sub>	Write Pulse to Data Delay		Note 19		Note 19		Note 19	ns
<b>Interrupt Timing</b>								
t <sub>WINS</sub>	R/W to INTERRUPT Set Time		15		25		25	ns
t <sub>EINS</sub>	CE to INTERRUPT Set Time		15		25		25	ns
t <sub>INS</sub>	Address to INTERRUPT Set Time		15		25		25	ns
t <sub>OINR</sub>	OE to INTERRUPT Reset Time <sup>[17]</sup>		15		25		25	ns
t <sub>EINR</sub>	CE to INTERRUPT Reset Time <sup>[17]</sup>		15		25		25	ns
t <sub>INR</sub>	Address to INTERRUPT Reset Time <sup>[17]</sup>		15		25		25	ns

Shaded areas contain preliminary information.

**Notes**

- 17. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
- 18. CY7C140/CY7C141 only.
- 19. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:  
 BUSY on Port B goes HIGH.  
 Port B's address is toggled.  
 CE for Port B is toggled.  
 R/W for Port B is toggled during valid read.

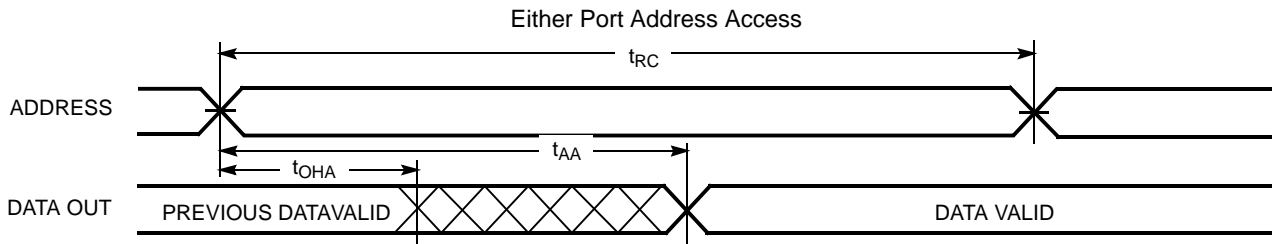
**Switching Characteristics** Over the Operating Range<sup>[7,12]</sup>

Parameter	Description	7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min	Max	Min	Max	Min	Max	
<b>Read Cycle</b>								
t <sub>RC</sub>	Read Cycle Time	35		45		55		ns
t <sub>AA</sub>	Address to Data Valid <sup>[13]</sup>		35		45		55	ns
t <sub>OHA</sub>	Data Hold from Address Change	0		0		0		ns
t <sub>ACE</sub>	CE LOW to Data Valid <sup>[13]</sup>		35		45		55	ns
t <sub>DOE</sub>	OE LOW to Data Valid <sup>[13]</sup>		20		25		25	ns
t <sub>LZOE</sub>	OE LOW to Low Z <sup>[10, 14, 15]</sup>	3		3		3		ns
t <sub>HZOE</sub>	OE HIGH to High Z <sup>[10, 14, 15]</sup>		20		20		25	ns
t <sub>LZCE</sub>	CE LOW to Low Z <sup>[10, 14, 15]</sup>	5		5		5		ns
t <sub>HZCE</sub>	CE HIGH to High Z <sup>[10, 14, 15]</sup>		20		20		25	ns
t <sub>PU</sub>	CE LOW to Power Up <sup>[10]</sup>	0		0		0		ns
t <sub>PD</sub>	CE HIGH to Power Down <sup>[10]</sup>		35		35		35	ns
<b>Write Cycle<sup>[16]</sup></b>								
t <sub>WC</sub>	Write Cycle Time	35		45		55		ns
t <sub>SCE</sub>	CE LOW to Write End	30		35		40		ns
t <sub>AW</sub>	Address Setup to Write End	30		35		40		ns
t <sub>HA</sub>	Address Hold from Write End	2		2		2		ns
t <sub>SA</sub>	Address Setup to Write Start	0		0		0		ns
t <sub>PWE</sub>	R/W Pulse Width	25		30		30		ns
t <sub>SD</sub>	Data Setup to Write End	15		20		20		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>HZWE</sub>	R/W LOW to High Z <sup>[15]</sup>		20		20		25	ns
t <sub>LZWE</sub>	R/W HIGH to Low Z <sup>[15]</sup>	0		0		0		ns
<b>Busy/Interrupt Timing</b>								
t <sub>B<sub>LA</sub></sub>	BUSY LOW from Address Match		20		25		30	ns
t <sub>B<sub>HA</sub></sub>	BUSY HIGH from Address Mismatch <sup>[17]</sup>		20		25		30	ns
t <sub>B<sub>LC</sub></sub>	BUSY LOW from CE LOW		20		25		30	ns
t <sub>B<sub>HC</sub></sub>	BUSY HIGH from CE HIGH <sup>[17]</sup>		20		25		30	ns
t <sub>PS</sub>	Port Set Up for Priority	5		5		5		ns
t <sub>W<sub>B</sub></sub> <sup>[18]</sup>	R/W LOW after BUSY LOW	0		0		0		ns
t <sub>W<sub>H</sub></sub>	R/W HIGH after BUSY HIGH	30		35		35		ns
t <sub>B<sub>DD</sub></sub>	BUSY HIGH to Valid Data		35		45		45	ns
t <sub>DD<sub>D</sub></sub>	Write Data Valid to Read Data Valid		Note 19		Note 19		Note 19	ns
t <sub>W<sub>DD</sub></sub>	Write Pulse to Data Delay		Note 19		Note 19		Note 19	ns
<b>Interrupt Timing</b>								
t <sub>W<sub>INS</sub></sub>	R/W to INTERRUPT Set Time		25		35		45	ns
t <sub>E<sub>INS</sub></sub>	CE to INTERRUPT Set Time		25		35		45	ns
t <sub>INS</sub>	Address to INTERRUPT Set Time		25		35		45	ns
t <sub>O<sub>INR</sub></sub>	OE to INTERRUPT Reset Time <sup>[17]</sup>		25		35		45	ns
t <sub>E<sub>INR</sub></sub>	CE to INTERRUPT Reset Time <sup>[17]</sup>		25		35		45	ns
t <sub>INR</sub>	Address to INTERRUPT Reset Time <sup>[17]</sup>		25		35		45	ns

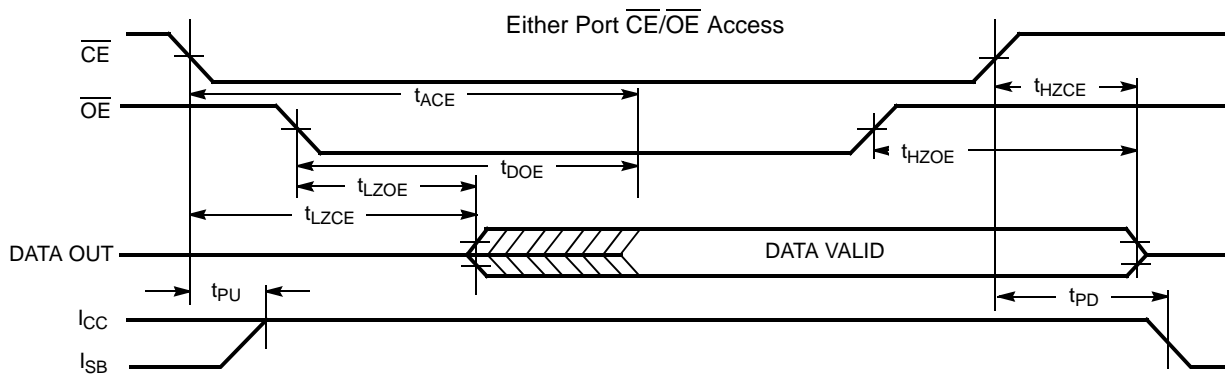


## Switching Waveforms

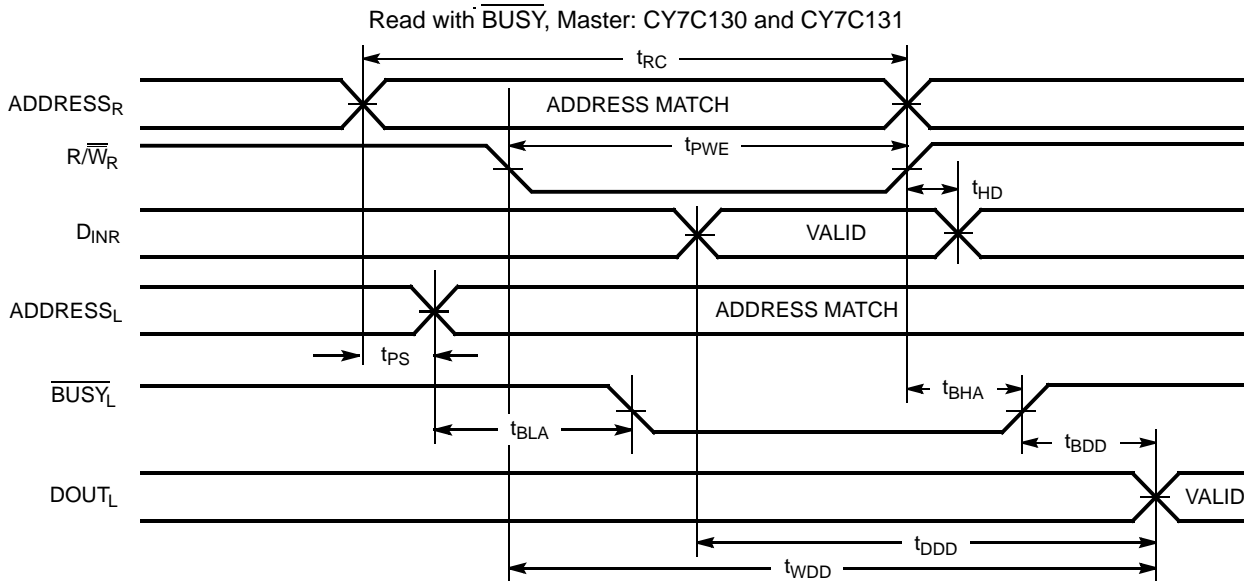
**Figure 5. Read Cycle No. 1<sup>[20, 21]</sup>**



**Figure 6. Read Cycle No. 2<sup>[20, 22]</sup>**



**Figure 7. Read Cycle No. 3<sup>[21]</sup>**



### Notes

20.  $R\overline{W}$  is HIGH for read cycle.
21. Device is continuously selected,  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .
22. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 (OE Three-States Data I/Os—Either Port)<sup>[16, 23]</sup>

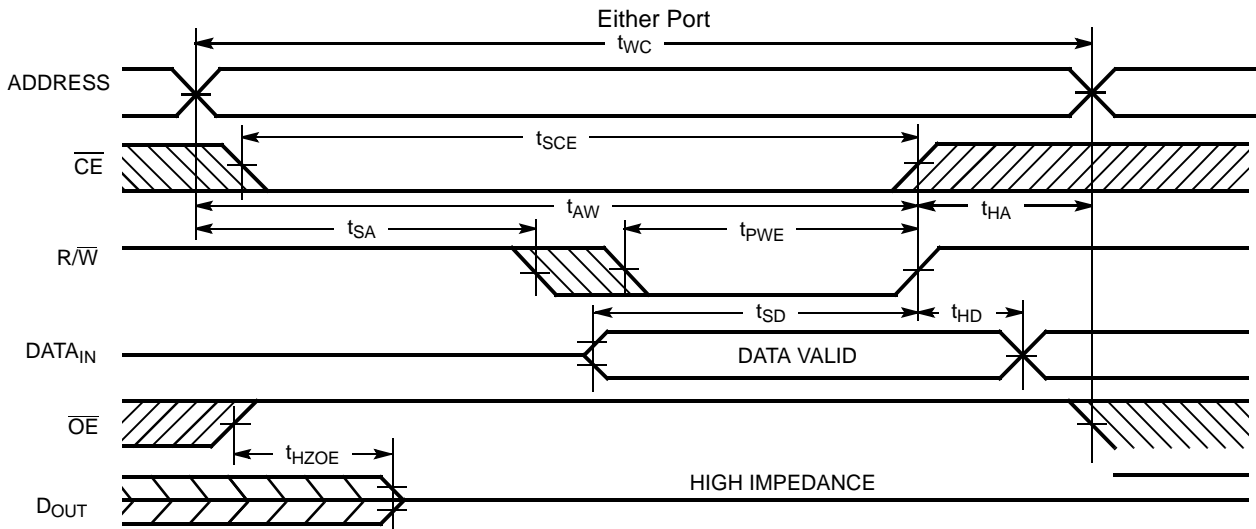
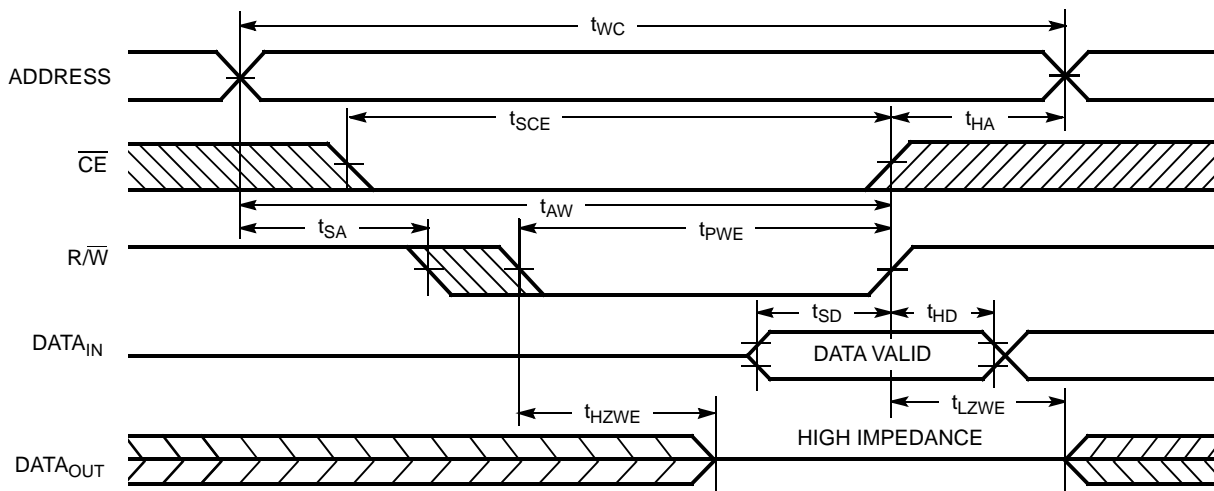


Figure 9. Write Cycle No. 2 (R/W Three-States Data I/Os—Either Port)<sup>[17, 24]</sup>



Notes

23. If  $\overline{OE}$  is LOW during a  $R/\overline{W}$  controlled write cycle, the write pulse width must be the larger of  $t_{PWE}$  or  $t_{HZOE} + t_{SD}$  to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required  $t_{SD}$ .
24. If the  $\overline{CE}$  LOW transition occurs simultaneously with or after the  $R/\overline{W}$  LOW transition, the outputs remain in the high impedance state.

Switching Waveforms (continued)

Figure 10. Busy Timing Diagram No. 1 ( $\overline{CE}$  Arbitration)

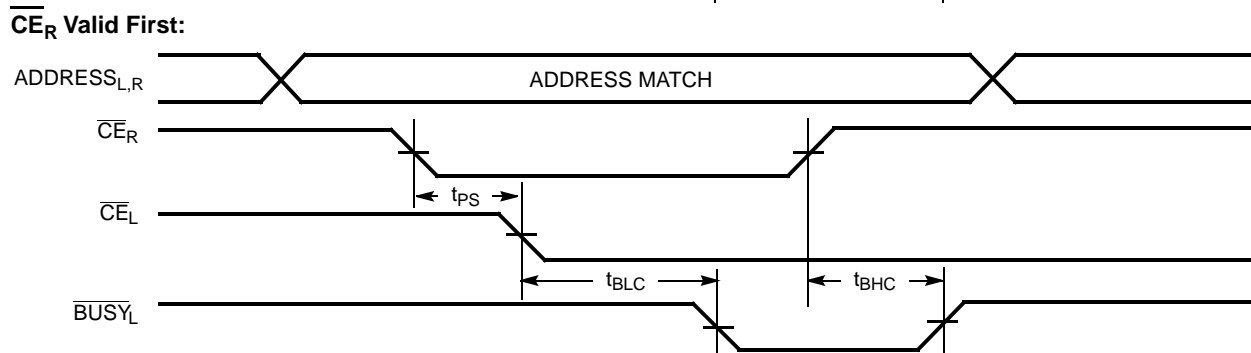
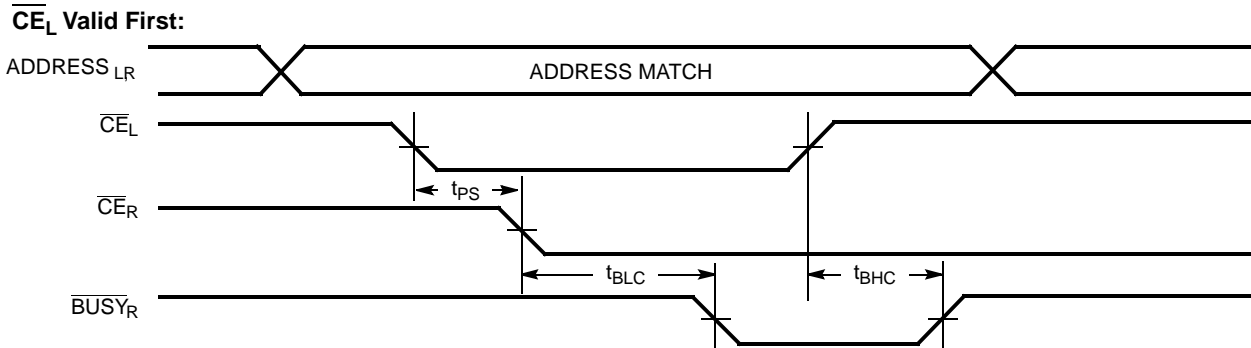
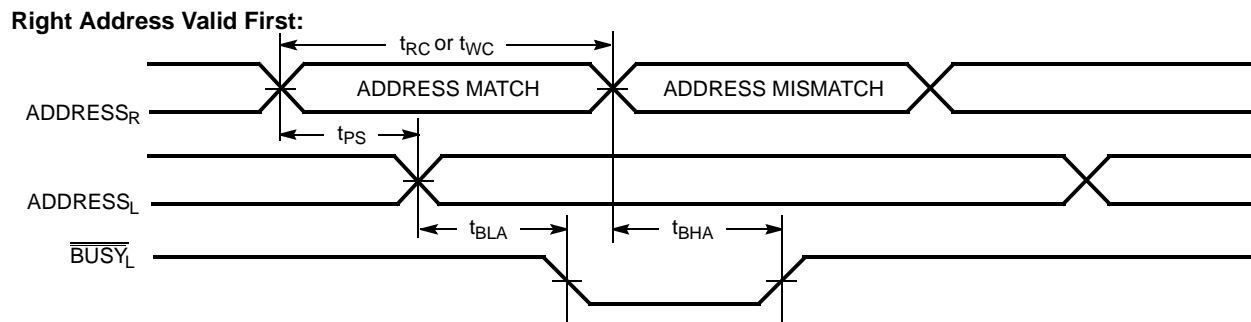
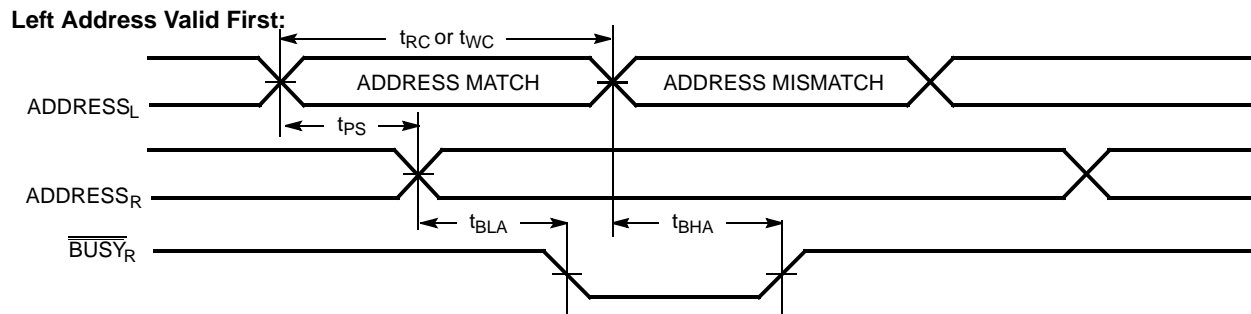


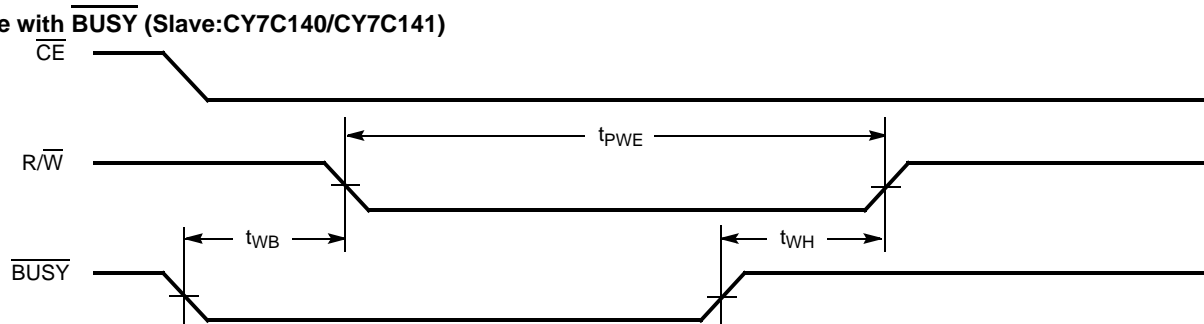
Figure 11. Busy Timing Diagram No. 2 (Address Arbitration)



Switching Waveforms (continued)

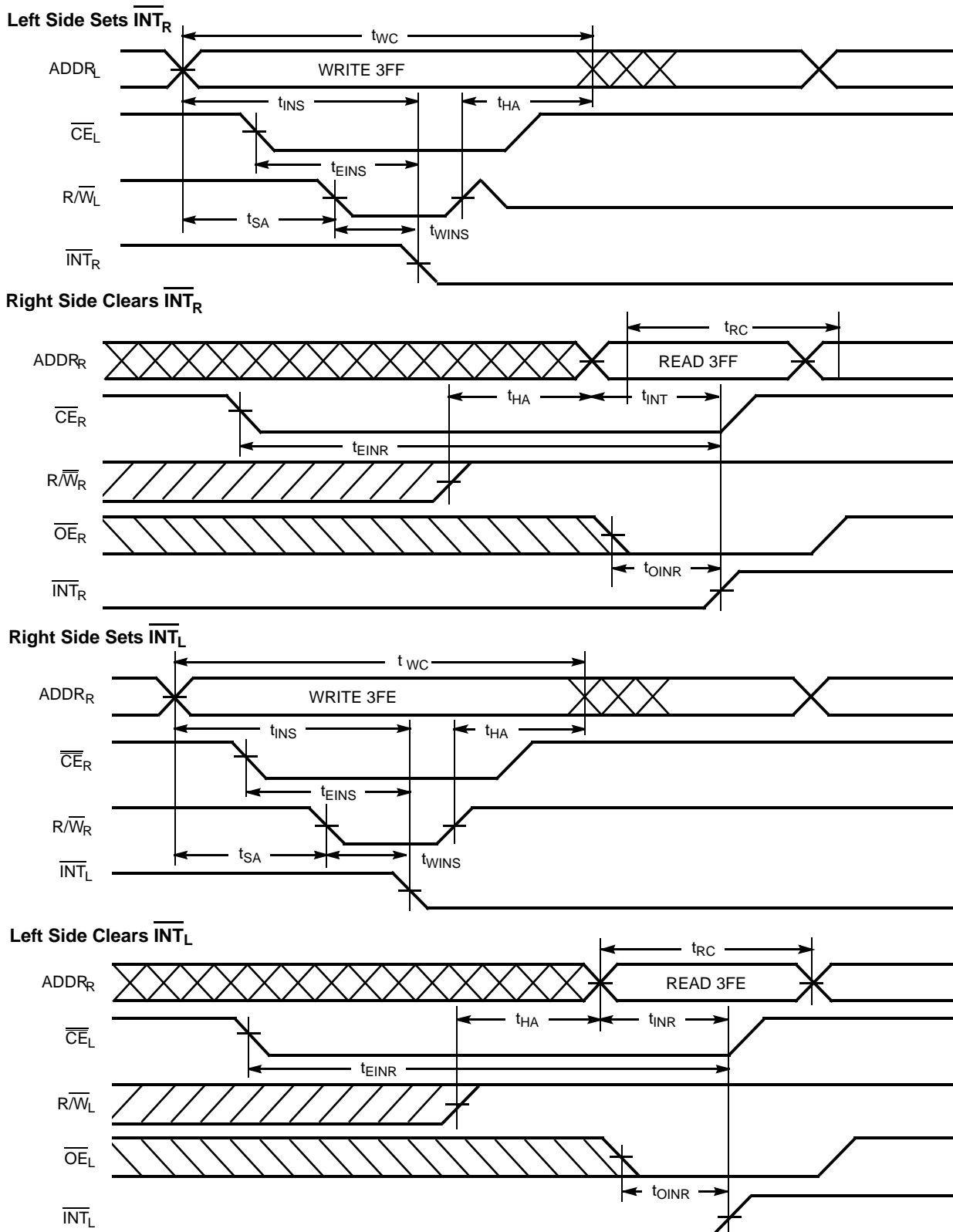
Figure 12. Busy Timing Diagram No. 3

Write with  $\overline{\text{BUSY}}$  (Slave:CY7C140/CY7C141)

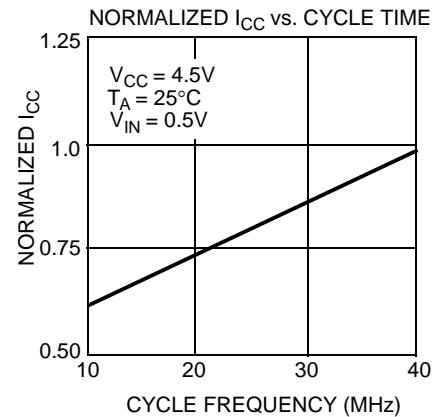
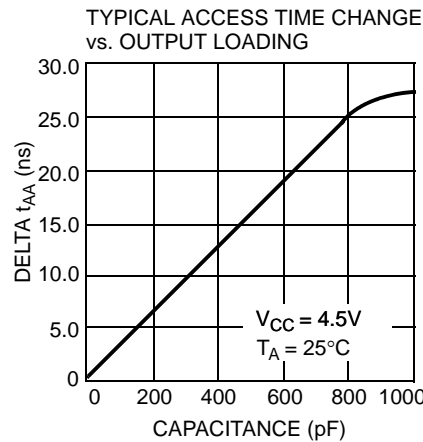
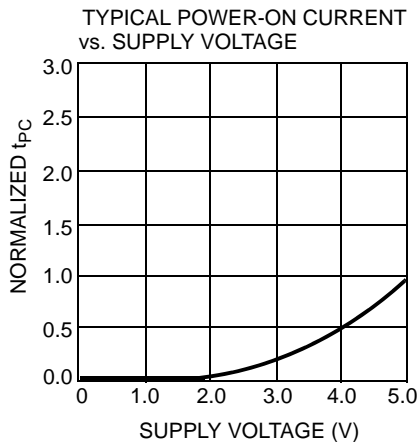
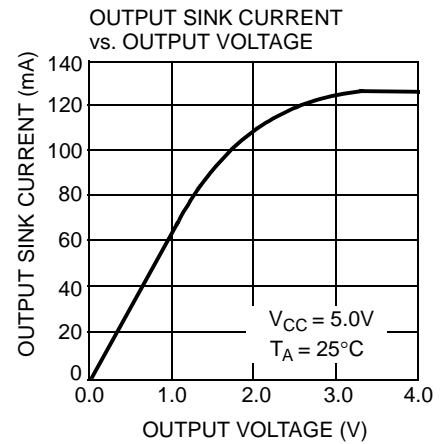
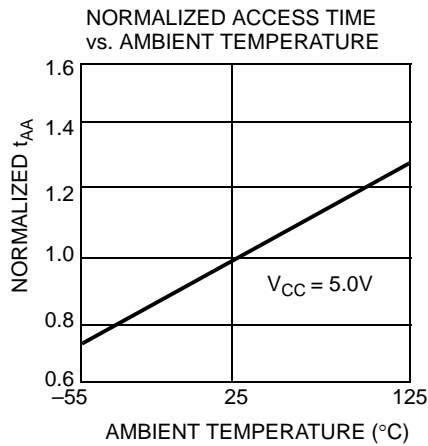
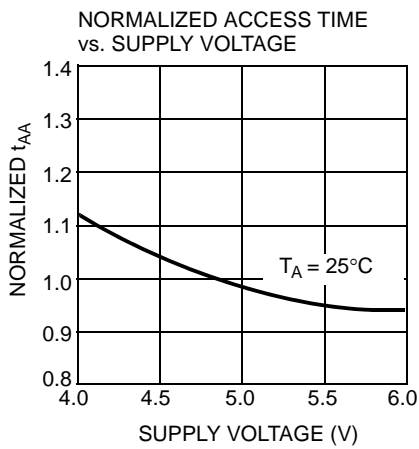
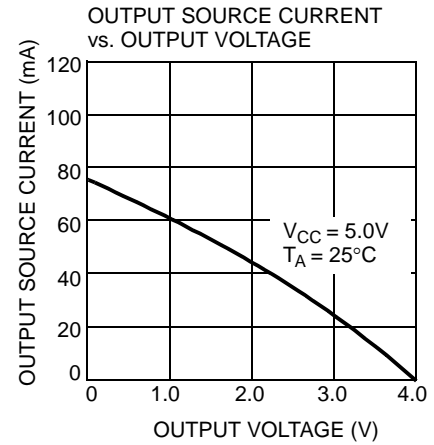
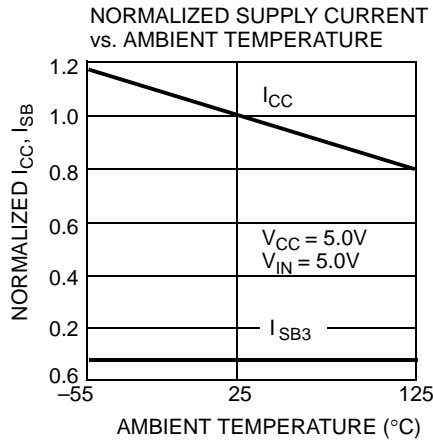
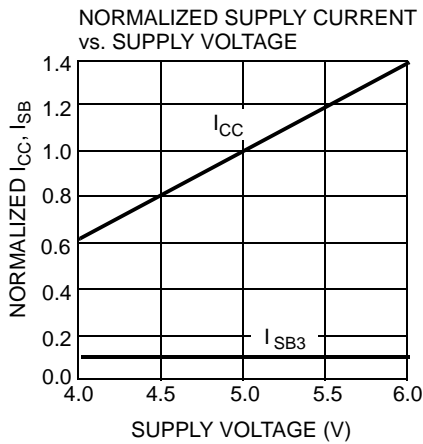


Switching Waveforms (continued)

Figure 13. Interrupt Timing Diagrams



**Typical DC and AC Characteristics**



## Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C130-30PC	P25	48-Pin (600 Mil) Molded DIP	Commercial
	CY7C130A-30PI	P25	48-Pin Pb-Free (600 Mil) Molded DIP	Industrial
35	CY7C130-35PC	P25	48-Pin (600 Mil) Molded DIP	Commercial
	CY7C130-35PI	P25	48-Pin (600 Mil) Molded DIP	Industrial
45	CY7C130-45PC	P25	48-Pin (600 Mil) Molded DIP	Commercial
	CY7C130-45PI	P25	48-Pin (600 Mil) Molded DIP	Industrial
55	CY7C130-55PC	P25	48-Pin (600 Mil) Molded DIP	Commercial
	CY7C130-55PI	P25	48-Pin (600 Mil) Molded DIP	Industrial
15	CY7C131-15JC	J69	52-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C131-15JXC	J69	52-Pin Pb-Free Plastic Leaded Chip Carrier	
	CY7C131-15NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-15JI	J69	52-Pin Plastic Leaded Chip Carrier	Industrial
	CY7C131A-15JXI	J69	52-Pin Pb-Free Plastic Leaded Chip Carrier	
	CY7C131-15NXI	N52	52-Pin Pb-Free Plastic Quad Flatpack	
25	CY7C131-25JC	J69	52-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C131-25JXC	J69	52-Pin Pb-Free Plastic Leaded Chip Carrier	
	CY7C131-25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-25NXC	N52	52-Pin Pb-Free Plastic Quad Flatpack	Industrial
	CY7C131-25JI	J69	52-Pin Plastic Leaded Chip Carrier	
	CY7C131-25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C131-30JC	J69	52-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C131-30NC	N52	52-Pin Plastic Quad Flatpack	Industrial
	CY7C131-30JI	J69	52-Pin Plastic Leaded Chip Carrier	
35	CY7C131-35JC	J69	52-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C131-35NC	N52	52-Pin Plastic Quad Flatpack	Industrial
	CY7C131-35JI	J69	52-Pin Plastic Leaded Chip Carrier	
	CY7C131-35NI	N52	52-Pin Plastic Quad Flatpack	
45	CY7C131-45JC	J69	52-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C131-45NC	N52	52-Pin Plastic Quad Flatpack	Industrial
	CY7C131-45JI	J69	52-Pin Plastic Leaded Chip Carrier	
	CY7C131-45NI	N52	52-Pin Plastic Quad Flatpack	
55	CY7C131-55JC	J69	52-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C131-55JXC	J69	52-Pin Pb-Free Plastic Leaded Chip Carrier	
	CY7C131-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-55NXC	N52	52-Pin Pb-Free Plastic Quad Flatpack	
	CY7C131-55JI	J69	52-Pin Plastic Leaded Chip Carrier	Industrial
	CY7C131-55JXI	J69	52-Pin Pb-Free Plastic Leaded Chip Carrier	
	CY7C131-55NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-55NXI	N52	52-Pin Pb-Free Plastic Quad Flatpack	
30	CY7C140-30PC	P25	48-Pin (600 Mil) Molded DIP	Commercial
	CY7C140-30PI	P25	48-Pin (600 Mil) Molded DIP	Industrial

**Ordering Information** (continued)

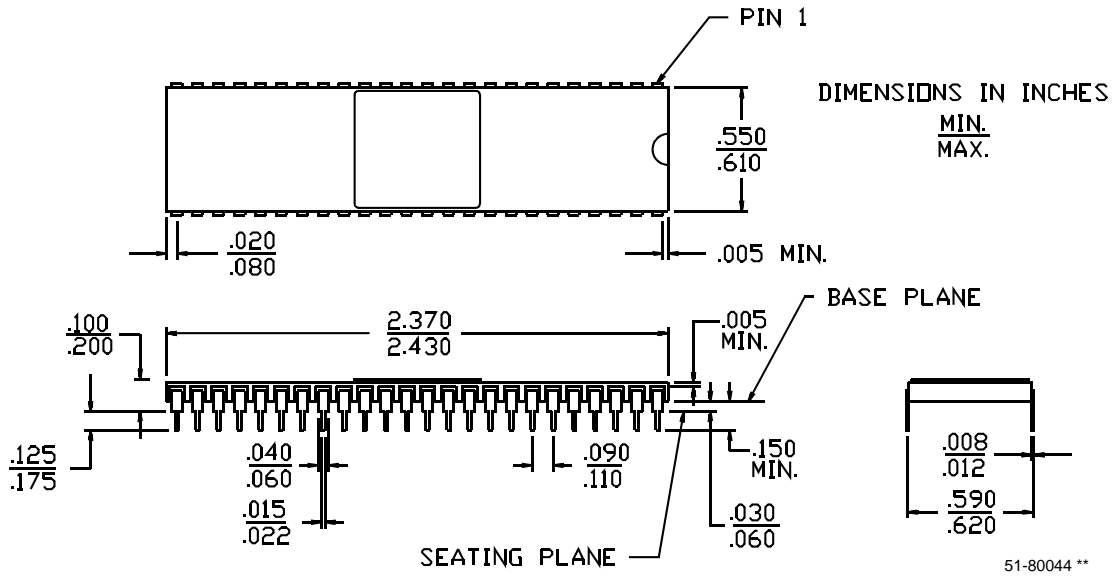
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
35	CY7C140-35PC	P25	48-Pin (600 Mil) Molded DIP	Commercial
	CY7C140-35PI	P25	48-Pin (600 Mil) Molded DIP	Industrial
45	CY7C140-45PC	P25	48-Pin (600 Mil) Molded DIP	Commercial
	CY7C140-45PI	P25	48-Pin (600 Mil) Molded DIP	Industrial
55	CY7C140-55PC	P25	48-Pin (600 Mil) Molded DIP	Commercial
	CY7C140-55PI	P25	48-Pin (600 Mil) Molded DIP	Industrial
15	CY7C141-15JC	J69	52-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C141-15NC	N52	52-Pin Plastic Quad Flatpack	
25	CY7C141-25JC	J69	52-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C141-25JXC	J69	52-Pin Pb-Free Plastic Leaded Chip Carrier	
	CY7C141-25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-25JI	J69	52-Pin Plastic Leaded Chip Carrier	Industrial
	CY7C141-25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C141-30JC	J69	52-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C141-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-30JI	J69	52-Pin Plastic Leaded Chip Carrier	Industrial
35	CY7C141-35JC	J69	52-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C141-35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-35JI	J69	52-Pin Plastic Leaded Chip Carrier	Industrial
	CY7C141-35NI	N52	52-Pin Plastic Quad Flatpack	
45	CY7C141-45JC	J69	52-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C141-45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-45JI	J69	52-Pin Plastic Leaded Chip Carrier	Industrial
	CY7C141-45NI	N52	52-Pin Plastic Quad Flatpack	
55	CY7C141-55JC	J69	52-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C141-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-55JI	J69	52-Pin Plastic Leaded Chip Carrier	Industrial
	CY7C141-55NI	N52	52-Pin Plastic Quad Flatpack	



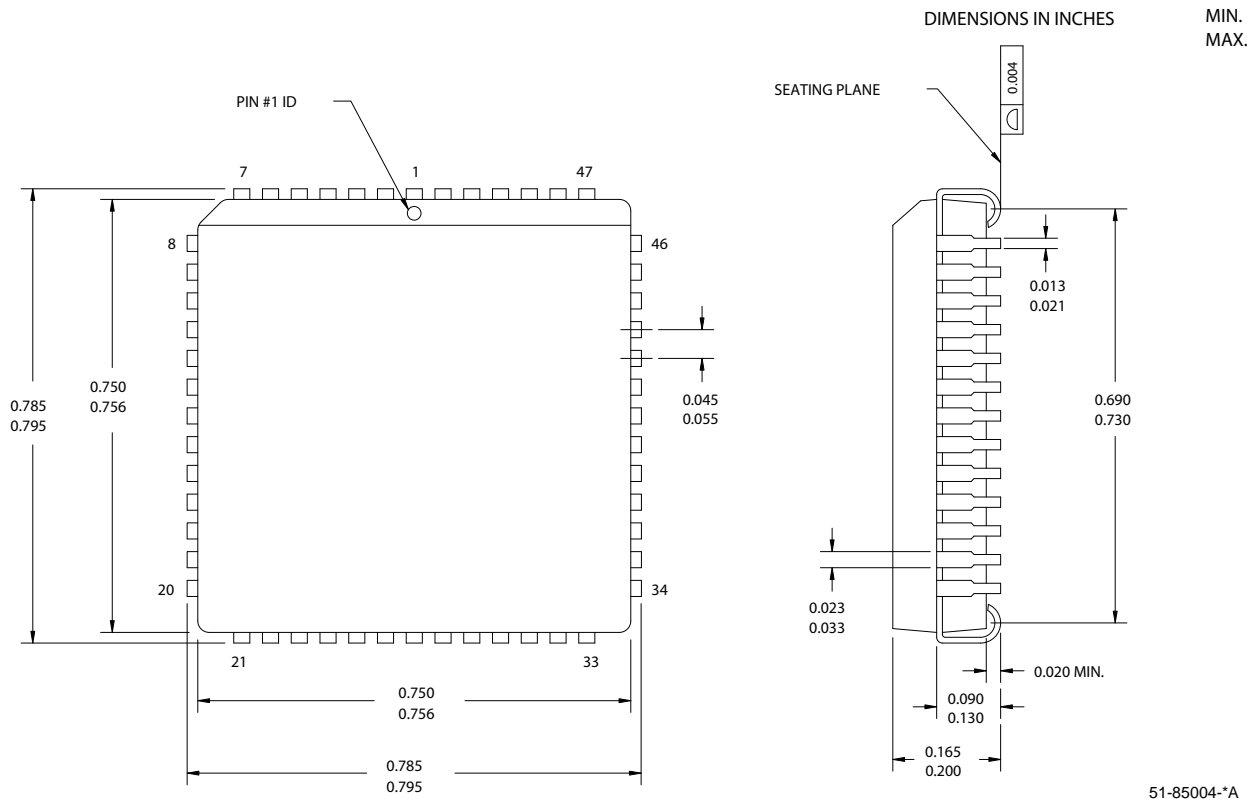
**Package Diagrams**

**Figure 14. 48-Pin (600 Mil) Sidebrazed DIP D26**

MIL-STD-1835 D-14 Config. C

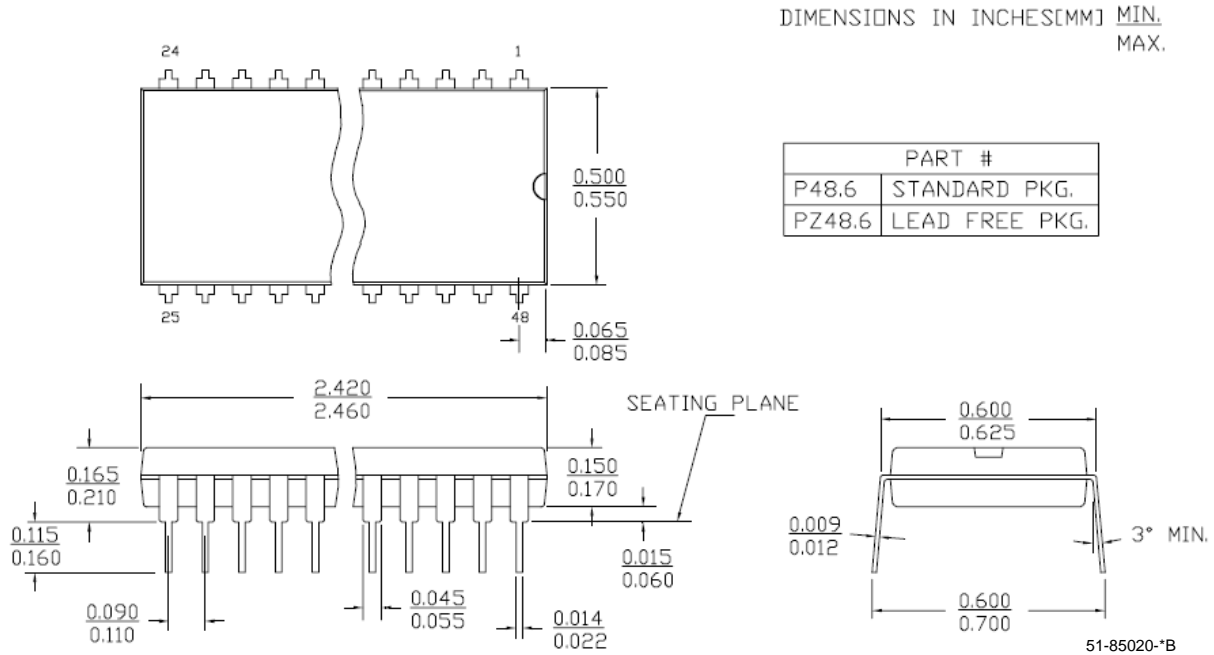


**Figure 15. 52-Pin Pb-Free Plastic Leaded Chip Carrier J69**

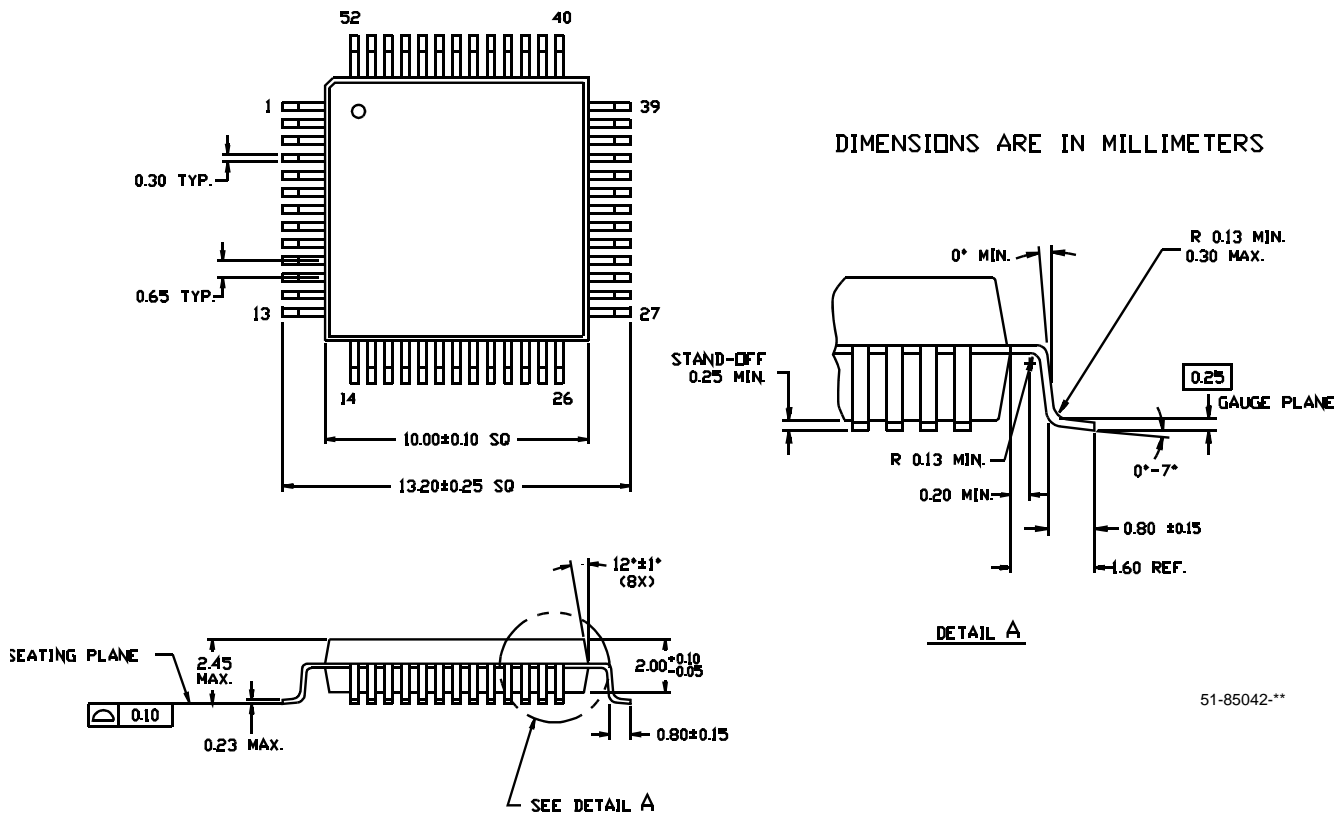


**Package Diagrams** (continued)

**Figure 16. 48-Pin (600 Mil) Molded DIP P25**



**Figure 17. 52-Pin Pb-Free Plastic Quad Flatpack N52**



## Document History Page

Document Title: CY7C130/CY7C130A/CY7C131/CY7C131A/CY7C140/CY7C141 1K x 8 Dual-Port Static RAM				
Document Number: 38-06002				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	110169	SZV	09/29/01	Change from Spec number: 38-00027 to 38-06002
*A	122255	RBI	12/26/02	Power up requirements added to Maximum Ratings Information
*B	236751	YDT	See ECN	Removed cross information from features section
*C	325936	RUY	See ECN	Added pin definitions table, 52-pin PQFP package diagram and Pb-free information
*D	393153	YIM	See ECN	Added CY7C131-15JI to ordering information Added Pb-Free parts to ordering information: CY7C131-15JXI
*E	2623540	VKN/PYRS	12/17/08	Added CY7C130A and CY7C131A parts Removed military information Updated ordering information table

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