NCV4263-2C

LDO Regulator - Enable, Reset, Watchdog

200 mA

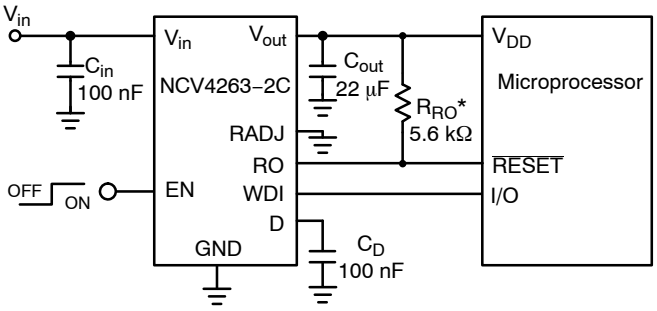
The NCV4263−2C is a 200 mA LDO regulator with integrated reset watchdog functions dedicated for microprocessor applications. Its robustness allows NCV4263−2C to be used in severe automotive environments. The Enable function can be used for decrease of quiescent current down to max 10 μA. The NCV4263−2C contains protection functions as current limit, thermal shutdown and reverse output current protection. The regulator provides also Watchdog, Reset function with adjustable Threshold and adjustable Power−on Reset Delay Time.

Features

- Output Voltage Option: 5 V
- Output Voltage Accuracy: ±2%
- Output Current up to 200 mA
- Very Low Dropout Voltage
- Enable Function (10 μA Max Quiescent Current when Disabled)
- Microprocessor Compatible Control Functions:
  - Reset with Adjustable Threshold and Adjustable Power−on Delay
  - Watchdog Function
- Wide Input Voltage Operation Range: up to 40 V
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
  - Reverse Output Current
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications

- Body Control Module
- Instruments and Clusters
- Occupant Protection and Comfort
- Powertrain



*−optional if Reset function is needed

Figure 1. Application Schematic

ON Semiconductor®

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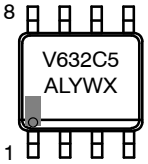
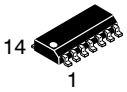
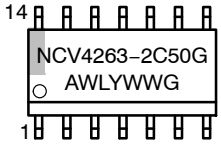
MARKING DIAGRAMS

SOIC−8 EP
PD SUFFIX
CASE 751AC





SOIC−14
D SUFFIX
CASE 751A



A	= Assembly Location
L, WL	= Wafer Lot
Y	= Year
W, WW	= Work Week
G	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

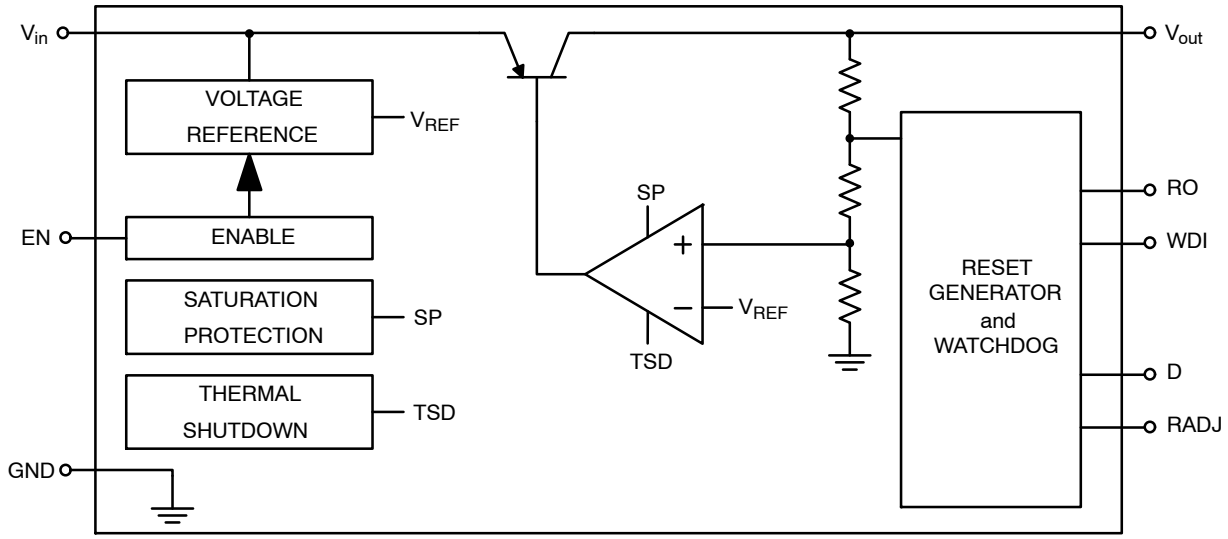


Figure 2. Simplified Block Diagram

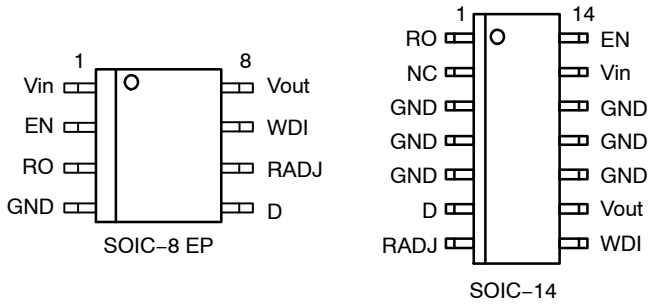


Figure 3. Pin Connections
(Top View)

PIN FUNCTION DESCRIPTION

Pin No. SO−8 EP	Pin No. SO−14	Pin Name	Description
1	13	V_{in}	Positive Power Supply. Connect ceramic capacitor to ground.
2	14	EN	Enable Input. Low level disables the chip. Connect to V_{in} if this function is not needed.
3	1	RO	Reset Output; Open Collector connected to the V_{out} via an internal 30 kΩ pull−up resistor; leave open if the function is not needed
4	3, 4, 5, 10, 11, 12	GND	Power Supply Ground. Connect pins to heat sink area with GND potential.
5	6	D	DelayTiming. Connect to GND via ceramic capacitor for adjusting reset delay timing and watchdog trigger time or leave open if this function is not needed.
6	7	RADJ	Reset Adjust Threshold. Connect to GND (V_{RT} = 93% of V_{out}) or to output voltage divider to adjust the reset threshold.
7	8	WDI	Watchdog Input. Rising edge triggered Input for watchdog pulses. Connect to GND if this function is not needed.
8	9	V_{out}	Regulated Output Voltage. Connect a $C_{out} \geq 22$ μF capacitor to ground.
EPAD	−	Exposed Pad	Connect to ground potential or leave unconnected.
−	2	NC	Not connected. No internally bonded.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 1)	V_{in}	−42	45	V
Enable Input	V_{EN}	−42	45	V
Output Voltage	V_{out}	−1	7	V
Reset Output Voltage	V_{RO}	−0.3	7	V
Watchdog Input Voltage	V_{WDI}	−0.3	7	V
Reset Adjust Threshold	V_{RADJ}	−0.3	7	V
Delay Timing Output Voltage	V_D	−0.3	7	V
Maximum Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

ESD CAPABILITY (Note 2)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−	2	kV
ESD Capability, Charged Device Model	ESD_{CDM}	−	1	kV

2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101)

LEAD SOLDERING TEMPERATURE AND MSL (Note 3)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level SOIC−14 SOIC−8 EP	MSL		1 2	−
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions	T_{SLD}	−	265 peak	°C

3. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC−8 Exposed Pad (Note 4) Thermal Resistance, Junction−to−Air (Note 5) Thermal Reference, Junction−to−Pad (Note 5)	 $R_{\theta JA}$ $\Psi_{\psi JPad}$	 65.1 8.7	°C/W
Thermal Characteristics, SOIC−14 (Note 4) Thermal Resistance, Junction−to−Air (Note 5) Thermal Reference, Junction−to−Pin4 (Note 5)	 $R_{\theta JA}$ $\Psi_{\psi JP4}$	 94.8 18.3	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 6)

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{in}	5.5	40	V
Junction Temperature	T_J	−40	150	°C

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, V_{EN} = 5 V, C_{in} = 100 nF, C_{out} = 22 μF, ESR = 1.5 Ω, WDI = 5 V pulses, f_{WDI} = 1 kHz. Min and Max values are valid for temperature range $-40°C \le T_J \le 150°C$ unless otherwise noted and are guaranteed by test design or statistical correlation. Typical values are referenced to T_J = 25°C. (Notes 7 and 8)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Voltage Accuracy	V_{in} = 6 V to 40 V, I_{out} = 5 to 150 mA	V_{out}	4.90	5.0	5.10	V
Line Regulation	I_{out} = 150 mA, V_{in} = 6 V to 28 V	Reg_{line}	−25	3	25	mV
Load Regulation	I_{out} = 5 mA to 150 mA	Reg_{load}	−25	−	25	mV
Dropout Voltage (Note 9)	I_{out} = 150 mA	V_{DO}	−	300	500	mV
DISABLE AND QUIESCENT CURRENTS						
Disable Current	V_{EN} = 0 V,T_J < 125°C	I_{DIS}	−	0.066	10	μA
Quiescent Current, $I_q = I_{in} - I_{out}$	I_{out} = 0 mA I_{out} = 150 mA I_{out} = 150 mA, V_{in} = 4.5 V	I_q	 − − −	 0.275 3 11.3	 1.3 18 23	mA
CURRENT LIMIT PROTECTION						
Current Limit	V_{out} = 0.96 x V_{out_nom}	I_{LIM}	200	418	500	mA
PSRR						
Power Supply Ripple Rejection (Note 10)	f = 100 Hz, 0.5 V_{p-p}	PSRR	−	80	−	dB
ENABLE						
Enable Input Threshold Voltage Logic High Logic Low	 $V_{out} \ge$ 0.9 x V_{out_nom} $V_{out} \le$ 0.1 V	$V_{th(EN)}$	 − 0.8	 2.0 1.74	 3.5 −	V
Enable Input Current	V_{EN} = 5 V	I_{EN}	5	10	25	μA
WATCHDOG INPUT						
Watchdog Input Low Time	C_D = 100 nF, $V_{out} > V_{RT}$, no WDI signal	t_{WL}	1	2	3.5	ms
Watchdog Trigger Time	C_D = 100 nF, $V_{out} > V_{RT}$, no WDI signal	t_{WTT}	16	20.8	27	ms
DELAY TIMING						
Charge Current	V_D = 1 V, no WDI signal	I_{D_charge}	40	66.8	95	μA
Discharge Current	V_D = 1 V, no WDI signal	I_{D_disch}	4.40	6.54	9.40	μA
Saturation Voltage	$V_{out} < V_{RT}$, no WDI signal	V_{D_sat}	−	6	100	mV
Switching Threshold Upper Lower		 $V_{thH(D)}$ $V_{thL(D)}$	 1.45 0.2	 1.70 0.34	 2.05 0.55	V
RESET OUTPUT						
Output Voltage Reset Threshold (Note 11)	V_{out} decreasing, V_{RADJ} = 0 V	V_{RT}	90	93	96	% V_{out}
Reset Adjust Threshold	(70% of V_{out_nom}) $\le V_{out} < (V_{RT})$	$V_{th(RADJ)}$	1.26	1.36	1.44	V
Reset Adjustment Range (Note 12)		V_{RT_range}	70	−	93	% V_{out}
Reset Output Low Voltage	I_{RO} = 1 mA	V_{ROL}	−	0.01	0.4	V
Reset Delay Time	C_D = 100 nF	t_{RD}	1.3	2.6	4.1	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
8. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
9. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.5 V.
10. Values based on design and/or characterization.
11. See APPLICATION INFORMATION section for Reset Threshold Adjustment
12. V_{RT_range} limits are guaranteed by V_{RT} and $V_{th(RADJ)}$ parameters.

ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, V_{EN} = 5 V, C_{in} = 100 nF, C_{out} = 22 μF, ESR = 1.5 Ω, WDI = 5 V pulses, f_{WDI} = 1 kHz. Min and Max values are valid for temperature range $-40°C \le T_J \le 150°C$ unless otherwise noted and are guaranteed by test design or statistical correlation. Typical values are referenced to T_J = 25°C. (Notes 7 and 8)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
RESET OUTPUT						
Reset Reaction Time	C_D = 100 nF	t_{RR}	0.5	1.2	4	μs
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 10)	I_{out} = 1 mA	T_{SD}	150	177	195	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
8. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
9. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.5 V.
10. Values based on design and/or characterization.
11. See APPLICATION INFORMATION section for Reset Threshold Adjustment
12. V_{RT_range} limits are guaranteed by V_{RT} and $V_{th(RADJ)}$ parameters.

TYPICAL CHARACTERISTICS

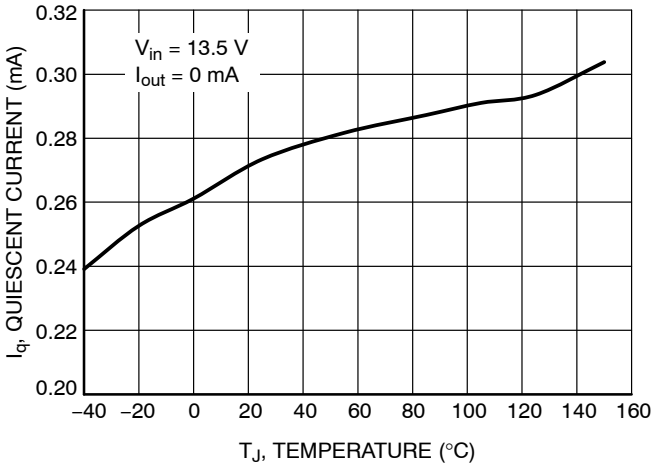


Figure 4. Quiescent Current vs. Temperature

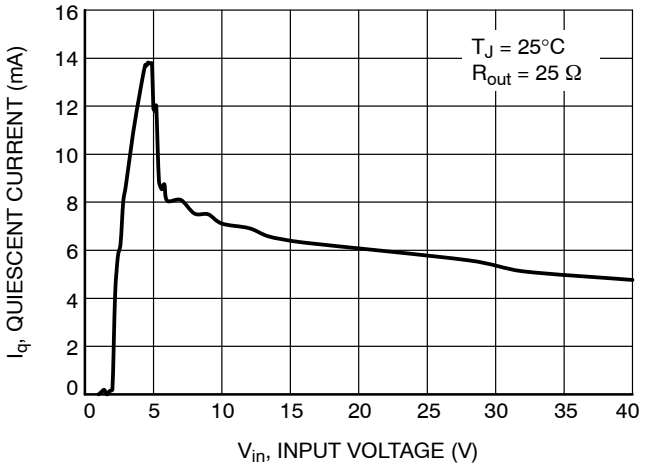


Figure 5. Quiescent Current vs. Input Voltage

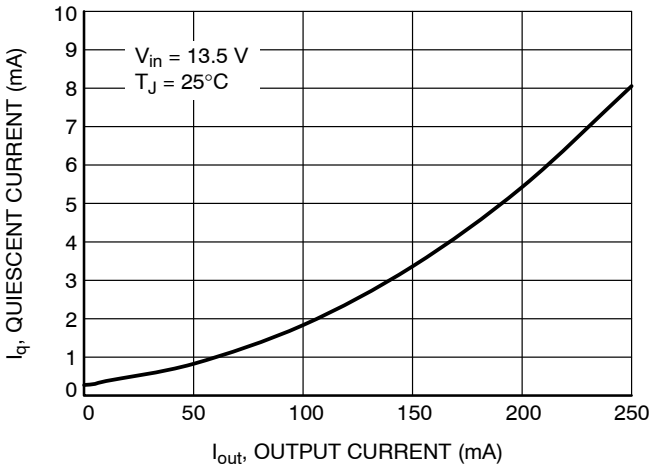


Figure 6. Quiescent Current vs. Output Current

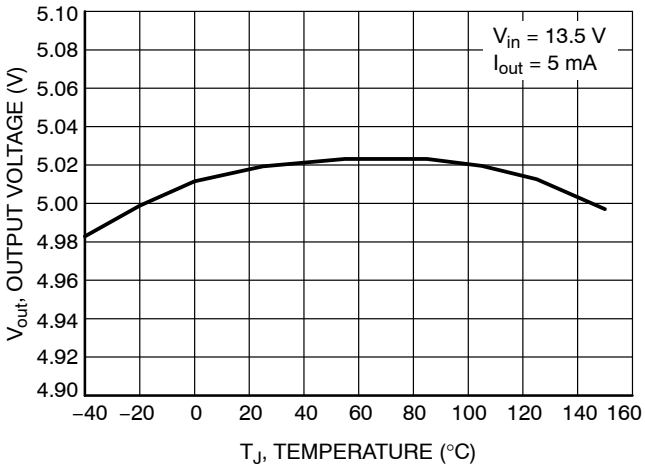


Figure 7. Output Voltage Accuracy

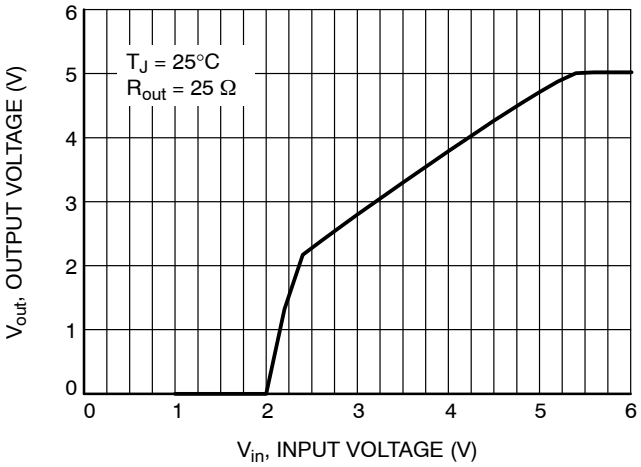


Figure 8. Output Voltage vs. Input Voltage

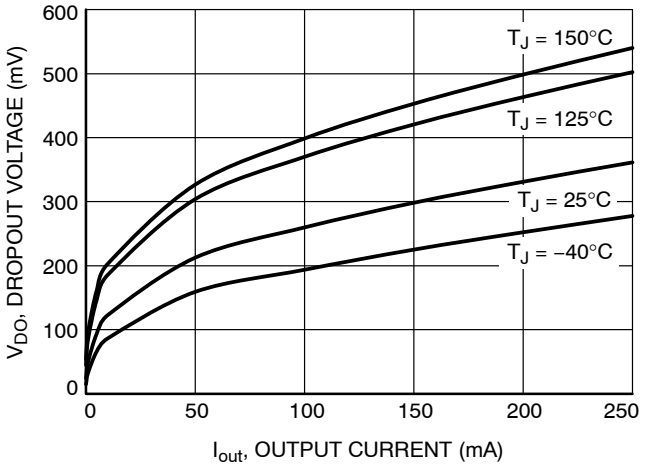


Figure 9. Dropout Voltage vs. Output Current

TYPICAL CHARACTERISTICS

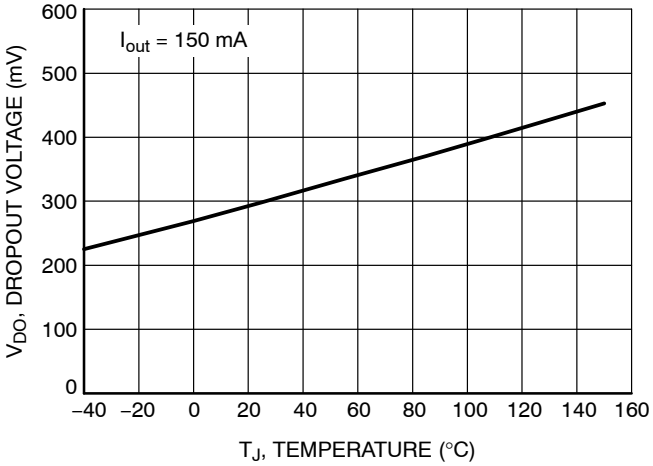


Figure 10. Dropout Voltage vs. Temperature

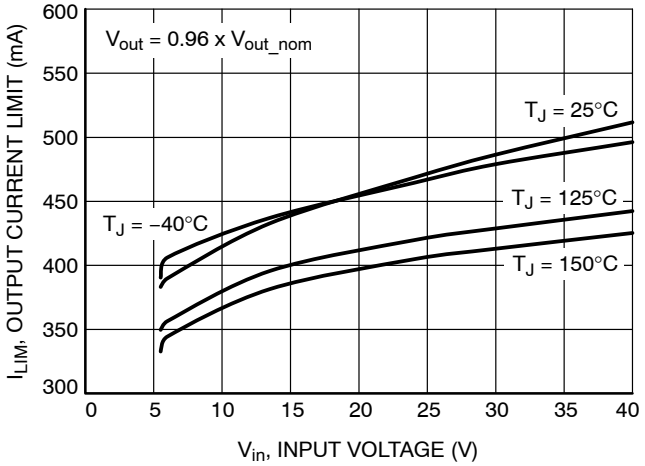


Figure 11. Output Current Limit vs. Input Voltage

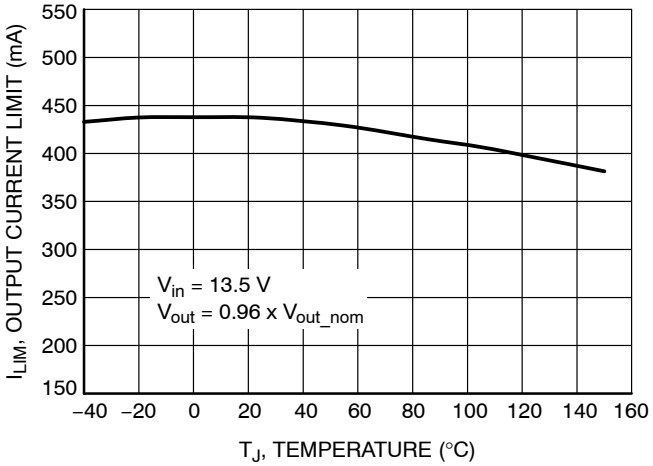


Figure 12. Output Current Limit vs. Temperature

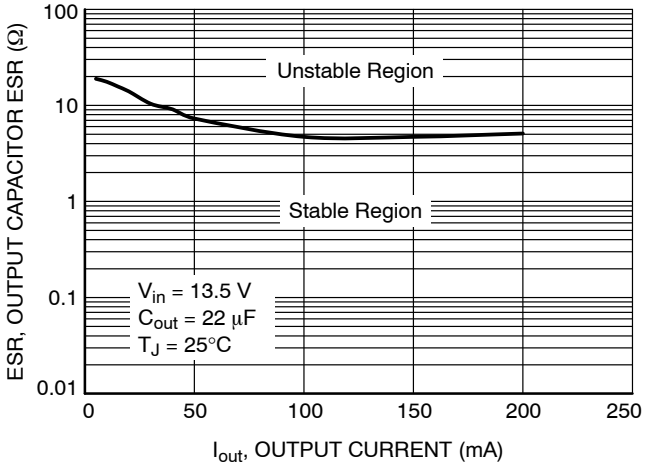


Figure 13. Output Capacitor ESR Stability Region vs. Output Current

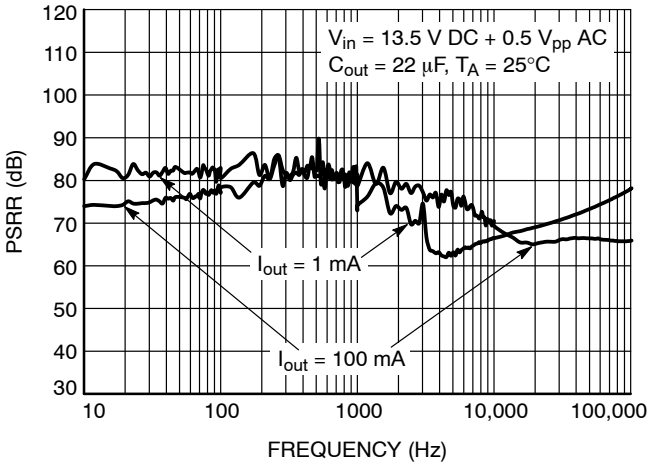


Figure 14. PSRR vs. Frequency

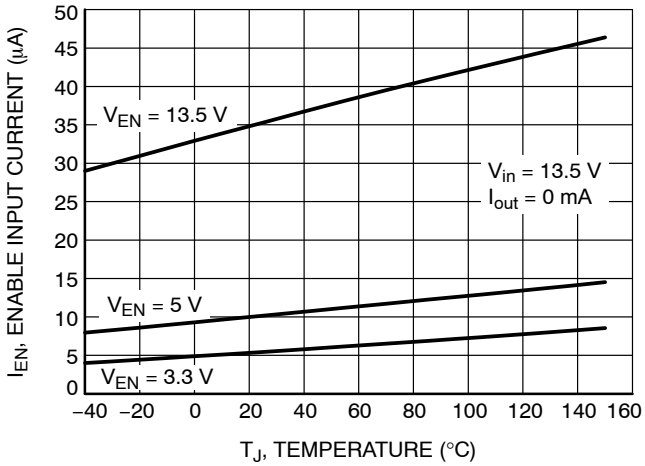


Figure 15. Enable Input Current vs. Temperature

TYPICAL CHARACTERISTICS

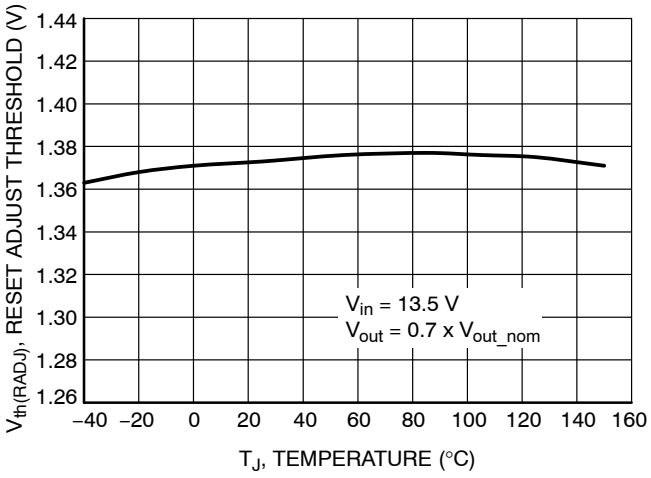


Figure 16. Reset Adjust Threshold vs. Temperature

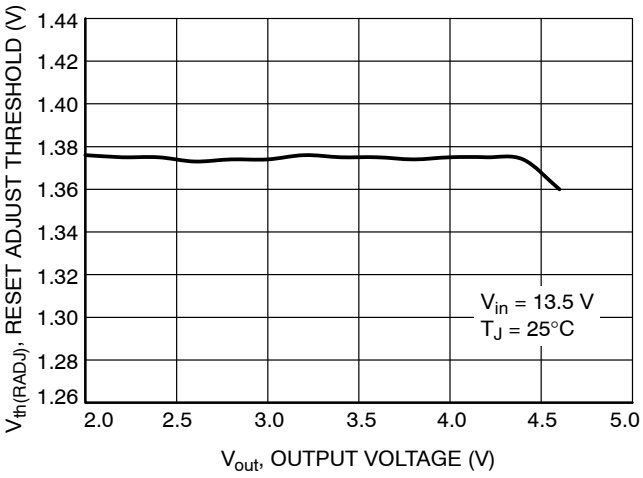


Figure 17. Reset Adjust Threshold vs. Output Voltage

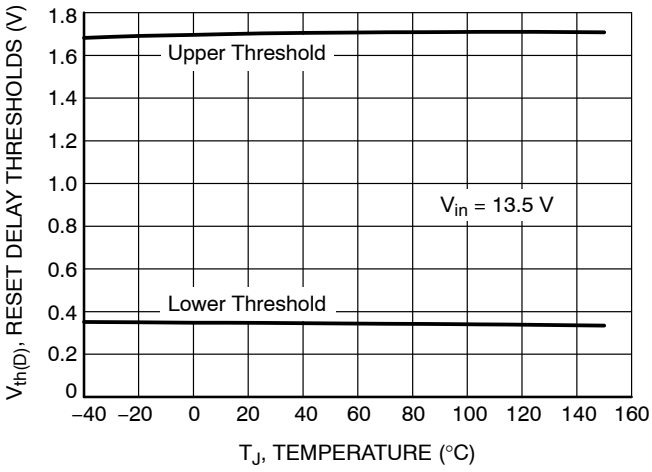


Figure 18. Delay Timing Switching Thresholds vs. Temperature

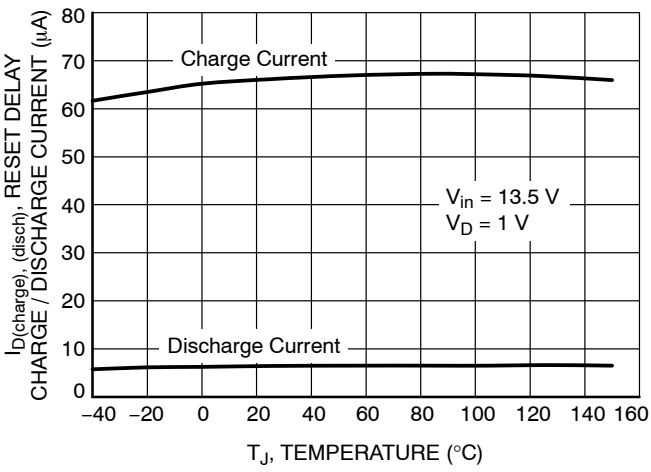


Figure 19. Reset Delay Charge / Discharge Current vs. Temperature

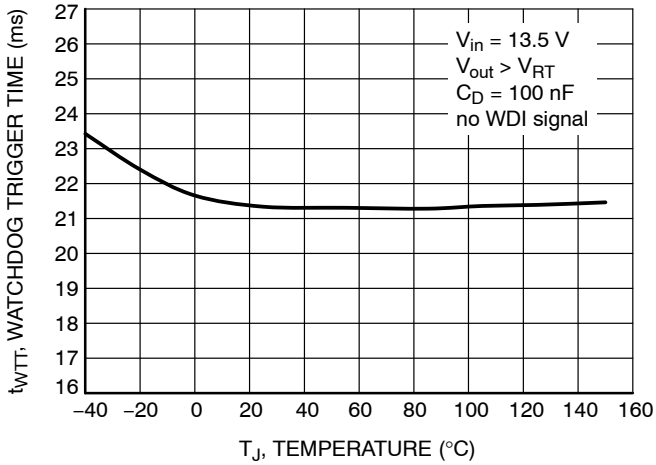


Figure 20. Watchdog Trigger Time vs. Temperature

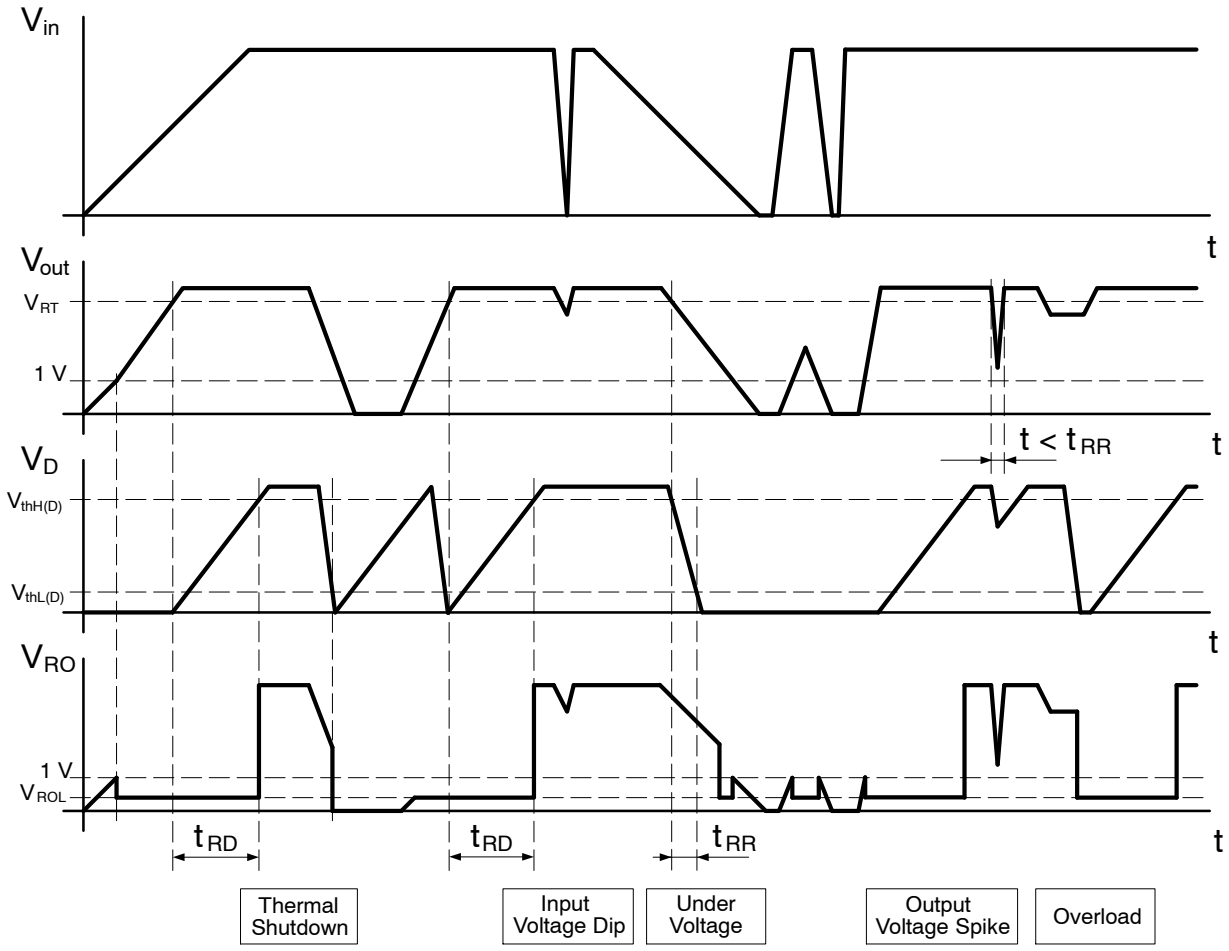


Figure 21. Reset Operation Timing Diagram

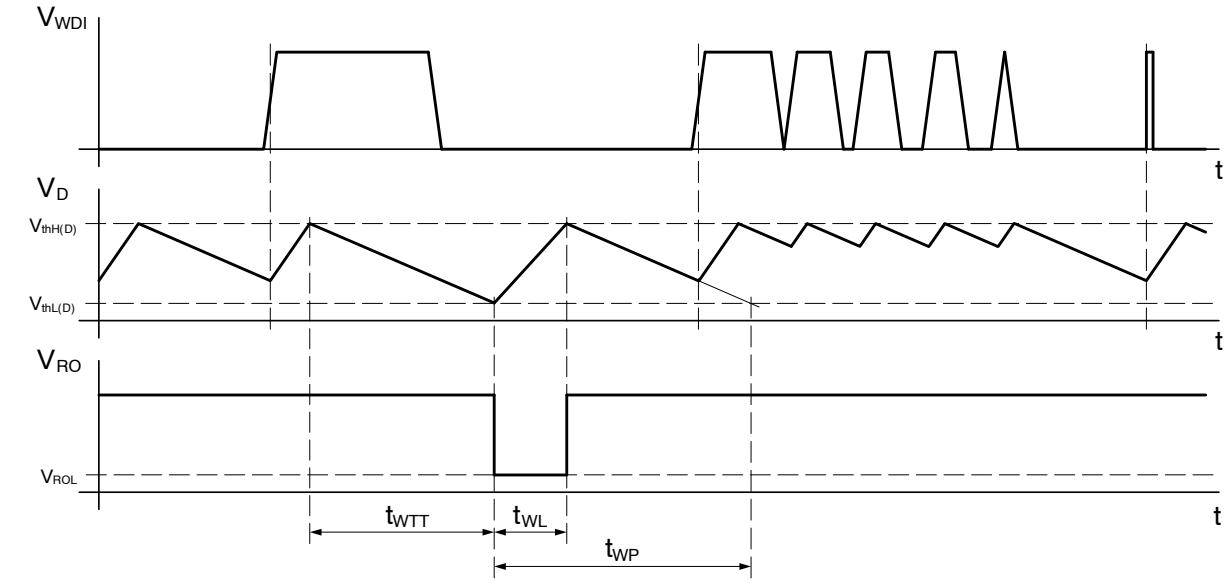


Figure 22. Watchdog Operation Timing Diagram

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output Voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent and Disable Currents

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current. If Enable pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current (I_{DIS}).

Current Limit and Short Circuit Current Limit

Current Limit is value of output current by which output voltage drops below 96% of its nominal value. It means that the device is capable to supply minimum 200 mA without sending Reset signal to microprocessor.

Short Circuit Current Limit is output current value measured with output of the regulator shorted to ground.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low−load and high−load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 177°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

The NCV4263−2C regulator is self−protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figures 4 to 22.

Input Decoupling (C_{in})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV4263−2C package. Higher capacitance and lower ESR will improve the overall line and load transient response. If extremely fast input voltage transients are expected then appropriate input filter is recommended to use in order to decrease rising and/or falling edges below 50 V/μs for proper operation. The filter can be composed of several capacitors in parallel.

Output Decoupling (C_{out})

The NCV4263−2C is a stable component and requires a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR versus Output Current is shown in Figure 13. The minimum output decoupling value is 22 μF and can be augmented to fulfill stringent load transient requirements. Larger values improve noise rejection and load transient response.

Enable Operation

The Enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet.

Delay Timing

The Delay Timing pin is current source. Current from Delay Timing pin charges connected capacitor. The value of this capacitor determines the Reset Delay Time by Equation 1 and Watchdog Trigger Time by Equation 4.

$$C_D = \left(\frac{t_{RD\_des}}{t_{RD}}\right) \times 100\ nF \qquad \text{(eq. 1)}$$

where:

C_D is capacitance of Delay capacitor
t_{RD_des} is desired Reset Delay Time
t_{RD} is Reset Delay Time specified in datasheet

Reset Operation

A reset signal is provided on the Reset Output pin to provide feedback to the microprocessor of an out of regulation condition. The timing diagram of reset function is shown in Figure 21. This is in the form of a logic signal on Reset Output. Output voltage conditions below the Reset Threshold causes Reset Output to go low. The Reset Output integrity is maintained down to V_{out} = 1.0 V. The Reset Output circuitry is open collector output with internal 30 kΩ pull−up resistor. Leave open this output if the Reset function is not needed else an external pull−up resistor (5.6 kΩ) connect to the output (V_{out}).

Reset Threshold is default set to 93% of nominal Output Voltage (V_{RADJ} = 0 V). Reset Threshold can be varied in range of Output Voltage 70% ≤ V_{out} < V_{RT} by external resistor output voltage divider, see schematic on Figure 23 and specification of Reset Output.

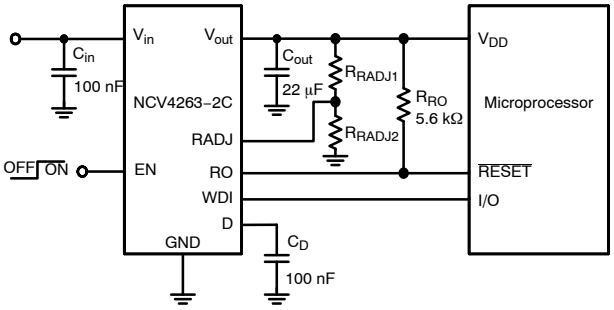


Figure 23. Application Schematic with Adjustable Reset Threshold

Desired Reset Threshold is given by Equation 2.

$$V_{RT\_des} = \left(\frac{R_{RADJ1} + R_{RADJ2}}{R_{RADJ2}}\right) \times V_{th(RADJ)} \qquad \text{(eq. 2)}$$

where:

V_{RT_des} is desired Reset Threshold
R_{RADJ1}, R_{RADJ2} are resistance of resistor divider
$V_{th(RADJ)}$ is Reset Adjust Threshold specified in datasheet

Use $R_{RADJ2} \leq 50$ kΩ to avoid significant Reset Threshold error due to RADJ bias current.

Watchdog Operation

Watchdog Input monitors a signal from microprocessor. This input is positive edge sensitive. The timing diagram of watchdog function is shown in Figure 22. When watchdog signal is not received during Watchdog Trigger Time, Reset Output goes low for a Watchdog Input Low Time and is periodically generated with period given by Equation 3. Capacitance of Delay capacitor for setting the desired Watchdog Trigger Time is given by Equation 4.

$$t_{WP} = t_{WL} + t_{WTT} \qquad \text{(eq. 3)}$$

$$C_D = \left(\frac{t_{WTT\_des}}{t_{WTT}}\right) \times 100\ nF \qquad \text{(eq. 4)}$$

where:

C_D is capacitance of Delay capacitor
t_{WTT_des} is desired Watchdog Trigger Time
t_{WTT} is Watchdog Trigger Time specified in datasheet
t_{WL} is Watchdog Input Low Time
t_{WP} is Watchdog Input Period

Thermal Considerations

As power in the NCV4263−2C increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent

upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV4263−2C has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV4263−2C can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 5)}$$

Since T_J is not recommended to exceed 150°C, then the NCV4263−2C soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 1.3 W in SOIC−14 package and 1.9 W in SOIC−8 EP package, when the ambient temperature (T_A) is 25°C. See Figures 24 and 25 for $R_{\theta JA}$ versus PCB area. The power dissipated by the NCV4263−2C can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_q @ I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \quad \text{(eq. 6)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \quad \text{(eq. 7)}$$

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV4263−2C and make traces as short as possible.

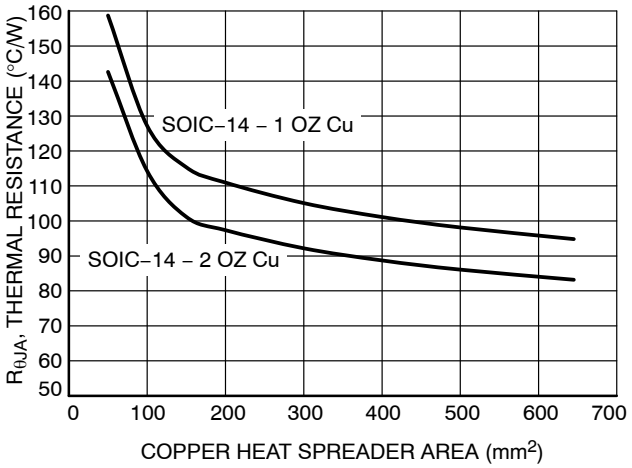


Figure 24. Thermal Resistance vs. PCB Copper Area for SOIC−14

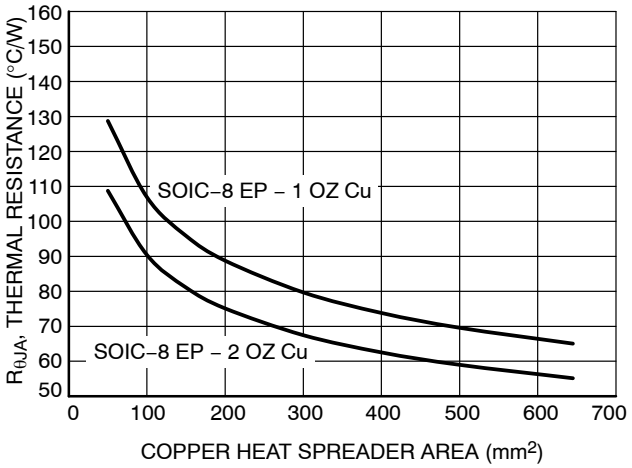


Figure 25. Thermal Resistance vs. PCB Copper Area for SOIC−8 EP

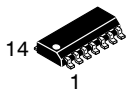
ORDERING INFORMATION

Device	Output Voltage	Marking	Package	Shipping†
NCV4263−2CD250R2G	5.0 V	NCV4263−2C50G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
NCV4263−2CPD50R2G	5.0 V	V632C5	SOIC−8 EP (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

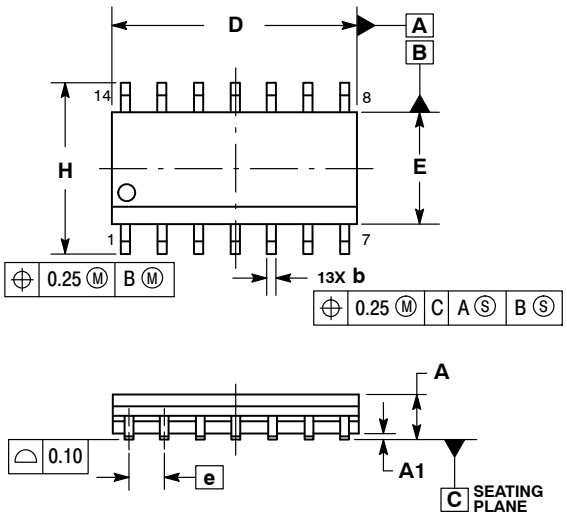
ON Semiconductor®

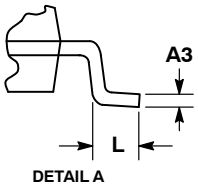


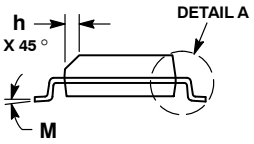
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



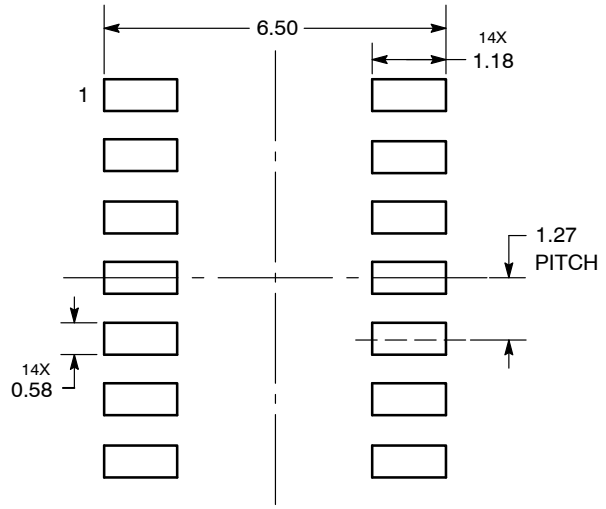




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

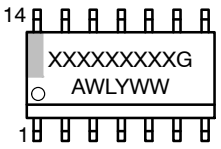
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

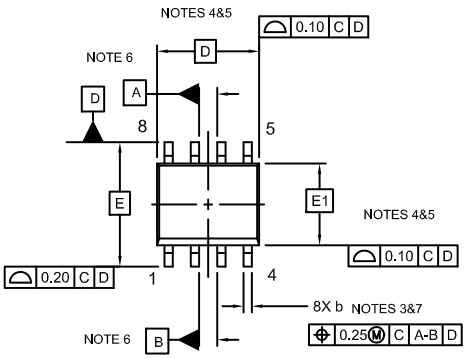
SCALE 1:1

SOIC−8 EP
CASE 751AC
ISSUE D

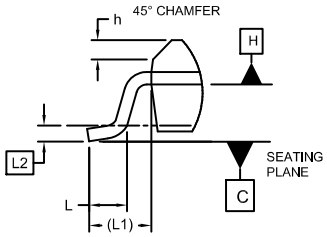
DATE 02 APR 2019

NOTES:

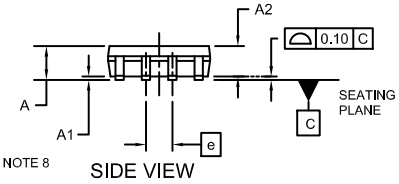
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



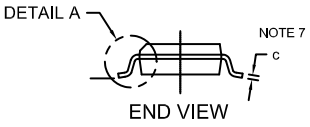
TOP VIEW



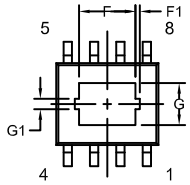
DETAIL A



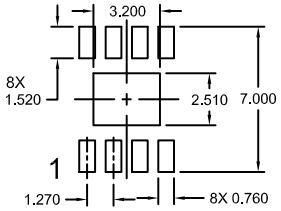
SIDE VIEW



END VIEW



BOTTOM VIEW

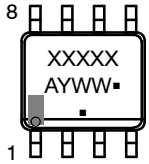


RECOMMENDED
MOUNTING FOOTPRINT*

DIM	MILLIMETERS		
	MIN.	NOM..	MAX.
A	1.35	1.55	1.75
A1	−−−	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1	0.15	0.20	0.25
G	1.55	2.03	2.51
G1	0.41	0.46	0.51
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
Ø	0°	4°	8°

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON14029D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC−8 EP	PAGE 1 OF 1

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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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