MIC7122

## Rail-to-Rail Dual Op Amp

## Features

- Small Footprint MSOP-8 Package
- 350 µA Supply Current per Op Amp at 2.2V Supply
- Guaranteed 2.2V, 5V, and 15V Performance
- 750 kHz Gain-Bandwidth Product at 2.2V Supply
- 0.01% Total Harmonic Distortion at 1 kHz (15V, 2 kΩ)
- Drives 200 pF at 5V and Greater Supply Voltages

## Applications

- Battery-Powered Instrumentation
- PCMCIA, USB Peripherals
- Portable Computers and PDAs

## General Description

The MIC7122 is a dual high-performance CMOS operational amplifier featuring rail-to-rail inputs and outputs.

The input common-mode range extends beyond the rails by 300 mV, and the output voltage swings to within 150 µV of both rails when driving a 100 kΩ load.

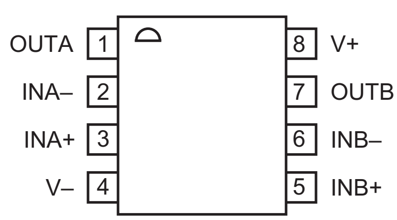
The amplifiers operate from 2.2V to 15V and are fully specified at 2.2V, 5V, and 15V. Gain bandwidth and slew rate are 750 kHz and 0.7 V/µs, respectively at a 2.2V supply.

The MIC7122 is available in an 8-lead MSOP package.

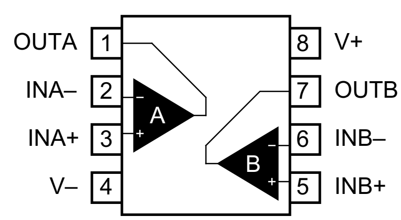
## Package Type

**MIC7122**
MSOP-8 (MM)

Pin Configuration




Functional Pinout



# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings †

Supply Voltage ($V_{V+}$ – $V_{V–}$) .......... +16.5V
Differential Input Voltage ($V_{IN+}$ – $V_{IN–}$) .......... ±10V
I/O Pin Voltage ($V_{IN}$, $V_{OUT}$ Note 1) .......... $V_{V+}$ + 0.3V to $V_{V–}$ – 0.3V
ESD Rating (Note 2) .......... 1 kV

## Operating Ratings ‡

Supply Voltage ($V_{V+}$ – $V_{V–}$) .......... +2.2V to +15V

**† Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

**‡ Notice:** The device is not guaranteed to function outside its operating ratings.

**Note 1:** I/O Pin Voltage is any external voltage to which an input or output is referenced.

**2:** Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

## DC ELECTRICAL CHARACTERISTICS (2.2V)

$V_{V+}$ = +2.2V, $V_{V-}$ = 0V, $V_{CM}$ = $V_{OUT}$ = $V_{V+}$/2; $R_L$ = 1 MΩ; $T_J$ = +25°C; Note 1.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | — | 0.5 | 9 | mV | — |
| Input Offset Voltage Average Drift | $TCV_{OS}$ | — | 3.0 | — | µV/°C | — |
| Input Bias Current | $I_B$ | — | 1.0 | 10 | pA | — |
| | | — | 64 | 500 | | –40°C ≤ $T_J$ ≤ +85°C |
| Input Offset Current | $I_{OS}$ | — | 0.5 | 5 | pA | — |
| | | — | 32 | 250 | | –40°C ≤ $T_J$ ≤ +85°C |
| Input Resistance | $R_{IN}$ | — | >1 | — | TΩ | — |
| Common-Mode Rejection Ratio | CMRR | 45 | 65 | — | dB | –0.3V ≤ $V_{CM}$ ≤ 2.5V, Note 2 |
| Power Supply Rejection Ratio | PSRR | 60 | 85 | — | dB | $V_{V+}$ = \|$V_{V-}$\| = 1.1V to 2.5V, $V_{OUT}$ = $V_{CM}$ = 0 |
| Common-Mode Input Capacitance | $C_{IN}$ | — | 3 | — | pF | — |
| Output Swing | $V_O$ | — | 0.15 | 1 | mV | Output high, $R_L$ = 100 kΩ, specified as $V_{V+}$ – $V_{OUT}$ |
| | | — | — | 1 | | Output high, $R_L$ = 100 kΩ, specified as $V_{V+}$ – $V_{OUT,}$ –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 0.15 | 1 | | Output low, $R_L$ = 100 kΩ |
| | | — | — | 1 | | Output low, $R_L$ = 100 kΩ, –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 8 | 33 | | Output high, $R_L$ = 2 kΩ, specified as $V_{V+}$ – $V_{OUT}$ |
| | | — | — | 50 | | Output high, $R_L$ = 2 kΩ, specified as $V_{V+}$ – $V_{OUT,}$ –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 8 | 33 | | Output low, $R_L$ = 2 kΩ |
| | | — | — | 50 | | Output low, $R_L$ = 2 kΩ –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 26 | 110 | | Output high, $R_L$ = 600Ω, specified as $V_{V+}$ – $V_{OUT}$ |
| | | — | — | 165 | | Output high, $R_L$ = 600Ω, specified as $V_{V+}$ – $V_{OUT,}$ –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 26 | 110 | | Output low, $R_L$ = 600Ω |
| | | — | — | 165 | | Output low, $R_L$ = 600Ω –40°C ≤ $T_J$ ≤ +85°C |
| Output Short-Circuit Current | $I_{SC}$ | 20 | 50 | — | mA | Sinking or sourcing, Note 3 |
| Supply Current | $I_S$ | — | 0.7 | 1.6 | mA | Both amplifiers |

**Note 1:** All limits guaranteed by testing or statistical analysis.

**2:** CMRR is determined as follows: The maximum $\Delta V_{OS}$ over the $V_{CM}$ range is divided by the magnitude of the $V_{CM}$ range. The measurement points are: $V_{CM}$ = $V_{V-}$ – 0.3V, ($V_{V+}$ – $V_{V-}$)/2, and $V_{V+}$ + 0.3V.

**3:** Continuous short circuit may exceed absolute maximum $T_J$ under some conditions.

## AC ELECTRICAL CHARACTERISTICS (2.2V)

$V_{V+}$ = +2.2V, $V_{V-}$ = 0V, $V_{CM}$ = $V_{OUT}$ = $V_{V+}$/2; $R_L$ = 1 MΩ; $T_J$ = +25°C; Note 1.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Slew Rate | SR | — | 0.7 | — | V/µs | — |
| Gain-Bandwidth Product | GBWP | — | 750 | — | kHz | — |
| Phase Margin | $\phi_m$ | — | 80 | — | ° | $C_L$ = 0 pF |
| | | — | 40 | — | | $C_L$ = 200 pF |
| Gain Margin | $G_M$ | — | 10 | — | dB | — |
| Interamplifier Isolation | — | — | 90 | — | dB | Note 2 |

**Note 1:** All limits guaranteed by testing or statistical analysis.
**2:** Referenced to input.

## DC ELECTRICAL CHARACTERISTICS (5V)

$V_{V+}$ = +5.0V, $V_{V-}$ = 0V, $V_{CM}$ = 1.5V, $V_{OUT}$ = $V_{V+}$/2; $R_L$ = 1 MΩ; $T_J$ = +25°C; Note 1.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | — | 0.5 | 9 | mV | — |
| Input Offset Voltage Average Drift | $TCV_{OS}$ | — | 3.0 | — | µV/°C | — |
| Input Bias Current | $I_B$ | — | 1.0 | 10 | pA | — |
| | | — | 64 | 500 | | –40°C ≤ $T_J$ ≤ +85°C |
| Input Offset Current | $I_{OS}$ | — | 0.5 | 5 | pA | — |
| | | — | 32 | 250 | | –40°C ≤ $T_J$ ≤ +85°C |
| Input Resistance | $R_{IN}$ | — | >1 | — | TΩ | — |
| Common-Mode Rejection Ratio | CMRR | 55 | 75 | — | dB | –0.3V ≤ $V_{CM}$ ≤ 5.3V, Note 2 |
| Power Supply Rejection Ratio | PSRR | 55 | 100 | — | dB | $V_{V+}$ = \|$V_{V-}$\| = 2.5V to 7.5V, $V_{OUT}$ = $V_{CM}$ = 0 |
| Common-Mode Input Capacitance | $C_{IN}$ | — | 3 | — | pF | — |

**Note 1:** All limits guaranteed by testing or statistical analysis.
**2:** CMRR is determined as follows: The maximum $\Delta V_{OS}$ over the $V_{CM}$ range is divided by the magnitude of the $V_{CM}$ range. The measurement points are: $V_{CM}$ = $V_{V-}$ – 0.3V, ($V_{V+}$ – $V_{V-}$)/2, and $V_{V+}$ + 0.3V.
**3:** Continuous short circuit may exceed absolute maximum $T_J$ under some conditions.

## DC ELECTRICAL CHARACTERISTICS (5V) (CONTINUED)

$V_{V+}$ = +5.0V, $V_{V-}$ = 0V, $V_{CM}$ = 1.5V, $V_{OUT}$ = $V_{V+}/2$; $R_L$ = 1 MΩ; $T_J$ = +25°C; Note 1.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Output Swing | $V_O$ | — | 0.3 | 1.0 | mV | Output high, $R_L$ = 100 kΩ, specified as $V_{V+} - V_{OUT}$ |
| | | — | — | 1.5 | | Output high, $R_L$ = 100 kΩ, specified as $V_{V+} - V_{OUT}$, –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 0.3 | 1.0 | | Output low, $R_L$ = 100 kΩ |
| | | — | — | 1.5 | | Output low, $R_L$ = 100 kΩ –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 13 | 50 | | Output high, $R_L$ = 2 kΩ, specified as $V_{V+} - V_{OUT}$ |
| | | — | — | 75 | | Output high, $R_L$ = 2 kΩ, specified as $V_{V+} - V_{OUT}$, –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 13 | 50 | | Output low, $R_L$ = 2 kΩ |
| | | — | — | 75 | | Output low, $R_L$ = 2 kΩ –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 40 | 165 | | Output high, $R_L$ = 600Ω, specified as $V_{V+} - V_{OUT}$ |
| | | — | — | 250 | | Output high, $R_L$ = 600Ω, specified as $V_{V+} - V_{OUT}$, –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 40 | 165 | | Output low, $R_L$ = 600Ω |
| | | — | — | 250 | | Output low, $R_L$ = 600Ω –40°C ≤ $T_J$ ≤ +85°C |
| Output Short-Circuit Current | $I_{SC}$ | 40 | 140 | — | mA | Sinking or sourcing, Note 3 |
| Supply Current | $I_S$ | — | 0.8 | 1.8 | mA | Both amplifiers |

**Note 1:** All limits guaranteed by testing or statistical analysis.

**2:** CMRR is determined as follows: The maximum $\Delta V_{OS}$ over the $V_{CM}$ range is divided by the magnitude of the $V_{CM}$ range. The measurement points are: $V_{CM} = V_{V-} - 0.3V$, $(V_{V+} - V_{V-})/2$, and $V_{V+} + 0.3V$.

**3:** Continuous short circuit may exceed absolute maximum $T_J$ under some conditions.

## AC ELECTRICAL CHARACTERISTICS (5V)

$V_{V+}$ = +5.0V, $V_{V-}$ = 0V, $V_{CM}$ = 1.5V, $V_{OUT}$ = $V_{V+}$/2; $R_L$ = 1 MΩ; $T_J$ = +25°C; Note 1.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Total Harmonic Distortion | THD | — | 0.05 | — | % | f = 1 kHz, $A_V$ = –2, $R_L$ = 2 kΩ, $V_{OUT}$ = 4.0 $V_{PP}$ |
| Slew Rate | SR | — | 0.6 | — | V/µs | — |
| Gain-Bandwidth Product | GBWP | — | 465 | — | kHz | — |
| Phase Margin | $\phi_m$ | — | 85 | — | ° | $C_L$ = 0 pF |
| | | — | 40 | — | | $C_L$ = 200 pF |
| Gain Margin | $G_M$ | — | 10 | — | dB | — |
| Interamplifier Isolation | — | — | 90 | — | dB | Note 2 |

**Note 1:** All limits guaranteed by testing or statistical analysis.
**2:** Referenced to input.

## DC ELECTRICAL CHARACTERISTICS (15V)

$V_{V+}$ = +15V, $V_{V-}$ = 0V, $V_{CM}$ = 1.5V, $V_{OUT}$ = $V_{V+}$/2; $R_L$ = 1 MΩ; $T_J$ = +25°C; Note 1.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | — | 0.5 | 9 | mV | — |
| Input Offset Voltage Average Drift | $TCV_{OS}$ | — | 3.0 | — | µV/°C | — |
| Input Bias Current | $I_B$ | — | 1.0 | 10 | pA | — |
| | | — | 64 | 500 | | –40°C ≤ $T_J$ ≤ +85°C |
| Input Offset Current | $I_{OS}$ | — | 0.5 | 5 | pA | — |
| | | — | 32 | 250 | | –40°C ≤ $T_J$ ≤ +85°C |
| Input Resistance | $R_{IN}$ | — | >1 | — | TΩ | — |
| Common-Mode Rejection Ratio | CMRR | 60 | 85 | — | dB | –0.3V ≤ $V_{CM}$ ≤ 15.3V, Note 2 |
| Power Supply Rejection Ratio | PSRR | 55 | 100 | — | dB | $V_{V+}$ = \|$V_{V-}$\| = 2.5V to 7.5V, $V_{OUT}$ = $V_{CM}$ = 0 |
| Large Signal Voltage Gain | $A_V$ | — | 340 | — | V/mV | Sourcing or sinking, $R_L$ = 2 kΩ, Note 3 |
| | | — | 300 | — | | Sourcing or sinking, $R_L$ = 600Ω, Note 3 |
| Common-Mode Input Capacitance | $C_{IN}$ | — | 3 | — | pF | — |

**Note 1:** All limits guaranteed by testing or statistical analysis.
**2:** CMRR is determined as follows: The maximum $\Delta V_{OS}$ over the $V_{CM}$ range is divided by the magnitude of the $V_{CM}$ range. The measurement points are: $V_{CM}$ = $V_{V-}$ – 0.3V, ($V_{V+}$ – $V_{V-}$)/2, and $V_{V+}$ + 0.3V.
**3:** $R_L$ connected to 7.5V. Sourcing: 7.5V ≤ $V_{OUT}$ ≤ 12.5V. Sinking: 2.5V ≤ $V_{OUT}$ ≤ 7.5V.
**4:** Continuous short circuit may exceed absolute maximum $T_J$ under some conditions.

## DC ELECTRICAL CHARACTERISTICS (15V) (CONTINUED)

$V_{V+}$ = +15V, $V_{V-}$ = 0V, $V_{CM}$ = 1.5V, $V_{OUT}$ = $V_{V+}$/2; $R_L$ = 1 MΩ; $T_J$ = +25°C; Note 1.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Output Swing | $V_O$ | — | 0.8 | 2 | mV | Output high, $R_L$ = 100 kΩ, specified as $V_{V+} - V_{OUT}$ |
| | | — | — | 3 | | Output high, $R_L$ = 100 kΩ, specified as $V_{V+} - V_{OUT}$, –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 0.8 | 2 | | Output low, $R_L$ = 100 kΩ |
| | | — | — | 3 | | Output low, $R_L$ = 100 kΩ, –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 40 | 80 | | Output high, $R_L$ = 2 kΩ, specified as $V_{V+} - V_{OUT}$ |
| | | — | — | 120 | | Output high, $R_L$ = 2 kΩ, specified as $V_{V+} - V_{OUT}$, –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 40 | 80 | | Output low, $R_L$ = 2 kΩ |
| | | — | — | 120 | | Output low, $R_L$ = 2 kΩ, –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 130 | 270 | | Output high, $R_L$ = 600Ω, specified as $V_{V+} - V_{OUT}$ |
| | | — | — | 400 | | Output high, $R_L$ = 600Ω, specified as $V_{V+} - V_{OUT}$, –40°C ≤ $T_J$ ≤ +85°C |
| | | — | 130 | 270 | | Output low, $R_L$ = 600Ω |
| | | — | — | 400 | | Output low, $R_L$ = 600Ω –40°C ≤ $T_J$ ≤ +85°C |
| Output Short-Circuit Current | $I_{SC}$ | 50 | 250 | — | mA | Sinking or sourcing, Note 4 |
| Supply Current | $I_S$ | — | 0.9 | 2.0 | mA | Both amplifiers |

**Note 1:** All limits guaranteed by testing or statistical analysis.

**2:** CMRR is determined as follows: The maximum $\Delta V_{OS}$ over the $V_{CM}$ range is divided by the magnitude of the $V_{CM}$ range. The measurement points are: $V_{CM} = V_{V-} - 0.3V$, $(V_{V+} - V_{V-})/2$, and $V_{V+} + 0.3V$.

**3:** $R_L$ connected to 7.5V. Sourcing: 7.5V ≤ $V_{OUT}$ ≤ 12.5V. Sinking: 2.5V ≤ $V_{OUT}$ ≤ 7.5V.

**4:** Continuous short circuit may exceed absolute maximum $T_J$ under some conditions.

## AC ELECTRICAL CHARACTERISTICS (15V)

$V_{V+}$ = +15V, $V_{V-}$ = 0V, $V_{CM}$ = 1.5V, $V_{OUT}$ = $V_{V+}/2$; $R_L$ = 1 MΩ; $T_J$ = +25°C; Note 1.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Total Harmonic Distortion | THD | — | 0.01 | — | % | f = 1 kHz, $A_V$ = –2, $R_L$ = 2 kΩ, $V_{OUT}$ = $8.5V_{PP}$ |
| Slew Rate | SR | — | 0.5 | — | V/µs | V+ = 15V, Note 2 |
| Gain-Bandwidth Product | GBWP | — | 420 | — | kHz | — |
| Phase Margin | $\phi_m$ | — | 85 | — | ° | $C_L$ = 0 pF |
| | | — | 40 | — | | $C_L$ = 200 pF |
| Gain Margin | $G_M$ | — | 10 | — | dB | — |
| Input-Referred Voltage Noise | $e_n$ | — | 37 | — | nV/√Hz | f = 1 kHz, $V_{CM}$ = 1V |
| Input-Referred Current Noise | $i_n$ | — | 1.5 | — | fA/√Hz | f = 1 kHz |
| Interamplifier Isolation | — | — | 90 | — | dB | Note 3 |

**Note 1:** All limits guaranteed by testing or statistical analysis.

**2:** Device connected as a voltage follower with a 10V step input. The value is the positive or negative slew rate, whichever is slower.

**3:** Referenced to input.

## TEMPERATURE SPECIFICATIONS

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Operating Junction Temperature Range | $T_J$ | –40 | — | +125 | °C | — |
| Storage Temperature | $T_S$ | –65 | — | +150 | °C | — |
| Maximum Junction Temperature Range | $T_J$ | — | — | +150 | °C | — |
| Lead Temperature | — | — | — | +260 | °C | Soldering, 10 sec. |
| Maximum Power Dissipation | — | — | — | — | — | — |
| **Package Thermal Resistance** | | | | | | |
| MSOP-8 | $\theta_{JA}$ | — | 200 | — | °C/W | Note 1 |

**Note 1:** Thermal resistance, $\theta_{JA}$, applies to a part soldered on a printed-circuit board.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | OUTA | Op Amp A Output. |
| 2 | INA– | Op Amp A Inverting Input. |
| 3 | INA+ | Op Amp A Non-Inverting Input. |
| 4 | V– | Negative Supply: Negative supply for split supply application or ground for single supply applications. |
| 5 | INB+ | Op Amp B Non-Inverting Input. |
| 6 | INB– | Op Amp B Inverting Input. |
| 7 | OUTB | Op Amp B Output. |
| 8 | V+ | Positive Supply. |

# 3.0 APPLICATION INFORMATION

## 3.1 Input Common-Mode Voltage

The MIC7122 tolerates input overdrive by at least 300 mV beyond either rail without producing phase inversion.

If the absolute maximum input voltage is exceeded, the input current should be limited to ±5 mA maximum to prevent reducing reliability. A 10 kΩ series input resistor, used as a current limiter, will protect the input structure from voltages as large as 50V above the supply or below ground. See Figure 3-1.

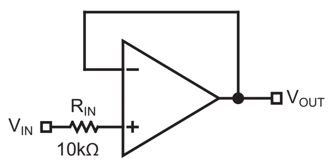



*FIGURE 3-1: Input Current-Limit Protection.*

## 3.2 Output Voltage Swing

Sink and source output resistances of the MIC7122 are equal. Maximum output voltage swing is determined by the load and the approximate output resistance. The output resistance is:

**EQUATION 3-1:**

$$R_{OUT} = \frac{V_{DROP}}{I_{LOAD}}$$

$V_{DROP}$ is the voltage dropped within the amplifier output stage. $V_{DROP}$ and $I_{LOAD}$ can be determined from the $V_O$ (output swing) portion of the appropriate Electrical Characteristics table. $I_{LOAD}$ is equal to the typical output high voltage minus V+/2 and divided by $R_{LOAD}$. For example, using the DC Electrical Characteristics (5V) table, the typical output high voltage drops 13 mV using a 2 kΩ load (connected to V+/2), which produces an $I_{LOAD}$ of:

**EQUATION 3-2:**

$$\frac{5.0V - 0.013V - 2.5V}{2k\Omega} = 1.244mA$$

Because of output stage symmetry, the corresponding typical output low voltage (13 mV) also equals $V_{DROP}$. Then:

**EQUATION 3-3:**

$$R_{OUT} = \frac{0.013V}{0.001244A} = 10.5\Omega$$

## 3.3 Power Dissipation

The MIC7122 output drive capability requires considering power dissipation. If the load impedance is low, it is possible to damage the device by exceeding the 125°C junction temperature rating.

On-chip power consists of two components: supply power and output stage power. Supply power ($P_S$) is the product of the supply voltage ($V_S = V_{V+} – V_{V–}$) and supply current ($I_S$). Output stage power ($P_O$) is the product of the output stage voltage drop ($V_{DROP}$) and the output (load) current ($I_{OUT}$).

Total on-chip power dissipation is:

**EQUATION 3-4:**

$$P_D = P_S + P_O$$

Where:
$P_D$ = Total On-Chip Power
$P_S$ = Supply Power Dissipation
$P_O$ = Output Power Dissipation

**EQUATION 3-5:**

$$P_D = (V_S \times I_S) + (V_{DROP} \times I_{OUT})$$

Where:
$V_S = V_{V+} – V_{V–}$
$I_S$ = Power Supply Current
$V_{DROP} = V_{V+} – V_{OUT}$ (Sourcing Current)
$V_{DROP} = V_{OUT} – V_{V–}$ (Sinking Current)

Equation 3-4 and Equation 3-5 address only steady state (DC) conditions. For non-DC conditions, the user must estimate power dissipation based on the RMS value of the signal.

The task is one of determining the allowable on-chip power dissipation for operation at a given ambient temperature and power supply voltage. From this determination, one may calculate the maximum allowable power dissipation and, after subtracting $P_S$, determine the maximum allowable load current, which in turn can be used to determine the minimum load impedance that may safely be driven. The calculation is summarized below in Equation 3-6.

**EQUATION 3-6:**

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

$\theta_{JA(MSOP-8)}$ = 200°C/W

## 3.4 Driving Capacitive Loads

Driving a capacitive load introduces phase lag into the output signal and this, in turn, reduces op-amp system phase margin.

The application that is least forgiving of reduced phase margin is a unity gain amplifier. The MIC7122 can typically drive a 200 pF capacitive load connected directly to the output when configured as a unity-gain amplifier and powered with a 2.2V supply. At 15V operation the circuit typically drives 500 pF.

## 3.5 Using Large-Value Feedback Resistors

A large-value feedback resistor (>500 kΩ) can reduce the phase margin of a system. This occurs when the feedback resistor acts in conjunction with input capacitance to create phase lag in the feedback signal. Input capacitance is usually a combination of input circuit components and other parasitic capacitance, such as amplifier input capacitance and stray printed circuit board capacitance.

Figure 3-2 illustrates a method of compensating phase lag caused by using a large-value feedback resistor. Feedback capacitor $C_{FB}$ introduces sufficient phase lead to overcome the phase lag caused by feedback resistor $R_{FB}$ and input capacitance $C_{IN}$. The value of $C_{FB}$ is determined by first estimating $C_{IN}$ and then applying the following formula:

**EQUATION 3-7:**

$$R_{IN} \times C_{IN} \le R_{FB} \times C_{FB}$$

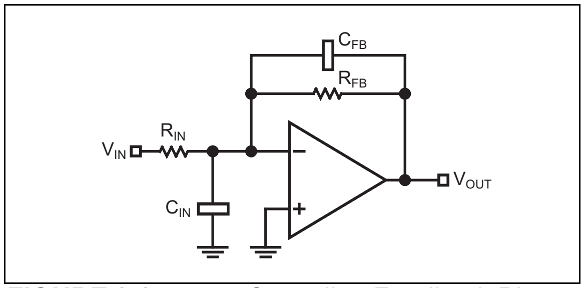



***FIGURE 3-2:*** *Canceling Feedback Phase Lag.*

Because a significant percentage of $C_{IN}$ may be caused by board layout, it is important to note that the correct value of $C_{FB}$ may change when changing from a breadboard to the final circuit layout.

## 3.6 Typical Circuits

Some single-supply, rail-to-rail applications for which the MIC7122 is well suited are shown in the circuit diagrams of Figure 3-3 through Figure 3-8.

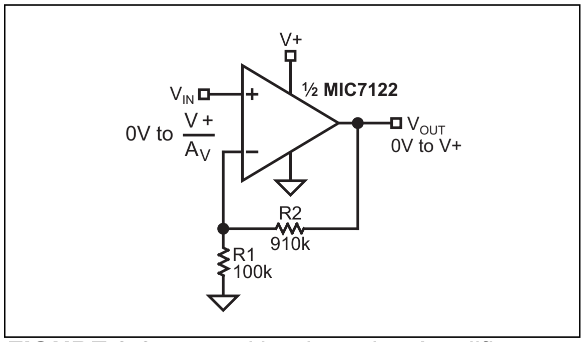



***FIGURE 3-3:*** *Non-Inverting Amplifier.*

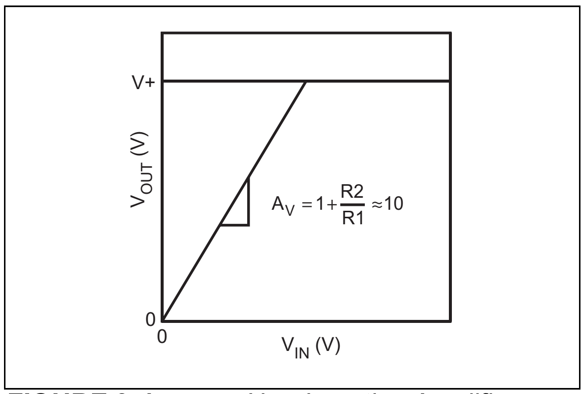



***FIGURE 3-4:*** *Non-Inverting Amplifier Behavior.*

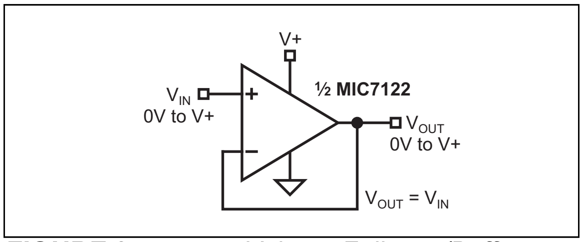



*FIGURE 3-5: Voltage Follower/Buffer.*

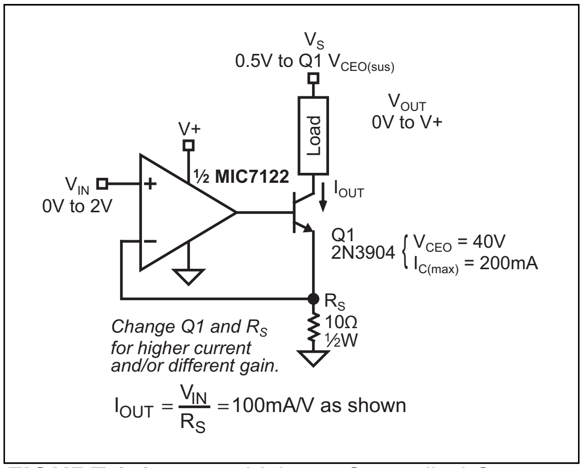



*FIGURE 3-6: Voltage-Controlled Current Sink.*

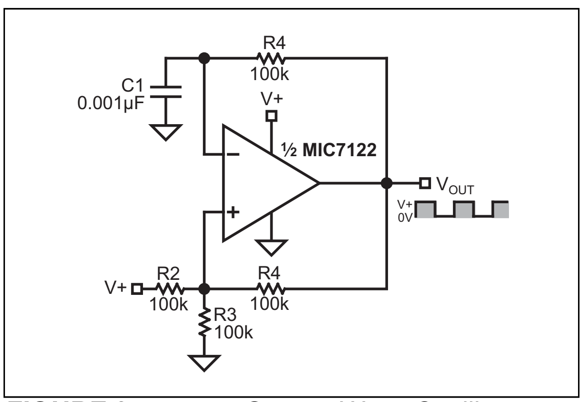



*FIGURE 3-7: Square Wave Oscillator.*

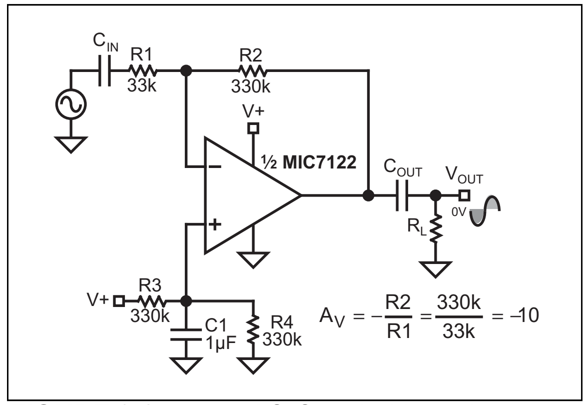
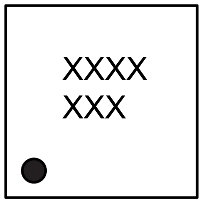



*FIGURE 3-8: AC-Coupled Inverting Amplifier.*

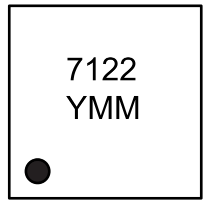
# 4.0 PACKAGE MARKING INFORMATION

## 4.1 Package Marking Information

8-Lead MSOP*
(FRONT)

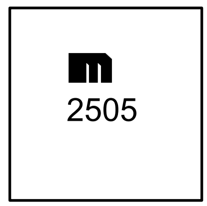



Example




8-Lead MSOP*
(BACK)


Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Product code or customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

●, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

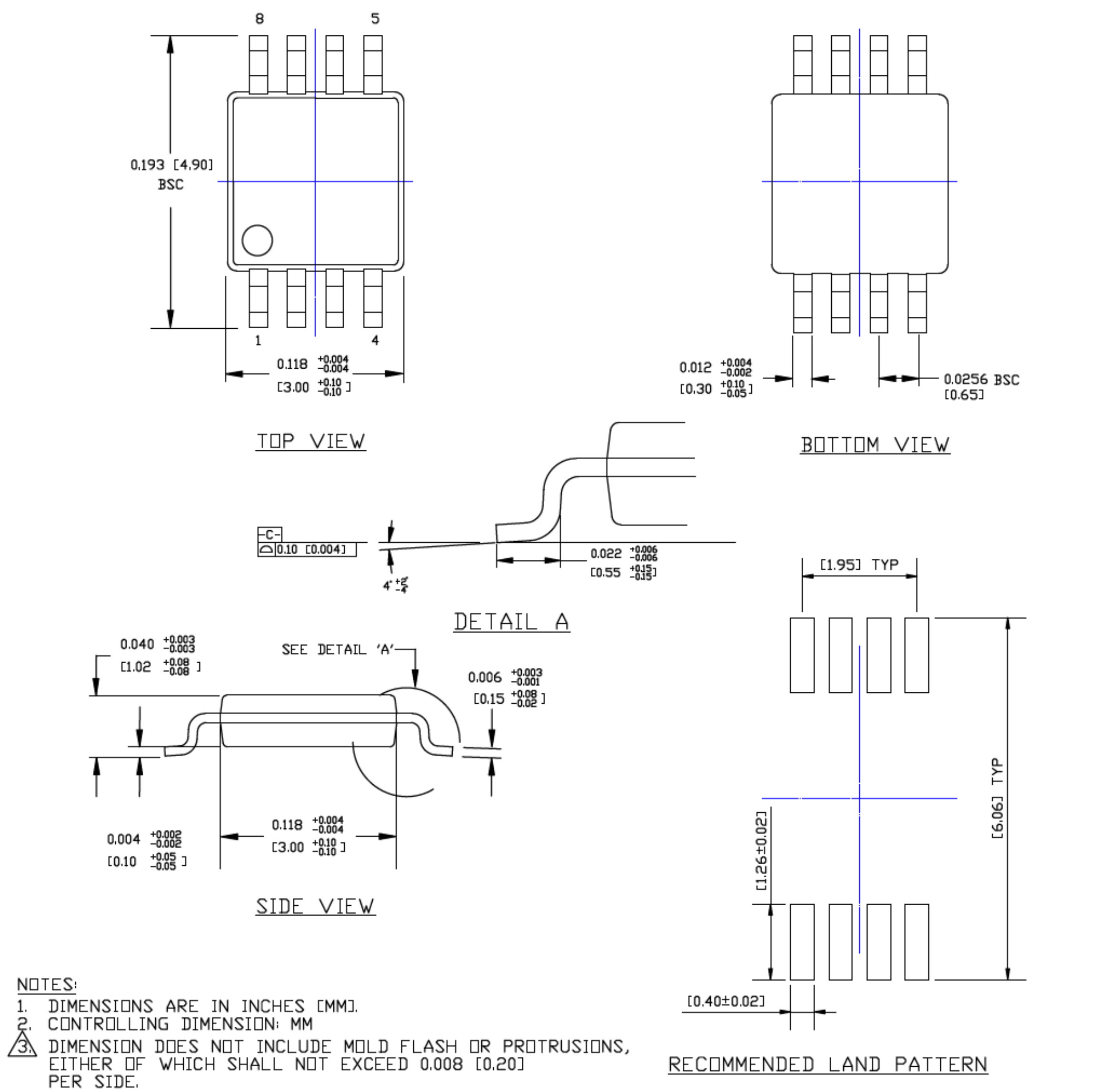
Underbar (_) and/or Overbar (‾) symbol may not be to scale.

## 8-Lead MSOP Package Outline and Recommended Land Pattern

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|

**TITLE**
8 LEAD MSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| **DRAWING #** | MSOP-8LD-PL-1 | **UNIT** | INCH [MM] |
|---|---|---|---|



**NOTES:**

# APPENDIX A: REVISION HISTORY

## Revision A (January 2020)

- Converted Micrel data sheet MIC7122 to Microchip DS20006290A.
- Minor text changes throughout.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | X | XX | -XX |
|---|---|---|---|
| Device | Temperature Range | Package | Media Type |

| | | |
|---|---|---|
| **Device:** | MIC7122: | Rail-to-Rail Dual Op Amp |
| **Temperature Range:** | Y = | –40°C to +85°C (Industrial) |
| **Package:** | MM = | 8-Pin MSOP |
| **Media Type:** | <blank>=<br>TR = | 100/Tube<br>2,500/Reel |

**Examples:**

| | |
|---|---|
| a) MIC7122YMM: | Rail-to-Rail Dual Op Amp, –40°C to +85°C Temperature Range, 8-Lead MSOP, 100/Tube |
| b) MIC7122YMM-TR: | Rail-to-Rail Dual Op Amp, –40°C to +85°C Temperature Range, 8-Lead MSOP, 2500/Reel |

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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