Keywords: BERT, DS2172, pattern, synchronization

APPLICATION NOTE 333

DS2172 Pattern Synchronization

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Abstract: This application note describes the operation of pattern synchronization of the DS2172 BERT.

Introduction

The DS2172 can be used to generate repetitive patterns up to 32 bits in length. Synchronizer operation differs in this mode from the pseudorandom pattern mode. In the repetitive pattern mode, the receiver looks for a repeating pattern of the same length (or multiple of) as the one being transmitted. It does not verify a pattern match with what is being transmitted. Once it has found a pattern of the same length it declares synchronization and counts any deviations in that pattern, not the one being transmitted, as bit errors. An all-zero or all-ones pattern received at RDATA emulates any length pattern, and the DS2172 synchronizes to it no matter what has been programmed into the pattern set register. Consider the following examples where the pattern at RDATA emulates the 6-bit pattern programmed into the transmitter.

Transmit pattern 101110
Received pattern 000000 synchronizes
Received pattern 111111 synchronizes
Received pattern 101010 synchronizes
Received pattern 111010 synchronizes

After synchronization has been established it is up to the user to check the pattern receive register to verify that the correct pattern is being received. The pattern in these registers is likely shifted one or more positions from the pattern in the pattern set registers. The flow chart in **Figure 1** describes the basic algorithm that verifies that the received pattern is the same as the transmitted pattern. Additionally, the received-all-zeros and received-all-ones indicators within the status register can be used to verify pattern synchronization. The user should always check the status register after synchronization to ensure the system is operating as expected.

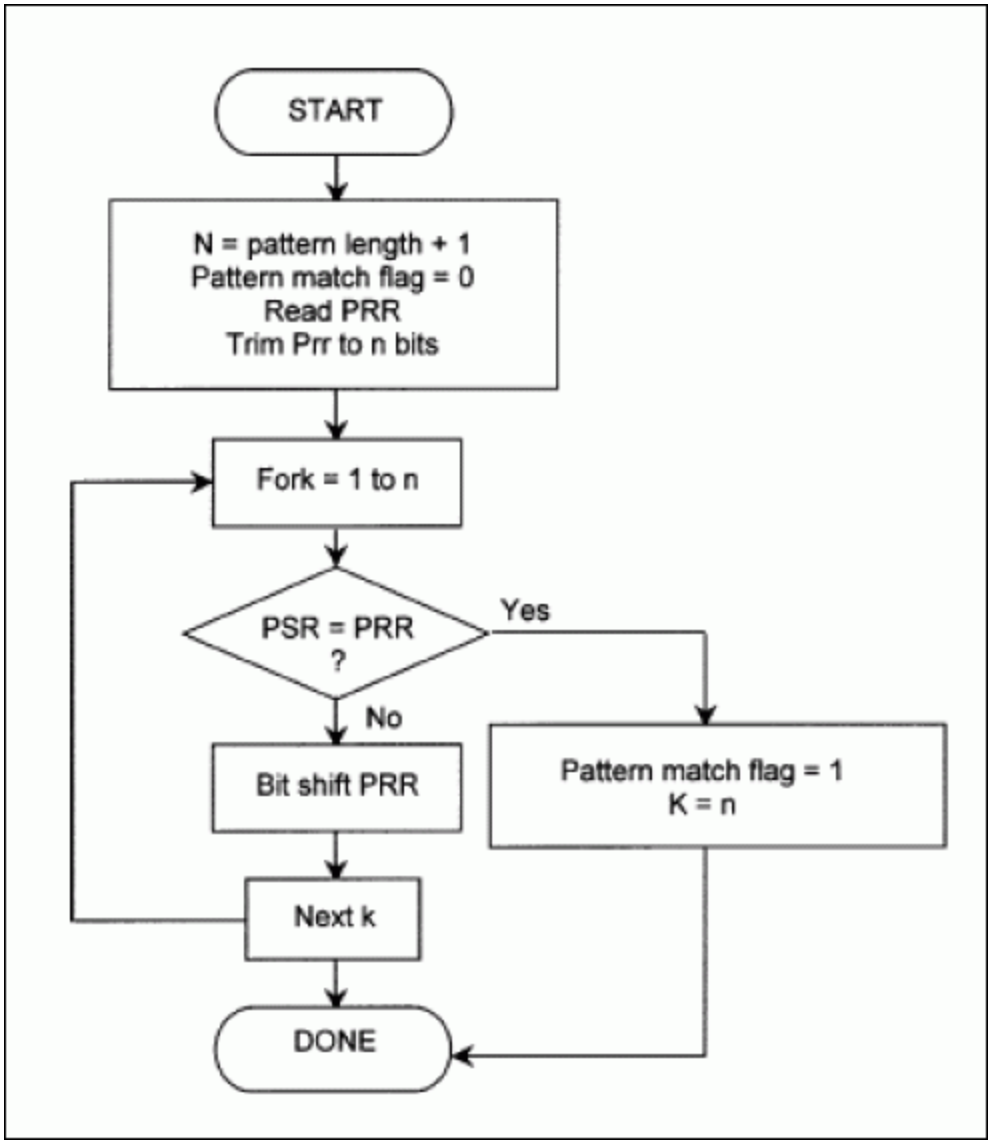

Figure 1. Algorithm for comparing received pattern with transmitted pattern.

The bit count register and the bit error-count register are inhibited during a loss-of-sync condition.

Once sync is established, the bit count register increments on every RCLK. The bit error-count register increments for every bit error in the pattern to which the receiver synchronized.

Both receive and transmit functions operate off RCLK and TCLK, respectively. Typically events such as latch count, transmit load, and receive data load are triggered off the rising edge of the clocks. These operations may take several clock cycles to complete. At low clock rates and high processor speeds, the user should allow for sufficient time for operations such as reading the counters to take place. Also note that using RDIS and TDIS to gap the receive and transmit signal inhibits all associated functions in the device.

DS2172 Information

If you have further questions on DS2172 pattern synchronization, please contact the Telecommunication Applications support team.

For more information about the DS2172, please consult the DS2172 data sheet.

Related Parts		
DS2172	Bit Error Rate Tester (BERT)	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/support
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