ARM® Cortex®-M

**32-bit Microcontroller**

# NuMicro® Family
# Nano103 Series
# Datasheet

For additional information or questions, please contact:Nuvoton Technology Corporation.

www.nuvoton.com

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# 1 GENERAL DESCRIPTION

The Nano103 series ultra-low-power 32-bit microcontroller embeded with ARM® Cortex®-M0 core operates at low voltage ranged from 2.2V to 3.6V and runs up to 36 MHz frequency with 64 Kbytes embedded Flash (APROM) and 16 Kbytes embedded SRAM and 4 Kbytes Flash loader memory (LDROM) for In-System Programming (ISP).

The Nano103 series integrates RTC with independent $V_{BAT}$ pin, 12-bit SAR ADC, comparator and provides high performance connectivity peripheral interfaces such as UART, SPI, I$^2$C, GPIOs, and ISO-7816-3 for Smart card.

The Nano103 series supports main power off with only $V_{BAT}$ and RTC on less than 1.0 uA and Deep Power-down mode with RAM retention is less than 1.6 uA and fast wake-up via many peripheral interfaces.

The Nano103 series provides low voltage, low operating power consumption, low standby current, high integration peripherals, high-efficiency operation, fast wake-up function and the lowest cost 32-bit microcontrollers. The Nano103 series is suitable for a wide range of battery device applications such as:

- Hand-Held Medical Device
- Wearable Device & Smart Watch
- Wireless Gaming Control, Thermostats, Sensors Node Device (WSND)
- Wireless Auto Meter Reading (AMR)
- RFID Reader
- Portable Wireless Data Collector
- Mobile Payment Smart Card Reader
- Security Alarm System
- Smart Home Appliance
- Smart Water, Gas, Heat Meters

## 1.1 Connectivity Support Table

| Product Line | UART | SPI | I$^2$C | ADC | ACMP | RTC/V$_{bat}$ | SC | Timer |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| Nano103 | ● | ● | ● | ● | ● | ● | ● | ● |

Table 1.1-1 Connectivity Support Table

## 2 FEATURES

- Low Supply Voltage Range: 2.2V to 3.6V

- Operating Temperature: -40℃~105℃

- Four power modes

  ◆ Normal mode

  ◆ Idle mode

  ◆ Power-down mode with RTC on and RAM retention

  ◆ RTC domain only

- Wake-up sources

  ◆ RTC, WDT, I²C, Timer, UART, SPI, BOD, GPIO

- Fast wake-up from power-down mode: less than 3.5 µs when using HIRC0

- Brown-out

  ◆ Built-in 1.7~3.1V BOD for wide operating voltage range operation

  ◆ Built-in low power 2.0/2.5V BOD

- Core

  ◆ ARM® Cortex®-M0 core running up to 36 MHz

  ◆ One 24-bit system timer

  ◆ Supports Low Power Sleep mode

  ◆ Single-cycle 32-bit hardware multiplier

  ◆ NVIC for the 32 interrupt inputs, each with 4-levels of priority

  ◆ Serial Wire Debug supports with 2 watchpoints/4 breakpoints

- Flash EPROM Memory

  ◆ 64 Kbytes application program memory (APROM)

  ◆ 4 Kbytes in system programming (ISP) loader program memory (LDROM)

  ◆ Programmable data flash start address and memory size with 512 bytes page erase unit

  ◆ In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM

- SRAM Memory

  ◆ 16 Kbytes embedded SRAM

  ◆ Supports DMA mode

- DMA: Supports Five channels includingfour PDMA channels and one CRC channel

  ◆ PDMA

    ■ Three modes: peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer

    ■ Source address and destination address must be word alignment in all modes.

    ■ Memory-to-memory mode: transfer length must be word alignment.

    ■ Peripheral-to-memory and memory-to-peripheral mode: transfer length

could be word/half-word/byte alignment.

■ Peripheral-to-memory and memory-to-peripheral mode: transfer data width could be word/half-word/byte alignment

■ Supports source and destination address direction: increment, fixed, and wrap around

◆ CRC

■ Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32

◆ CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$

◆ CRC-8: $X^8 + X^2 + X + 1$

◆ CRC-16: $X^{16} + X^{15} + X^2 + 1$

◆ CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

● Clock Control

◆ Built-in 12/16MHz OSC (HIRC0) has 2 % deviation within all temperarure range. Deviation could be reduced to 1% if turning on auto-trim function.

◆ Built-in 36MHz OSC(HIRC1)

◆ Built-in 4MHz OSC(MIRC)

◆ Supports one PLL, up to 36 MHz, for high performance system operation

◆ External 4~24 MHz(HXT) crystal input for precise timing operation

◆ Low power 10 kHz OSC(LIRC) for watchdog and low power system operation

◆ External 32.768 kHz(LXT) crystal input for RTC and low power system operation

● GPIO

◆ Three I/O modes:

■ Push-Pull output

■ Open-Drain output

■ Input only with high impendence

◆ All inputs with Schmitt trigger

◆ I/O pin configured as interrupt source with edge/level setting

◆ Supports input 5V tolerance, except

■ PA.0 ~ PA.7 (sharing pin with ADC),

■ PA.12~ PA.13 (sharing pin with comparator),

■ PF.0~ PF.1 and PF.6 ~ PF.7(sharing pin with HXT and LXT)

■ PA.8, PB.4 and PB.5

● Timer

◆ Supports 4 sets of 32-bit timers, each timer with 24-bit up-counting timer and one 8-bit pre-scale counter

◆ Each timer could have independent clock source selection

◆ Supports one-shot,periodic, output toggle and continuous operation modes

◆ Internal trigger event to ADC and PDMA

◆ Supports PDMA mode

◆ Wake system up from Power-down mode

● Watchdog Timer

◆ Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)

◆ Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)

◆ Interrupt or reset selectable when watchdog time-out

◆ Wakes system up from Power-down mode

● Window Watchdog Timer(WWDT)

◆ 6-bit down counter and 6-bit compare value to make the window period flexible

◆ Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.

● RTC

◆ Supports software compensation by setting frequency compensate register (FREQADJ)

◆ Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)

◆ Supports Alarm registers (second, minute, hour, day, month, year)

◆ Selectable 12-hour or 24-hour mode

◆ Automatic leap year recognition

◆ Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second

◆ Wake system up from Power-down mode

◆ Supports 20 bytes spare registers and a tamper pin to clear the content of these spare registers

◆ Supports 1 Hz clock output

◆ Support independent $V_{BAT}$ power domain to provide for PF.6~PF.7 (sharing pin with LXT) and tamper pins (LQFP64: PB.13/LQFP48: PA.9/QFN32: PB.8)

● PWM/Capture

◆ Supports one PWM module to provides 6 output channels

◆ Supports independent mode for PWM output/Capture input channe

◆ Supports complementary mode for 3 complementary paired PWM output channel

◆ Supports 16-bit resolution PWM counter, each module provides 3 PWM counters

◆ Supports PWM triggerADC function

◆ Supports up to 12 capture input channels with 16-bit resolution

● UART

◆ Supports up to two sets of UART

◆ Up to 1 Mbit/s baud rate

◆ Support 9600 baud rate at 32.768 kHz

- ◆ Up to two 16-byte FIFO UART controllers
- ◆ UART ports with flow control (TX, RX, nCTS and nRTS)
- ◆ Supports IrDA (SIR) function
- ◆ Supports LIN function
- ◆ Supports RS-485 9 bit mode and direction control.
- ◆ Programmable baud rate generator
- ◆ Supports PDMA mode
- ◆ Supports wake-up function (nCTS, incoming RX data, RS-485 AAD mode address matched or received FIFO is equal to the RFITL)

- ● SPI
  - ◆ Up to two sets of SPI controllers
  - ◆ Supports Master (max. 32 MHz) or Slave (max. 16 MHz) mode operation
  - ◆ Supports 1 bit and 2 bit transfer mode
  - ◆ Support Dual IO transfer mode
  - ◆ Configurable bit length of a transaction from 8 to 32-bit
  - ◆ Supports MSB first or LSB first transfer sequence
  - ◆ Two slave select lines supported in Master mode
  - ◆ Configurable byte or word suspend mode
  - ◆ Supports byte re-ordering function
  - ◆ Supports variable serial clock in Master mode
  - ◆ Provide separate 8-level depth transmit and receive FIFO buffer
  - ◆ Supports wake-up function(SPI clock toggle in Power-down mode)
  - ◆ Supports PDMA transfer
  - ◆ Supports 3-wires, no slave select signal, bi-direction interface

- ● $I^2C$
  - ◆ Up to two sets of $I^2C$ device
  - ◆ Master/Slave up to 1 Mbit/s
  - ◆ Bi-directional data transfer between masters and slaves
  - ◆ Multi-master bus (no central master)
  - ◆ Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - ◆ Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - ◆ Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - ◆ Built-in 14-bit time-out counter requesting the $I^2C$ interrupt if the $I^2C$ bus hangs up and timer-out counter overflows
  - ◆ Programmable clocks allowing for versatile rate control
  - ◆ Supports 7-bit addressing mode

- Supports multiple address recognition (four slave addresses with mask option)
- Wake system up(address match) from Power-down mode

- ADC
  - 12-bit SAR ADC
  - Up to 12 channels: 8 external channel(PA.0 ~ PA.6 and PC.7) and 4 internal channels.
  - Four internal channels: internal reference voltage (Int_$V_{REF}$), Temperature sensor, $AV_{DD}$, and $AV_{SS}$.
  - Supports three reference voltage sources: $V_{REF}$ pin, internal reference voltage (Int_$V_{REF}$: 2.5V/1.8V/1.5V), and $AV_{DD}$.
  - Supports Single Scan, Single Cycle Scan, and Continuous Scan mode
  - Each channel with individual result register
  - Threshold voltage detection (comparator function)
  - Conversion started by software programming or external input
  - Supports PDMA mode
  - Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3) to enable ADC

- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separates receive/transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 267 ETU)
  - A 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
  - Supports UART mode (full–duplex)

- ACMP
  - Supports one comparator
  - Analog input voltage range: 0~$AV_{DD}$
  - Supports Hysteresis function

- 96-bit unique ID

- 128-bit unique customer ID

- Packages:
  - ◆ All Green package (RoHS)
  - ◆ LQFP 64-pin(7x7)
  - ◆ LQFP 48-pin(7x7)
  - ◆ QFN 33-pin(5x5)

## 3   ABBREVIATIONS

| Acronym | Description |
|---------|-------------|
| ACMP | Analog Comparator Controller |
| ADC | Analog-to-Digital Converter |
| AES | Advanced Encryption Standard |
| APB | Advanced Peripheral Bus |
| AHB | Advanced High-Performance Bus |
| BOD | Brown-out Detection |
| CAN | Controller Area Network |
| DAP | Debug Access Port |
| DES | Data Encryption Standard |
| EBI | External Bus Interface |
| EPWM | Enhanced Pulse Width Modulation |
| FIFO | First In, First Out |
| FMC | Flash Memory Controller |
| FPU | Floating-point Unit |
| GPIO | General-Purpose Input/Output |
| HCLK | The Clock of Advanced High-Performance Bus |
| HIRC | 12/16 MHz Internal High Speed RC Oscillator |
| HXT | 4~24 MHz External High Speed Crystal Oscillator |
| IAP | In Application Programming |
| ICP | In Circuit Programming |
| ISP | In System Programming |
| LDO | Low Dropout Regulator |
| LIN | Local Interconnect Network |
| LIRC | 10 kHz internal low speed RC oscillator (LIRC) |
| MPU | Memory Protection Unit |
| NTC | Negative Temperature Coefficient |
| NVIC | Nested Vectored Interrupt Controller |
| PCLK | The Clock of Advanced Peripheral Bus |
| PDMA | Peripheral Direct Memory Access |
| PLL | Phase-Locked Loop |
| PTC | Positive Temperature Coefficient |
| PT1000 | Thermal Resistance |
| PWM | Pulse Width Modulation |

| QEI | Quadrature Encoder Interface |
|-----|------------------------------|
| SDIO | Secure Digital Input/Output |
| SPI | Serial Peripheral Interface |
| SPS | Samples per Second |
| TDES | Triple Data Encryption Standard |
| TMR | Timer Controller |
| UART | Universal Asynchronous Receiver/Transmitter |
| UCID | Unique Customer ID |
| USB | Universal Serial Bus |
| WDT | Watchdog Timer |
| WWDT | Window Watchdog Timer |

Table 1.1-1 List of Abbreviations

## 4   PARTS INFORMATION LIST AND PIN CONFIGURATION

### 4.1 NuMicro® Nano103 Series Selection Code

NANO 1 0 3 - X X X A E

**Ultra-low Power M0**

**Product  Line  Function**
1 : Base Line

**Package Type**

Z : QFN 33  (5x5mm.0.5mm pitch)
L : LQFP 48  (7x7mm,0.5mm pitch)
S : LQFP 64  (7x7mm,0.4mm pitch)

**Temperature**

E :- 40℃ ~ +105℃

**Version**
A : Version

**SRAM Size**
1 :   4KB
2 :   8KB
3 :   16KB

**Flash ROM**
B:   16KB
C:   32KB
D:   64KB
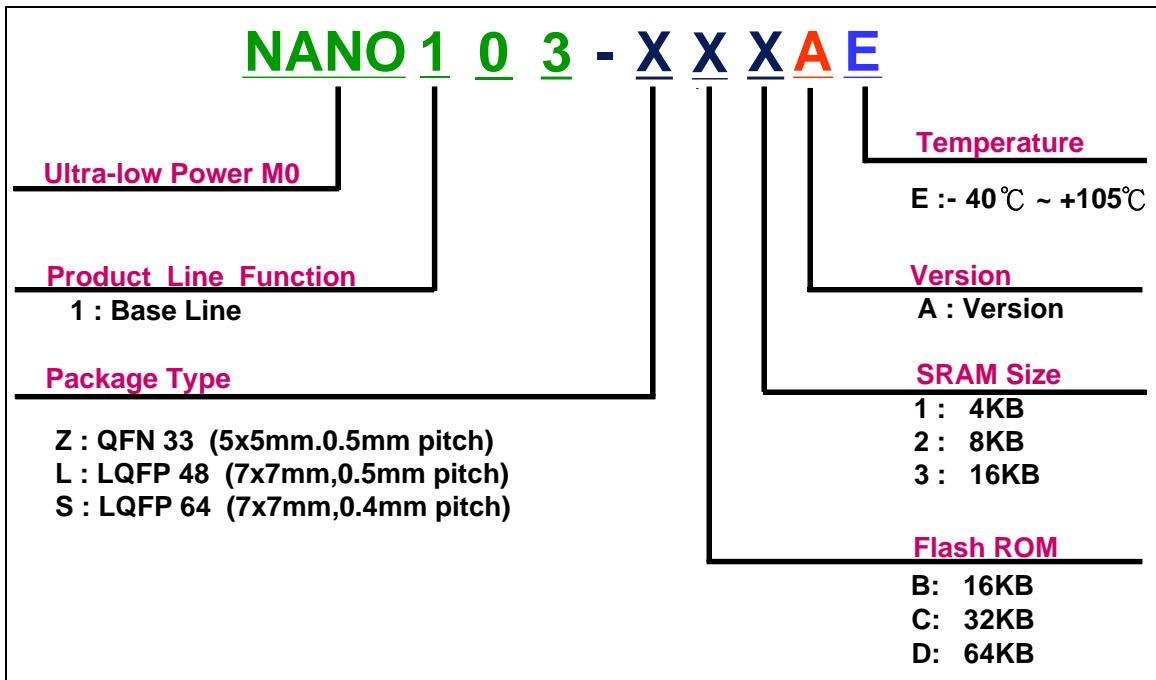
Figure 4.1-1 NuMicro® Nano103 Series Selection Code

### 4.2 NuMicro® Nano103 Products Selection Guide

#### 4.2.1    NuMicro® Nano103 Base Line Selection Guide

| Part No. | Flash (KB) | SRAM (KB) | Data Flash Shared AP ROM (KB) | LDROM (ISP Loader) (KB) | I/O | Timer | Connectivity | | | I²S | PWM | 12-bit ADC | ACMP | RTC | IRC 10 kHz 4 MHz 12/16 MHz 36 MHz | PDMA | ISO-7816-3* | ISP/ICP | Package |
| | | | | | | | UART* | SPI | I²C | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NANO103ZD3AE | 64 | 16 | Configurable | 4 | 26 | 4x32-bit | 2+2 | 4 | 2 | - | 2 | 6 | 1 | V | V | 4 | 2 | V | QFN33 |
| NANO103LD3AE | 64 | 16 | Configurable | 4 | 39 | 4x32-bit | 2+2 | 4 | 2 | - | 6 | 8 | 1 | V | V | 4 | 2 | V | LQFP48 |
| NANO103SD3AE | 64 | 16 | Configurable | 4 | 53 | 4x32-bit | 2+2 | 4 | 2 | - | 6 | 8 | 1 | V | V | 4 | 2 | V | LQFP64 |

*Marked in the table (2+2) means 2 UART + 2 ISO-7816 UART
*ISO-7816 UART supports UART full duplex mode

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## 4.3 Pin Configuration

### 4.3.1    NuMicro® Nano103 Pin Diagrams

*4.3.1.1    NuMicro® Nano103 LQFP 64-pin*
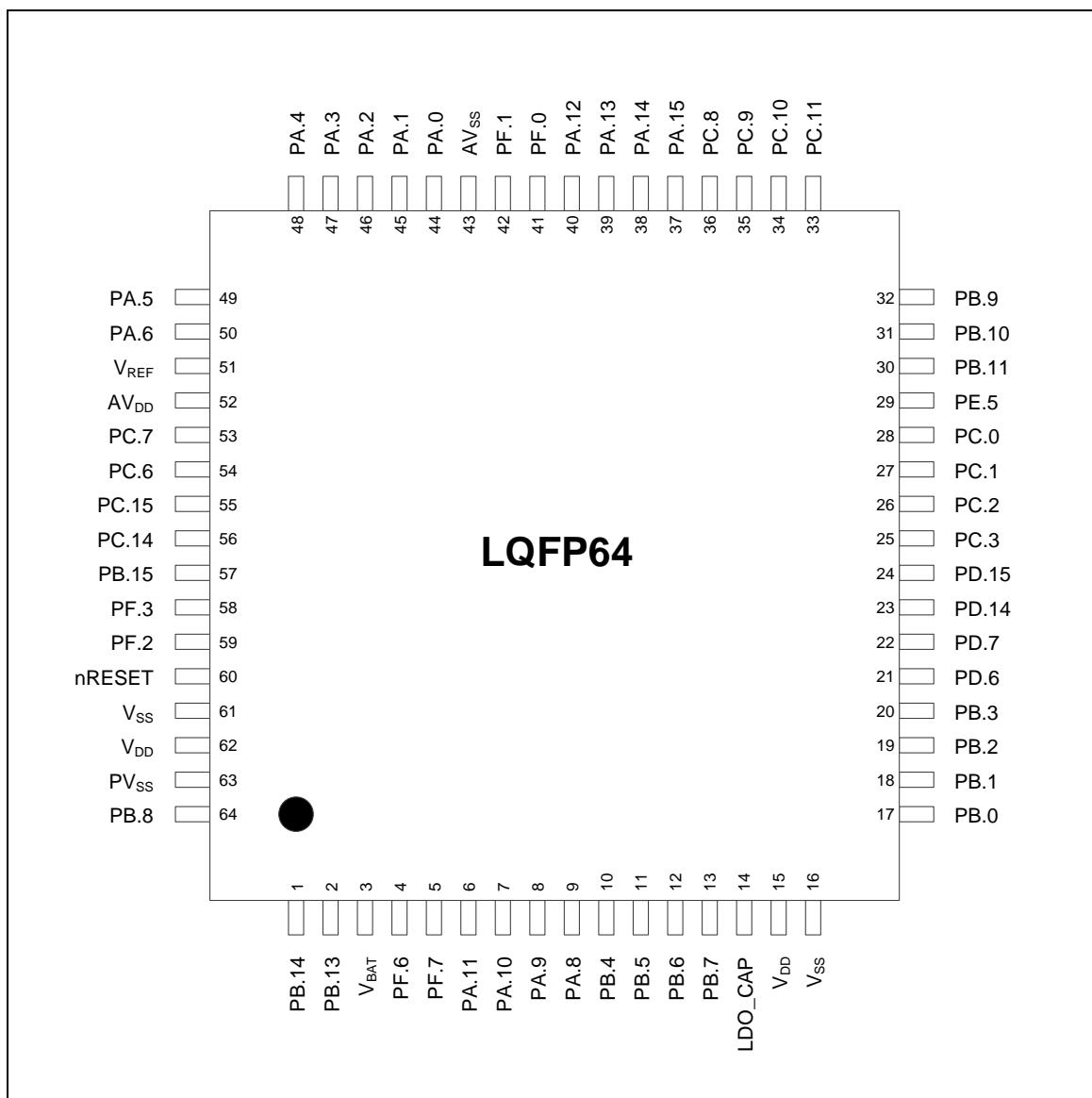


Figure 4.3-1 NuMicro® Nano103 LQFP 64-pin Diagram

*4.3.1.2   NuMicro® Nano103 LQFP 48-pin*
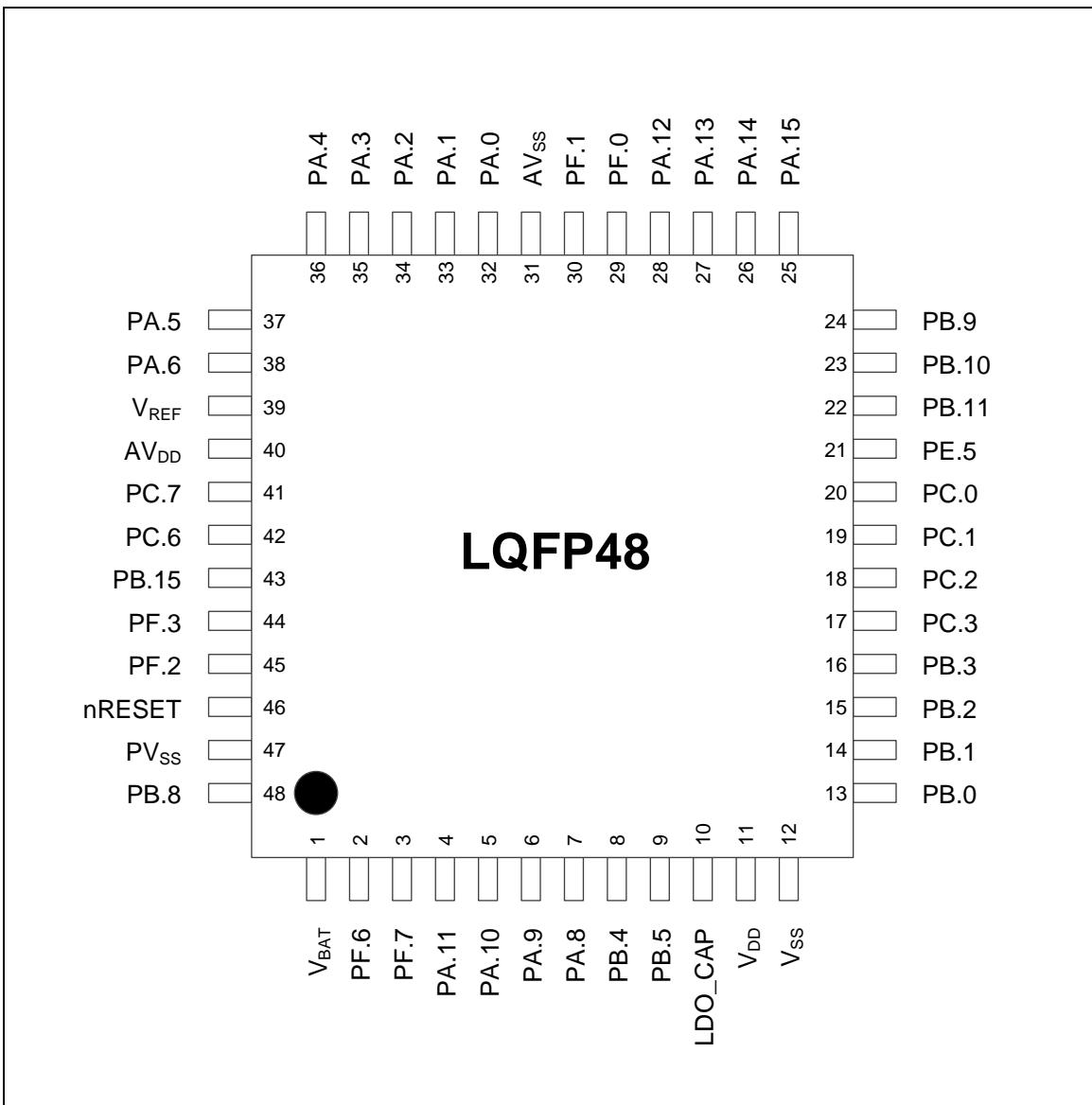


Figure 4.3-2 NuMicro® Nano103 LQFP 48-pin Diagram

*4.3.1.3    NuMicro® Nano103 QFN33-pin*
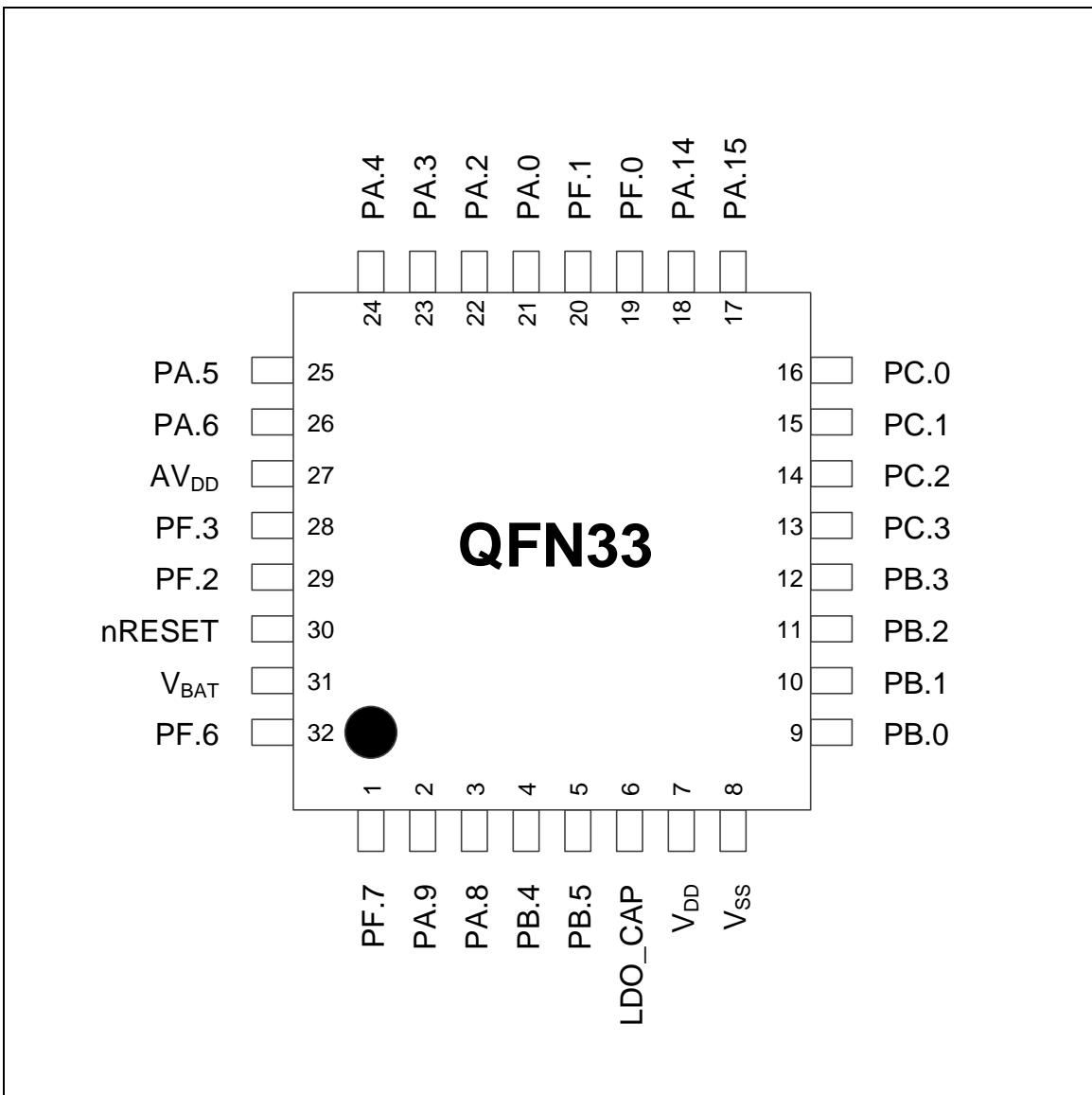


Figure 4.3-3 NuMicro® Nano103 QFN32-pin Diagram

## 4.4 Pin Description

### 4.4.1 NuMicro® Nano103 Pin Description

| Pin No. | | | Pin Name | Pin Type | MFP* | Description |
|---|---|---|---|---|---|---|
| 64-pin | 48-pin | 32-pin | | | | |
| 1 | - | - | PB.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | INT0 | I | MFP1 | External interrupt0 input pin. |
| | | | SPI2_MOSI1 | I/O | MFP3 | SPI2 2nd MOSI (Master Out, Slave In) pin. |
| | | | SPI2_SS1 | I/O | MFP4 | SPI2 2nd slave select pin. |
| 2 | - | - | PB.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI2_MISO1 | I/O | MFP3 | SPI2 2nd MISO (Master In, Slave Out) pin. |
| | | | SNOOPER | I | MFP7 | Snooper pin. |
| 3 | 1 | 31 | $V_{BAT}$ | P | MFP0 | Power supply for tamper pin (LQFP64: PB.13/LQFP48: PA.9/QFN32: PB.8) and RTC. |
| 4 | 2 | 32 | PF.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2C1_SDA | I/O | MFP1 | $I^2C1$ data input/output pin. |
| | | | X32_OUT | O | MFP7 | External 32.768 kHz crystal output pin(default). |
| 5 | 3 | 1 | PF.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2C1_SCL | I/O | MFP1 | $I^2C1$ clock pin. |
| | | | SC0_CD | I | MFP3 | SmartCard0 card detect pin. |
| | | | X32_IN | I | MFP7 | External 32.768 kHz crystal input pin(default). |
| - | - | 2 | PA.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2C0_SCL | I/O | MFP1 | $I^2C0$ clock pin. |
| | | | TM1_CNT | I | MFP2 | Timer1 event counter input. |
| | | | SC0_DAT | I/O | MFP3 | SmartCard0 data pin. |
| | | | SPI2_CLK | I/O | MFP4 | SPI2 serial clock pin. |
| | | | TM1_OUT | O | MFP5 | Timer1 toggle output. |
| | | | UART1_nRTS | O | MFP6 | UART1 Request to Send output pin. |
| | | | SNOOPER | I | MFP7 | Snooper pin. |
| 6 | 4 | - | PA.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2C1_SCL | I/O | MFP1 | $I^2C1$ clock pin. |
| | | | TM3_CNT | I | MFP2 | Timer3 event counter input. |
| | | | SC0_RST | O | MFP3 | SmartCard0 reset pin. |
| | | | SPI2_MOSI0 | I/O | MFP4 | SPI2 1st MOSI (Master Out, Slave In) pin. |
| | | | TM3_OUT | O | MFP5 | Timer3 toggle output. |

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| Pin No. | | | Pin Name | Pin Type | MFP* | Description |
|---|---|---|---|---|---|---|
| 64-pin | 48-pin | 32-pin | | | | |
| 7 | 5 | - | PA.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2C1_SDA | I/O | MFP1 | I$^2$C1 data input/output pin. |
| | | | TM2_CNT | I | MFP2 | Timer2 event counter input. |
| | | | SC0_PWR | O | MFP3 | SmartCard0 power pin. |
| | | | SPI2_MISO0 | I/O | MFP4 | SPI2 1$^{st}$ MISO (Master In, Slave Out) pin. |
| | | | TM2_OUT | O | MFP5 | Timer2 toggle output. |
| 8 | 6 | - | PA.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2C0_SCL | I/O | MFP1 | I$^2$C0 clock pin. |
| | | | TM1_CNT | I | MFP2 | Timer1 event counter input. |
| | | | SC0_DAT | I/O | MFP3 | SmartCard0 data pin. |
| | | | SPI2_CLK | I/O | MFP4 | SPI2 serial clock pin. |
| | | | TM1_OUT | O | MFP5 | Timer1 toggle output. |
| | | | UART1_nRTS | O | MFP6 | UART1 Request to Send output pin. |
| | | | SNOOPER | I | MFP7 | Snooper pin. |
| 9 | 7 | 3 | PA.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2C0_SDA | I/O | MFP1 | I$^2$C0 data input/output pin. |
| | | | TM0_CNT | I | MFP2 | Timer0 event counter input. |
| | | | SC0_CLK | O | MFP3 | SmartCard0 clock pin. |
| | | | SPI2_SS0 | I/O | MFP4 | SPI2 1$^{st}$ slave select pin. |
| | | | TM0_OUT | O | MFP5 | Timer0 toggle output. |
| | | | UART1_nCTS | I | MFP6 | UART1 Clear to Send input pin. |
| 10 | 8 | 4 | PB.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_RXD | I | MFP1 | Data receiver input pin for UART1. |
| | | | SC0_CD | I | MFP3 | SmartCard0 card detect pin. |
| | | | SPI2_SS0 | I/O | MFP4 | SPI2 1$^{st}$ slave select pin. |
| | | | RTC_HZ | O | MFP6 | RTC 1Hz output. |
| 11 | 9 | 5 | PB.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_TXD | O | MFP1 | Data transmitter output pin for UART1. |
| | | | SC0_RST | O | MFP3 | SmartCard0 reset pin. |
| | | | SPI2_CLK | I/O | MFP4 | SPI2 serial clock pin. |
| 12 | - | - | PB.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_RSTn | O | MFP1 | UART1 Request to Send output pin. |
| | | | SPI2_MISO0 | I/O | MFP4 | SPI2 1$^{st}$ MISO (Master In, Slave Out) pin. |

| Pin No. | | | Pin Name | Pin Type | MFP* | Description |
|---|---|---|---|---|---|---|
| 64-pin | 48-pin | 32-pin | | | | |
| 13 | - | - | PB.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_nCTS | I | MFP1 | UART1 Clear to Send input pin. |
| | | | SPI2_MOSI0 | I/O | MFP4 | SPI2 1st MOSI (Master Out, Slave In) pin. |
| 14 | 10 | 6 | LDO_CAP | AO | MFP0 | LDO output pin. |
| 15 | 11 | 7 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital function. |
| 16 | 12 | 8 | $V_{SS}$ | G | MFP0 | Ground pin for digital circuit. |
| 17 | 13 | 9 | PB.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART0_RXD | I | MFP1 | Data receiver input pin for UART0. |
| | | | SPI1_MOSI0 | I/O | MFP3 | SPI1 1st MOSI (Master Out, Slave In) pin. |
| 18 | 14 | 10 | PB.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART0_TXD | O | MFP1 | Data transmitter output pin for UART0. |
| | | | SPI1_MISO0 | I/O | MFP3 | SPI1 1st MISO (Master In, Slave Out) pin. |
| 19 | 15 | 11 | PB.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART0_nRTS | O | MFP1 | UART0 Request to Send output pin. |
| | | | SPI1_CLK | I/O | MFP3 | SPI1 serial clock pin. |
| | | | CLKO | O | MFP4 | Frequency Divider output pin. |
| 20 | 16 | 12 | PB.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART0_nCTS | I | MFP1 | UART0 Clear to Send input pin. |
| | | | SPI1_SS0 | I/O | MFP3 | SPI1 1st slave select pin. |
| | | | SC1_CD | I | MFP4 | SmartCard1 card detect pin. |
| 21 | - | - | PD.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI1_MOSI1 | I/O | MFP3 | SPI1 2nd MOSI (Master Out, Slave In) pin. |
| | | | SC1_RST | O | MFP4 | SmartCard1 reset pin. |
| 22 | - | - | PD.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI1_MISO1 | I/O | MFP3 | SPI1 2nd MISO (Master In, Slave Out) pin. |
| | | | SC1_PWR | O | MFP4 | SmartCard1 power pin. |
| 23 | - | - | PD.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI0_MOSI1 | I/O | MFP1 | SPI0 2nd MOSI (Master Out, Slave In) pin. |
| | | | SC1_DAT | I/O | MFP4 | SmartCard1 data pin. |
| 24 | - | - | PD.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI0_MISO1 | I/O | MFP1 | SPI0 2nd MISO (Master In, Slave Out) pin. |
| | | | SC1_CLK | O | MFP4 | SmartCard1 clock pin. |
| 25 | 17 | 13 | PC.3 | I/O | MFP0 | General purpose digital I/O pin. |

| Pin No. | | | Pin Name | Pin Type | MFP* | Description |
|---|---|---|---|---|---|---|
| 64-pin | 48-pin | 32-pin | | | | |
| | | | SPI0_MOSI0 | I/O | MFP1 | SPI0 1$^{st}$MOSI (Master Out, Slave In) pin. |
| | | | SC1_RST | O | MFP4 | SmartCard1 reset pin. |
| | | | PWM0_BRAKE0 | I | MFP5 | PWM0 Brake0 input pin . |
| 26 | 18 | 14 | PC.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI0_MISO0 | I/O | MFP1 | SPI0 1st MISO (Master In, Slave Out) pin. |
| | | | SC1_PWR | O | MFP4 | SmartCard1 power pin. |
| | | | PWM0_BRAKE1 | I | MFP5 | PWM0 Brake1 input pin. |
| 27 | 19 | 15 | PC.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI0_CLK | I/O | MFP1 | SPI0 serial clock pin. |
| | | | SC1_DAT | I/O | MFP4 | SmartCard1 data pin. |
| | | | PWM0_BRAKE0 | I | MFP5 | PWM0 Brake0 input pin. |
| 28 | 20 | 16 | PC.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI0_SS0 | I/O | MFP1 | SPI0 1$^{st}$ slave select pin. |
| | | | SC1_CLK | O | MFP4 | SmartCard1 clock pin. |
| | | | PWM0_BRAKE1 | I | MFP5 | PWM0 Brake1 input pin.. |
| 29 | 21 | - | PE.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | PWM0_CH5 | I/O | MFP1 | PWM0 channel5 output/capture input. |
| | | | RTC_HZ | O | MFP6 | RTC 1Hz output. |
| 30 | 22 | - | PB.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | PWM0_CH4 | I/O | MFP1 | PWM0 channel4 output/capture input. |
| | | | TM3_CNT | I | MFP2 | Timer3 event counter input. |
| | | | TM3_OUT | O | MFP4 | Timer3 toggle output. |
| | | | SPI0_MISO0 | I/O | MFP5 | SPI0 1$^{st}$ MISO (Master In, Slave Out) pin. |
| 31 | 23 | - | PB.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI0_MOSI0 | I/O | MFP1 | SPI0 1$^{st}$MOSI (Master Out, Slave In) pin. |
| | | | TM2_CNT | I | MFP2 | Timer2 event counter input. |
| | | | TM2_OUT | O | MFP4 | Timer2 toggle output. |
| | | | SPI0_SS1 | I/O | MFP5 | SPI0 2$^{nd}$ slave select pin. |
| 32 | 24 | - | PB.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI1_SS1 | I/O | MFP1 | SPI1 1$^{st}$ slave select pin. |
| | | | TM1_CNT | I | MFP2 | Timer1 event counter input. |
| | | | TM1_OUT | O | MFP4 | Timer1 toggle output. |
| | | | INT0 | I | MFP5 | External interrupt0 input pin. |

| Pin No. | | | Pin Name | Pin Type | MFP* | Description |
|---|---|---|---|---|---|---|
| 64-pin | 48-pin | 32-pin | | | | |
| 33 | - | - | PC.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI1_MOSI0 | I/O | MFP1 | SPI1 1st MOSI (Master Out, Slave In) pin. |
| | | | UART1_TXD | O | MFP5 | Data transmitter output pin for UART1. |
| 34 | - | - | PC.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI1_MISO0 | I/O | MFP1 | SPI1 1st MISO (Master In, Slave Out) pin. |
| | | | UART1_RXD | I | MFP5 | Data receiver input pin for UART1. |
| 35 | - | - | PC.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI1_CLK | I/O | MFP1 | SPI1 serial clock pin. |
| | | | I2C1_SCL | I/O | MFP5 | $I^2C1$ clock pin. |
| 36 | - | - | PC.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPI1_SS0 | I/O | MFP1 | SPI1 1st slave select pin. |
| | | | I2C1_SDA | I/O | MFP5 | $I^2C1$ data input/output pin. |
| 37 | 25 | 17 | PA.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | PWM0_CH3 | I/O | MFP1 | PWM0 channel3 output/capture input. |
| | | | I2C1_SCL | I/O | MFP2 | $I^2C1$ clock pin. |
| | | | TM3_EXT | I | MFP3 | Timer3 external capture input. |
| | | | SC0_PWR | O | MFP4 | SmartCard0 power pin. |
| | | | TM3_CNT | I | MFP5 | Timer3 event counter input. |
| | | | UART0_TXD | O | MFP6 | Data transmitter output pin for UART0. |
| | | | TM3_OUT | O | MFP7 | Timer3 toggle output. |
| 38 | 26 | 18 | PA.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | PWM0_CH2 | I/O | MFP1 | PWM0 channel2 output/capture input. |
| | | | I2C1_SDA | I/O | MFP2 | $I^2C1$ data input/output pin. |
| | | | TM2_EXT | I | MFP3 | Timer2 external capture input. |
| | | | TM2_CNT | I | MFP5 | Timer2 event counter input. |
| | | | UART0_RXD | I | MFP6 | Data receiver input pin for UART0. |
| | | | TM2_OUT | O | MFP7 | Timer2 toggle output. |
| 39 | 27 | - | PA.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | PWM0_CH1 | I/O | MFP1 | PWM0 channel1 output/capture input. |
| | | | TM1_EXT | I | MFP3 | Timer1 external capture input. |
| | | | I2C0_SCL | I/O | MFP5 | $I^2C0$ clock pin. |
| 40 | 28 | - | PA.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | PWM0_CH0 | I/O | MFP1 | PWM0 channel0 output/capture input. |

| Pin No. | | | Pin Name | Pin Type | MFP* | Description |
|---|---|---|---|---|---|---|
| 64-pin | 48-pin | 32-pin | | | | |
| | | | TM0_EXT | I | MFP3 | Timer0 external capture input. |
| | | | I2C0_SDA | I/O | MFP5 | $I^2$C0 data input/output pin. |
| 41 | 29 | 19 | PF.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | INT0 | I | MFP5 | External interrupt0 input pin. |
| | | | ICE_DAT | I/O | MFP7 | Serial wired debugger data pin |
| 42 | 30 | 20 | PF.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | CLKO | O | MFP4 | Frequency Divider output pin. |
| | | | INT1 | I | MFP5 | External interrupt1 input pin. |
| | | | ICE_CLK | I | MFP7 | Serial wired debugger clock pin. |
| 43 | 31 | - | AV$_{SS}$ | G | MFP0 | Ground pin for analog circuit. |
| 44 | 32 | 21 | PA.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | ADC_CH0 | AI | MFP1 | ADC analog input0. |
| | | | ACMP0_P | AI | MFP2 | Comparator0 P-end input. |
| | | | TM2_EXT | I | MFP3 | Timer2 external capture input. |
| | | | PWM0_CH2 | I/O | MFP5 | PWM0 channel2 output/capture input. |
| | | | SPI3_MOSI1 | I/O | MFP6 | SPI3 2$^{nd}$MOSI (Master Out, Slave In) pin. |
| 45 | 33 | - | PA.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | ADC_CH1 | AI | MFP1 | ADC analog input1. |
| | | | ACMP0_N | AI | MFP2 | Comparator0 N-end input. |
| | | | SPI3_MISO1 | I/O | MFP6 | SPI3 2$^{nd}$ MISO (Master In, Slave Out) pin. |
| 46 | 34 | 22 | PA.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | ADC_CH2 | AI | MFP1 | ADC analog input2. |
| | | | UART1_RXD | I | MFP5 | Data receiver input pin for UART1. |
| 47 | 35 | 23 | PA.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | ADC_CH3 | AI | MFP1 | ADC analog input3. |
| | | | UART1_TXD | O | MFP5 | Data transmitter output pin for UART1. |
| | | | SPI3_MOSI0 | I/O | MFP6 | SPI3 1$^{st}$ MOSI (Master Out, Slave In) pin. |
| 48 | 36 | 24 | PA.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | ADC_CH4 | AI | MFP1 | ADC analog input4. |
| | | | I2C0_SDA | I/O | MFP5 | $I^2$C0 data input/output pin. |
| | | | SPI3_MISO0 | I/O | MFP6 | SPI3 1$^{st}$ MISO (Master In, Slave Out) pin. |
| 49 | 37 | 25 | PA.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | ADC_CH5 | AI | MFP1 | ADC analog input5. |

| Pin No. | | | Pin Name | Pin Type | MFP* | Description |
|---|---|---|---|---|---|---|
| 64-pin | 48-pin | 32-pin | | | | |
| | | | I2C0_SCL | I/O | MFP5 | I$^2$C0 clock pin. |
| | | | SPI3_SCLK | I/O | MFP6 | SPI3 serial clock pin. |
| 50 | 38 | 26 | PA.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | ADC_CH6 | AI | MFP1 | ADC analog input6. |
| | | | ACMP0_O | O | MFP2 | Comparator0 output. |
| | | | TM3_EXT | I | MFP3 | Timer3 external capture input. |
| | | | TM3_CNT | I | MFP4 | Timer3 event counter input. |
| | | | PWM0_CH3 | I/O | MFP5 | PWM0 channel3 output/capture input. |
| | | | SPI3_SS0 | I/O | MFP6 | SPI3 1$^{st}$ slave select pin. |
| | | | TM3_OUT | O | MFP7 | Timer3 toggle output. |
| 51 | 39 | - | VREF | I | MFP0 | Voltage reference input for ADC. |
| 52 | 40 | 27 | AV$_{DD}$ | AP | MFP0 | Power supply for internal analog circuit. |
| 53 | 41 | - | PC.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_TXD | O | MFP1 | Data transmitter output pin for UART1. |
| | | | ADC_CH7 | AI | MFP2 | ADC analog input7. |
| | | | TM1_EXT | I | MFP3 | Timer1 external capture input. |
| | | | PWM0_CH1 | I/O | MFP5 | PWM0 channel1 output/capture input. |
| 54 | 42 | - | PC.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_RXD | I | MFP1 | Data receiver input pin for UART1. |
| | | | TM0_EXT | I | MFP3 | Timer0 external capture input. |
| | | | SC1_CD | I | MFP4 | SmartCard1 card detect pin. |
| | | | PWM0_CH0 | I/O | MFP5 | PWM0 channel0 output/capture input. |
| 55 | - | - | PC.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_nRTS | O | MFP1 | UART1 Request to Send output pin. |
| | | | TM0_EXT | I | MFP3 | Timer0 external capture input. |
| 56 | - | - | PC.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_nCTS | I | MFP1 | UART1 Clear to Send input pin. |
| 57 | 43 | - | PB.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | INT1 | I | MFP1 | External interrupt1 input pin. |
| | | | SNOOPER | I | MFP3 | Snooper pin. |
| | | | SC1_CD | I | MFP4 | SmartCard1 card detect pin. |
| 58 | 44 | 28 | PF.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | XT1_IN | I | MFP7 | External 4~24 MHz (high speed) crystal input pin. |

| Pin No. | | | Pin Name | Pin Type | MFP* | Description |
|---------|--------|--------|----------|----------|------|-------------|
| 64-pin | 48-pin | 32-pin | | | | |
| 59 | 45 | 29 | PF.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | XT1_OUT | O | MFP7 | External 4~24 MHz (high speed) crystal output pin. |
| 60 | 46 | 30 | nRESET | I | MFP0 | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. |
| 61 | - | - | $V_{SS}$ | G | MFP0 | Ground pin for digital circuit. |
| 62 | - | - | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital function. |
| 63 | 47 | - | $V_{SS}$ | G | MFP0 | Ground pin for digital circuit. |
| 64 | 48 | - | PB.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | STADC | I | MFP1 | ADC external trigger input. |
| | | | TM0_CNT | I | MFP2 | Timer0 event counter input. |
| | | | INT0 | I | MFP3 | External interrupt0 input pin. |
| | | | TM0_OUT | O | MFP4 | Timer0 toggle output. |
| | | | SNOOPER | I | MFP7 | Snooper pin. |

**Note:** Pin Type: I = Digital Input, O=Digital Output; AI = Analog Input; AO = Analog Output; P = Power Pin; AP = Analog Power.

# 5 BLOCK DIAGRAM

## 5.1 Nano103 Block Diagram
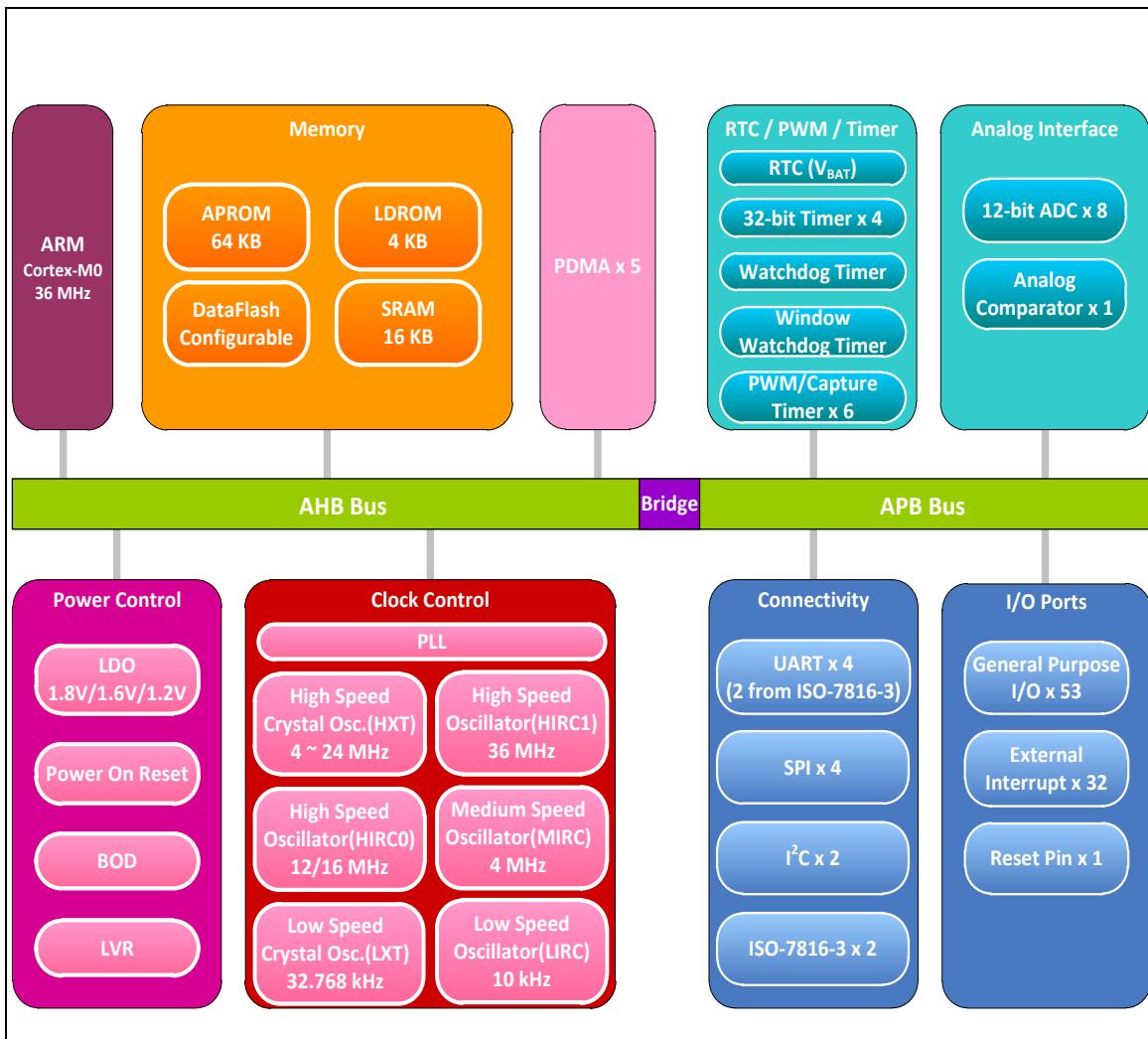


Figure 5.1-1 NuMicro® Nano103 Block Diagram

# 6 FUNCTIONAL DESCRIPTION

## 6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes –Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Figure 6.1-1shows the functional controller of processor.
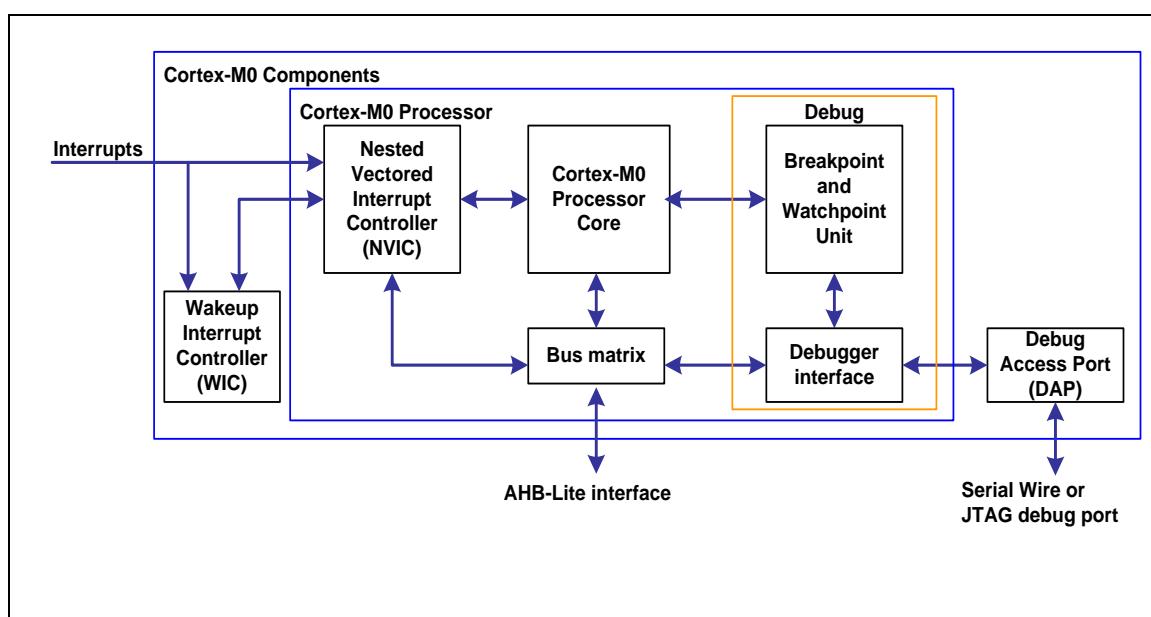


Figure 6.1-1 Functional Block Diagram

The implemented device provides:

● A low gate count processor:

  ■ ARMv6-M Thumb® instruction set
  ■ Thumb-2 technology
  ■ ARMv6-M compliant 24-bit SysTick timer
  ■ A 32-bit hardware multiplier
  ■ System interface supported with little-endian data accesses
  ■ Ability to have deterministic, fixed-latency, interrupt handling
  ■ Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  ■ C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  ■ Low Power Sleep mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature

● NVIC:

  ■ 32 external interrupt inputs, each with four levels of priority

- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode

● Debug support:

- Four hardware breakpoints
- Two watchpoints
- Program Counter Sampling Register (PCSR) for non-intrusive code profiling
- Single step and vector catch capabilities

● Bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
- Single 32-bit slave port that supports the DAP (Debug Access Port)

## 6.2 System Manager

### 6.2.1 Overview

The system manager provides the functions of power modes, wake-up sources, power architecture, reset sources, scalable LDO, system memory map, product ID and multi-function pin control.

### 6.2.2 Features

- Power modes and wake-up sources
- System power architecture
- Reset sources
- Scalable LDO
- HIRC0, HIRC1, and MIRC Auto-trim
- System memory map
- System manager Control registers map
- System timer (SysTick)
- System control register
- Nested vectored interrupt controller (NVIC)

## 6.3 Clock Controller

### 6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[6]) and Cortex®-M0 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT), 12~16 MHz internal high speed RC oscillator (HIRC0), 36 MHz internal high speed RC oscillator (HIRC1), and 4 MHz internal medium speed RC oscillator (MIRC) to reduce the overall system power consumption. The following figure shows the clock generator and the overview of the clock source control.

The clock controller consists of 7 sources as listed below:

- 32768 Hz external low speedcrystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- 12~16 MHz internal high speed RC oscillator (HIRC0)
- 36 MHz internal high speed RC oscillator (HIRC1)
- 4 MHz internal medium speed RC oscillator (MIRC)
- One programmable PLL FOUT (PLL source can be selected from HXT, HIRC0,HIRC1 or MIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

### 6.3.2 Features

- Generates clocks for system clocks and all peripheral module clocks.
- Each peripheral module clock can be turned on/off.
- In Power-down mode, the clock controller turns off the external high speed crystal (HXT) and internal high speed RC oscillator (HIRC0,HIRC1 and MIRC) to reduce the overall system power consumption.

## 6.4 Flash Memory Controller (FMC)

### 6.4.1    Overview

The Nano103 series is equipped with 32/64 Kbytes on-chip embedded flash for application and Data Flash to store some application dependent data. A User Configuration block provides for system initiation. A 4K bytes loader ROM (LDROM) is used for In-System-Programming (ISP) function.  This chip also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded flash updated.

### 6.4.2    Features

- Supports 32/64 Kbytesapplication ROM (APROM).

- Supports 4 Kbytesloader ROM (LDROM).

- Supports Data Flash with configurable memory size.

- Supports 12 bytes User Configuration block to control system initiation.

- Supports 512 bytes page erase for all embedded flash.

- Supports fast flash programming verification function.

- Supports CRC-32 checksum calculation function.

- Supports Flash All-One verification function.

- Supports In-System-Programming (ISP) /In-Application-Programming (IAP)to update embedded flash memory.

- Supports cache memory to improve flash access performance and reduce power consumption.

## 6.5 General Purpose I/O Controller

### 6.5.1    Overview

The Nano103 series hasup to 53 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 53 pins are arranged in 6 ports named as PA, PB, PC, PD, PE and PF.The PA, PB, PC, PD and PE have 16 pins on port, and the PF has 8 pins on port. Each of the 53 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each I/O pin can be configured by software individually as Input, Push-pull output, and Open-drain output. Each I/O pin has a very weak individual pull-up resistor which is about 110 k$\Omega$~40 k$\Omega$ and V$_{DD}$ is from 2.2 V to 3.6 V.

### 6.5.2    Features

- Three I/O modes:
  - Schmitt triggerInput-only with high impendence
  - Push-Pull Output mode
  - Open-Drain Output mode
- I/O pin can be configured as interrupt source with edge/level setting
- Enabling the pin interrupt function will also enable the wake-up function

## 6.6 PDMA Controller (PDMA)

### 6.6.1 Overview

The peripheral direct memory access (PDMA) controllerin the Nano103 series contains a four-channel DMA controller and a cyclic redundancy check (CRC) generator.

The PDMA controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 4 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

The PDMA controller also contains a cyclic redundancy check (CRC) generator that can perform CRC calculation with programmable polynomial settings. The CRC engine supports CPU mode and DMA transfer mode.

### 6.6.2 Features

- Supports 4 independently configurable channels and 1 CRC channel
- Supports hardware round robin priority scheme. PDMA channel 1 has the highest priority and channel 4 has the lowest priority
- PDMA
  - Supports transfer data width of 8, 16, or 32 bits
  - Supports software and SPI, UART, TIMER and ADC request
  - Supports source and destination address increment size can be byte, half-word, word, no increment or wrap around
  - Supports periodic transfer count interrupt
  - Supports time-out function for each channel
- Cyclic Redundancy Check (CRC)
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
    - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
    - CRC-8:$X^8 + X^2 + X + 1$
    - CRC-16: $X^{16} + X^{15} + X^2 + 1$
    - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
  - Programmable seed value
  - Supports programmable order reverse setting for input data and CRC checksum
  - Supports programmable 1's complement setting for input data and CRC checksum
  - Supports CPU mode or DMA transfer mode
  - Supports transfer data width of 8, 16, or 32 bits in CRC CPU mode
    - 8-bit write mode: 1-AHB clock cycle operation
    - 16-bit write mode: 2-AHB clock cycle operation
    - 32-bit write mode: 4-AHB clock cycle operation

◆ Supports transfer data width of 8 bits in CRC DMA mode

## 6.7 Timer Controller

### 6.7.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

### 6.7.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter

- Independent Clock Source for each Timer

- Provides one-shot, periodic, toggle-output and continuous counting operation modes

- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])

- Supports event counting function to count input event from pin TMx_CNT (x = 0~3)

- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])

- Supports event capture from external pin TMx_EXT (x = 0~3) for interval measurement

- Supports event capture from external pin TMx_EXT (x = 0~3) to reset 24-bit up counter

- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

- Supports time-out interrupt or capture interrupt to trigger ADC, PDMA and PWM.

- Supports Inter-Timer trigger that Timer 0 can trigger Timer 1 and Timer 2 can trigger Timer 3

## 6.8 PWM Generator and Capture Timer (PWM)

### 6.8.1 Overview

The Nano103 provides one PWM generator — PWM0. The PWM0 supports 6 channels for PWM0 output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM0 counter with 16-bit comparator. The PWM0 counter supports up, down and up-down counter types and uses a comparator compared with counter to generate events. These events are used to generate PWM0 pulse, interrupt and trigger signal for ADC to start conversion.

The PWM0 generator supports two standard PWM0 output modes: Independent mode and Complementary mode, which have different architecture. In Complementary mode, there are two comparators that generate various PWM0 pulse with 12-bit dead-time generator. The PWM0 output control unit supports polarity output, independent pin mask, tri-state output enable and brake functions.

The PWM0 generator also supports input capture function. It supports latch PWM0 counter value to a corresponding register when input channel has a rising transition, falling transition or both transitions.

### 6.8.2 Features

*6.8.2.1 PWM0 function features*

- Supports one PWM0 module to provides 6 output channels
- Supports independent mode for PWM0 output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM0 output channel
  - Dead-time insertion with 12-bit resolution
  - Two compared values during one period
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution PWM0 counter, each module provides 3 PWM0 counters
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each PWM0 pin
- Supports brake function
  - Brake source from pin and system safety events (Brown-out detection and CPU lockup)
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM0 counter match zero, period value or compared value
  - Brake condition happened
- Supports trigger ADCon the following events:
  - PWM0 counter match zero, period value or compared value

### 6.8.2.2 Capture Function Features

- Supportsup to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

## 6.9 Watchdog Timer Controller

### 6.9.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset after system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up CPU from Power-down mode. The watchdog timer includes an 18-bit free running up counter with programmable time-out intervals.

### 6.9.2 Features

- 18-bit free running up counter for Watchdog timer time-out interval.

- Selectable time-out interval ($2^4$ ~ $2^{18}$) and the time-out interval is 1.6 ms ~ 26.214 s (if WDT_CLK = 10 kHz).

- System kept in reset state for a period of (1 / WDT_CLK) * 63.

- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period.

- Supports to force WDT enabled after chip powered on or reset by setting CWDT_EN[2:0] in Config0 register.

- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT.

## 6.10 Window Watchdog Timer Controller

### 6.10.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition. The WWDT down counter value will stop to update when chip is in Idle or Power-down mode.

### 6.10.2 Features

- 6-bit down counter (WWDT_CNT) and 6-bit compare value (WINCMP) to make the WWDT time-out window period flexible

- Supports 4-bit value (PERIODSEL) to programmable maximum 11-bit prescale counter period of WWDT counter

## 6.11 Real Time Clock (RTC)

### 6.11.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick andalarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

The RTC controller also offers 80 bytes spare registers to store user's important information. The spare registers content is cleared when specified event on tamper pin is detected.

### 6.11.2 Features

- Supportsreal time counterin RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year,month, day) for RTC time and calendar check

- Supportsalarm time (hour, minute, second) and calendar (year,month, day) settings in RTC_TALM and RTC_CALM

- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK

- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register

- Supports Leap Year indication in RTC_LEAPYEAR register

- Supports Day of the Week counterin RTC_WEEKDAY register

- Frequency of RTC clock source compensateby RTC_FREQADJ register

- All time and calendar message expressed in BCD format

- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second

- Supports RTC Time Tick and Alarm Match interrupt

- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated

- Supports 20 bytes spare registers and a snoop pin detection to clear the content of these spare registers

## 6.12 UART Controller

### 6.12.1 Overview

The UART Controller provides up to two channels of Universal Asynchronous Receiver/Transmitter (UART). The UART Controller performs Normal Speed UART and supports flow control function. In addtion, the UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN Master/Slave, RS-485 and auto-baud rate measuring function.

### 6.12.2 Features

- Full duplex asynchronous communications.

- Separate receiving and transmitting 16/16 bytes entry FIFO for data payloads.

- Supports hardware auto-flow control

- Supports programmable receiver buffer trigger level.

- Supports programmable baud rate generator for each channel individually.

- Supports nCTS, incoming RX data, RS-485 AAD mode address matched or received FIFO is equal to the RFITL to wake-up function.

- Supports 9-bit receiver buffer time-out detection function.

- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (*UART_TOUT* [15:8])

- Supports Auto-Baud Rate measurement and baud rate compensation

- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function

- Fully programmable serial-interface characteristics

  ■ Programmable number of data bit, 5-, 6-, 7-, 8- bit character

  ■ Programmable parity bit, even, odd, no parity or stick parity bit generation and detection

  ■ Programmable stop bit, 1, 1.5, or 2 stop bit generation

- Supports IrDA SIR function mode

  ■ Supports for 3/16 bit duration for normal mode

- Supports LIN function mode

  ■ Supports LIN master/slave mode

  ■ Supports programmable break generation function for transmitter

  ■ Supports break detection function for receiver

- Supports RS-485 function mode

  ■ Supports RS-485 9-bit mode

  ■ Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction

- All UART Controller can be served by the PDMA.

## 6.13    Smart Card Host Interface (SC)

### 6.13.1    Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also can be set as UART mode to communicate with other device.

### 6.13.2    Features

- ISO-7816-3 T = 0, T = 1 compliant

- EMV2000 compliant

- Up to two ISO-7816-3 ports

- Separates receive/transmit 4 byte entry FIFO for data payloads

- Programmable transmission clock frequency

- Programmable receiver buffer trigger level

- Programmable guard time selection (11 ETU ~ 267 ETU)

- One 24-bit timer and two 8-bit timers for Answer to Request (ATR) and waiting times processing

- Supports auto inverse convention function

- Supports transmitter and receiver error retry and error number limitation function

- Supports hardware activation sequence process ,and the time between PWR on and CLK start is configurable

- Supports hardware warm reset sequence process

- Supports hardware deactivation sequence process

- Supports hardware auto deactivation sequence when detected the card removal

- Provides card insert/removal status

- Supports UART mode

    - Full duplex, asynchronous communications
    - Separates receiving / transmitting 4 bytes entry FIFO for data payloads
    - Supports programmable baud rate generator for each channel
    - Supports programmable receiver buffer trigger level
    - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting SC_EGTR register
    - Programmable even, odd or no parity bit generation and detection
    - Programmable stop bit, 1 or 2 stop bit generation

## 6.14 I$^2$C Serial Interface Controller (I$^2$C)

### 6.14.1 Overview

I$^2$C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I$^2$C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I$^2$C controllers which support Power-down wake-up function.

### 6.14.2 Features

The I$^2$C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I$^2$C bus include:

- Supports up to two I$^2$C ports

- Master/Slave mode

- Bidirectional data transfer between masters and slaves

- Multi-master bus (no central master)

- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus

- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus

- Built-in 14-bit time-out counter requesting the I$^2$C interrupt if the I$^2$C bus hangs up and timer-out counter overflows.

- Programmable clocks allow for versatile rate control

- Supports 7-bit addressing mode

- Supports multiple address recognition ( two slave address with mask option)

- Supports Power-down wake-up function

- Supports two-level buffer

- Supports data transmit or receive directly mode.

## 6.15 SPI

### 6.15.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. It is used to perform a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI controller can be configured as a master or a slave device.

The SPI controller supports wake-up function. When this chip stays in Power-down mode, it can be woken up by off-chip device.

The SPI controller supports 2-bit transfer mode to connect 2 off-chip slave devices and then perform full-duplex 2-bit data transfer. It also supports PDMA function to access the data buffer.

### 6.15.2 Features

- Up to four sets of SPI controllers
- Supports Master or Slave mode operation
- Supports 1 bit and 2 bit transfer mode
- Supports Dual I/O transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Supports MSB first or LSB first transfer sequence
- Two slave select lines supported in Master mode
- Configurable byte or word suspend mode
- Supports byte re-ordering function
- Provide separate 8-level depth transmit and receive FIFO buffer
- Supports wake-up function
- Supports PDMA transfer
- Supports 3-wires, no slave select signal, bi-direction interface

## 6.16 Analog to Digital Converter (ADC)

### 6.16.1 Overview

The Nano103 series contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 8 external input channels and 6 internal channels. The A/D converter supports three operation modes: Single, Single-cycle Scan and Continuous Scan mode, and can be started by software, external STADC(PB.8) pin, timer event trigger and PWM trigger.

Note that the I/O pins used as ADC analog input pins must configure the Pin Function (SYS_GPA_MFPL/SYS_GPC_MFPL) to ADC input and off digital input path disable control (Px_DINOFF) should be turned on before ADC function is enabled.

### 6.16.2 Features

- Analog input voltage range: $0 \sim V_{REF}$ (Max to $AV_{DD}$).

- Selectable 12-bit, 10-bit, 8-bit and 6-bit resolution.

- Supports sampling time settings for channel 0~7 individually and channel 12~17 share the same one sampling time setting.

- Supports two power saving modes:

  - Power-down mode.

  - Standby mode.

- Up to 8 external analog input channels (channel0 ~ channel7), and 6 internal channels (channel12 - channel17) converting six voltage sources (internal band-gap voltage, internal reference voltage, internal temperature sensor output, battery voltage, $AV_{DD}$, and $AV_{SS}$).

- Maximum ADC clock frequency is 36 MHz and each conversion needs 19 clocks and sampling time depending on the input resistance (Rin).

- Three operating modes:

  - Single mode: A/D conversion is performed one time on a specified channel.

  - Single-cycle Scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel.

  - Continuous Scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion.

- An A/D conversion can be started by:

  - Software write 1 to SWTRG (ADC_CTL[11]) bit.

  - External pin STADC.

  - PWM trigger.

  - Selects one of four timer events to trigger ADC and transfer A/D results by PDMA.

- Each conversion result is held in data registers for each channel with valid and overrun indicators.

- Conversion results can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.

- Supports calibration and load calibration words capability.

## 6.17 Analog Comparator Controller (ACMP0)

### 6.17.1 Overview

The Nano103 series contains one comparator. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. The comparator can be configured to generate an interrupt when the comparator output value changes.

### 6.17.2 Features

- Analog input voltage range: 0 ~ $AV_{DD}$(voltage of $AV_{DD}$ pin)
- Supports hysteresis function
- Supports wake-up function
- Selectableinput sources of negative input
- Comparator ACMP supports
    - 1 positive source
        - PA.0(ACMP0_P)
    - 4 negative sources
        - PA.1(ACMP0_N)
        - Comparator Reference Voltage (CRV)
        - Int_$V_{REF}$
        - AGND

## 7   APPLICATION CIRCUIT



**Note**: For the SPI device, the Nano103 chip supply voltage must be equal to SPI device working voltage. For example, when the SPI Flash working voltage is 3.3 V, the Nano103 chip supply voltage must also be 3.3V.
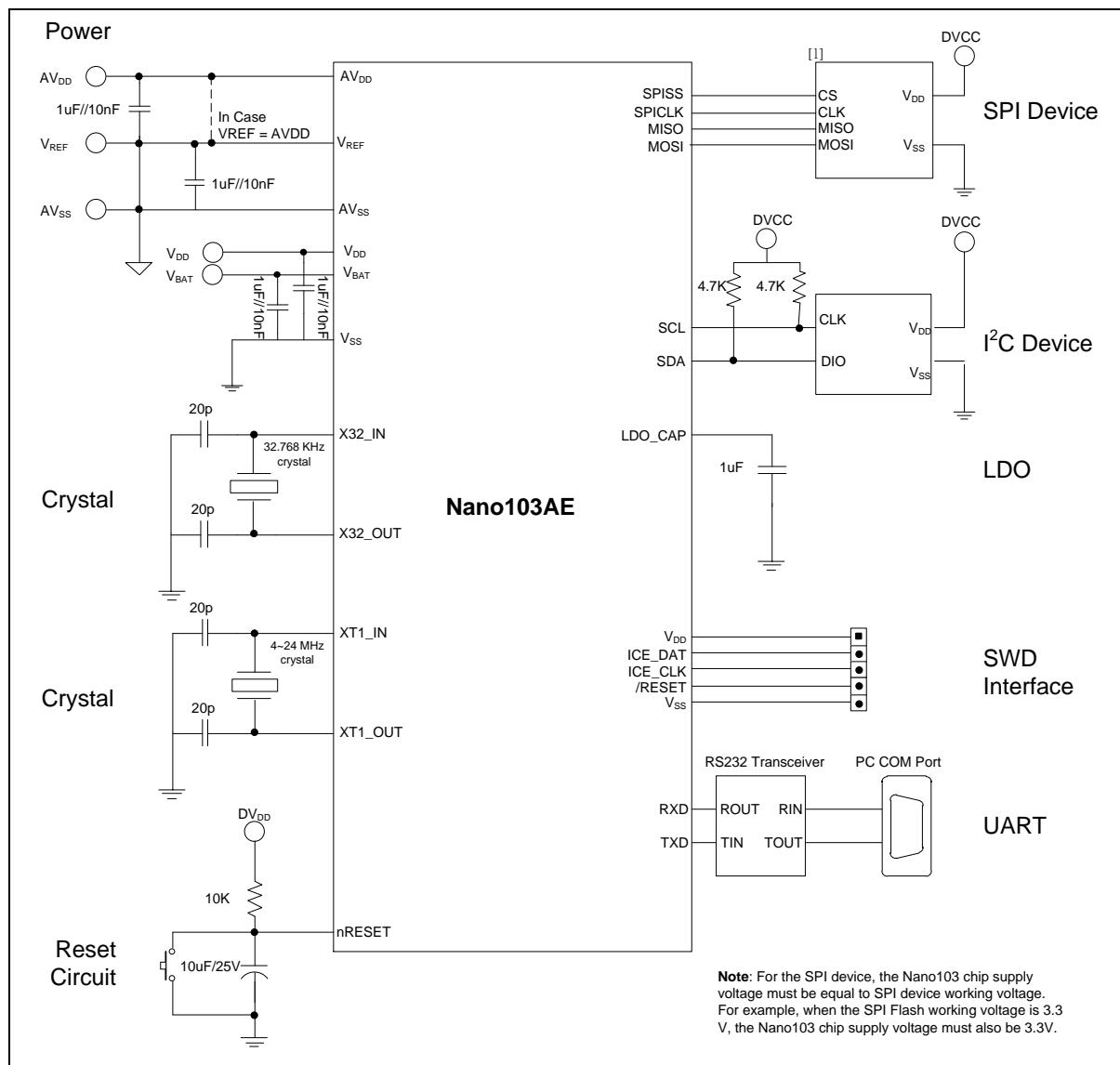
# 8 POWER COMSUMPTION

| Part No | Test Condition | VDD | CPU clock | Current |
|---------|----------------|-----|-----------|---------|
| Nano103 series | Operating Mode:<br>CPU run while(1) in FLASH ROM<br>Clock = 36MHz (from PLL and its clock source is 12 MHz Crystal Oscillator)<br>Disable all peripheral<br>Set LDO output = 1.8V | 3.6V | 36 MHz | 6.7mA<br>186uA/MHz |
| | Idle Mode:<br>CPU stop<br>Clock = 36MHz (from PLL and its clock source is 12 MHz Crystal Oscillator)<br>Disable all peripheral<br>Set LDO output = 1.8V | 3.6V | 36 MHz | 2.2mA<br>61uA/MHz |
| | Operating Mode:<br>CPU run while(1) in FLASH ROM<br>Clock = 36MHz Internal RC Oscillator<br>Disable all peripheral<br>Set LDO output = 1.8V | 3.6V | 36 MHz | 6.7mA<br>186uA/MHz |
| | Idle Mode:<br>CPU stop<br>Clock = 36MHz Internal RC Oscillator<br>Disable all peripheral<br>Set LDO output = 1.8V | 3.6V | 36 MHz | 1.9mA<br>53uA/MHz |
| | Operating Mode:<br>CPU run while(1) in FLASH ROM<br>Clock = 16MHz Crystal Oscillator<br>Disable all peripheral<br>Set LDO output = 1.6V | 3.6V | 16 MHz | 2.9mA<br>181uA/MHz |
| | Idle Mode:<br>CPU stop<br>Clock = 16MHz Crystal Oscillator<br>Disable all peripheral<br>Set LDO output = 1.6V | 3.6V | 16 MHz | 1.2mA<br>75uA/MHz |
| | Operating Mode:<br>CPU run while(1) in FLASH ROM<br>Clock = 36MHz Internal RC Oscillator<br>Disable all peripheral<br>Set LDO output = 1.6V | 3.6V | 16 MHz | 2.8mA<br>175uA/MHz |
| | Idle Mode:<br>CPU stop<br>Clock = 36MHz Internal RC Oscillator<br>Disable all peripheral<br>Set LDO output = 1.6V | 3.6V | 16 MHz | 1.1mA<br>69uA/MHz |
| | Operating Mode:<br>CPU run while(1) in FLASH ROM<br>Clock = 12MHz Crystal Oscillator<br>Disable all peripheral<br>Set LDO output = 1.6V | 3.6V | 12 MHz | 2.2mA<br>183uA/MHz |
| | Idle Mode:<br>CPU stop<br>Clock = 12MHz Crystal Oscillator | 3.6V | 12 MHz | 900uA<br>75uA/MHz |

| | | | |
|---|---|---|---|
| Disable all peripheral<br>Set LDO output = 1.6V | | | |
| Operating Mode:<br>CPU run while(1) in FLASH ROM<br>Clock = 12MHz Internal RC Oscillator<br>Disable all peripheral<br>Set LDO output = 1.6V | 3.6V | 12 MHz | 2.2mA<br>183uA/MHz |
| Idle Mode:<br>CPU stop<br>Clock = 12MHz Internal RC Oscillator<br>Disable all peripheral<br>Set LDO output = 1.6V | 3.6V | 12 MHz | 900uA<br>75uA/MHz |
| Operating Mode:<br>CPU run while(1) in FLASH ROM<br>Clock = 4MHz Crystal Oscillator<br>Disable all peripheral<br>Set LDO output = 1.2V | 3.6V | 4 MHz | 600uA<br>150uA/MHz |
| Idle Mode:<br>CPU stop<br>Clock = 4MHz Crystal Oscillator<br>Disable all peripheral<br>Set LDO output = 1.2V | 3.6V | 4 MHz | 500uA<br>125uA/MHz |
| Operating Mode:<br>CPU run while(1) in FLASH ROM<br>Clock = 4MHz Internal RC Oscillator<br>Disable all peripheral<br>Set LDO output = 1.2V | 3.6V | 4 MHz | 900uA<br>225uA/MHz |
| Idle Mode:<br>CPU stop<br>Clock = 4MHz Internal RC Oscillator<br>Disable all peripheral<br>Set LDO output = 1.2V | 3.6V | 4 MHz | 500uA<br>125uA/MHz |
| RTC Mode: (RAM retention)<br>(Main power off and only $V_{BAT}$ and RTC on)<br>CPU stop<br>Clock = 32.768KHz Crystal Oscillator<br>Disable all peripheral except RTC circuit | 3.6V | Stop | 1uA |
| RTC Mode: (RAM retention)<br>(Power down with LXT enable)<br>CPU stop<br>Clock = 32.768KHz Crystal Oscillator<br>Disable all peripheral except RTC circuit<br>Set LDO output = 1.2V | 3.6V | Stop | 2.1uA |
| Power Down Mode: (RAM retention)<br>CPU and all clocks stop<br>Set LDO output = 1.2V | 3.6V | Stop | 1.6uA |

## 9 ELECTRICAL CHARACTERISTICS

### 9.1 Absolute Maximum Ratings

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| DC Power Supply | $V_{DD}$-$V_{SS}$ | -0.3 | +3.6 | V |
| Battery Power Supply | $V_{BAT}$-$V_{SS}$ | -0.3 | +3.6 | V |
| Input Voltage on 5V Tolerance Pin | $V_{IN}$ | $V_{SS}$ -0.3 | 5.5 | V |
| Input Voltage on Any Other Pin without 5V Tolerance Pin | $VI_N$ | $V_{SS}$ -0.3 | $V_{DD}$ +0.3 | V |
| Oscillator Frequency | 1/t$_{CLCL}$ | 4 | 24 | MHz |
| Operating Temperature | $T_A$ | -40 | +105 | °C |
| Storage Temperature | $T_{ST}$ | -55 | +150 | °C |
| Maximum Current into $V_{DD}$ | | - | 150 | mA |
| Maximum Current out of $V_{SS}$ | | - | 150 | mA |
| Maximum Current sunk by a I/O Pin | | - | 25 | mA |
| Maximum Current Sourced by a I/O Pin | | - | 25 | mA |
| Maximum Current Sunk by Total I/O Pins | | - | 100 | mA |
| Maximum Current Sourced by Total I/O Pins | | - | 100 | mA |

**Note:** Output voltage for ADC/ACMP/HXT/LXT/PA.8/PB.4/PB.5 shared pins cannot be higher than $V_{DD}$ because these pins are without 5V tolerance.

## 9.2 Nano103 DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, FOSC = 36 MHz unless otherwise specified.)

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| Operation Voltage | $V_{DD}$ | 2.2 | - | 3.6 | V | $V_{DD}$ = 2.2V up to 36 MHz | | | | |
| Power Ground | $V_{SS}$ $AV_{SS}$ | -0.3 | - | - | V | | | | | |
| LDO Output Voltage | $V_{LDO}$ | 1.62 | 1.8 | 1.98 | V | MCU operating in Run, Idle or Power-down mode | | | | |
| | | 1.44 | 1.6 | 1.76 | V | Set LDO_LEVEL(LDO_CTL[3:2]) = 0x1 | | | | |
| | | 1.08 | 1.2 | 1.32 | V | Set LDO_LEVEL(LDO_CTL[3:2]) = 0x0 | | | | |
| | $C_{LDO}$ | 1 | - | 1 | uF | Connect to LDO_CAP pin | | | | |
| Analog Operating Voltage | $AV_{DD}$ | - | $V_{DD}$ | - | V | | | | | |
| Battery Operating Voltage | $V_{BAT}$ | - | $V_{DD}$ | - | V | | | | | |
| Operating Current Normal Run Mode HCLK =36 MHz while(1){}executed from flash $V_{LDO}$=1.8 V | $I_{DD1}$ | - | 14 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | 16 MHz | X | V | V |
| | $I_{DD2}$ | - | 6.9 | - | mA | 3.6 V | 16 MHz | X | V | X |
| | $I_{DD3}$ | - | 13.1 | - | mA | 2.2 V | 16 MHz | X | V | V |
| | $I_{DD4}$ | - | 6.7 | - | mA | 2.2 V | 16 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =36 MHz while(1){}executed from flash $V_{LDO}$=1.8 V | $I_{DD5}$ | - | 13.7 | - | mA | 3.6 V | 12 MHz | X | V | V |
| | $I_{DD6}$ | - | 6.7 | - | mA | 3.6 V | 12 MHz | X | V | X |
| | $I_{DD7}$ | - | 12.9 | - | mA | 2.2 V | 12 MHz | X | V | V |
| | $I_{DD8}$ | - | 6.6 | - | mA | 2.2 V | 12 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =36 MHz while(1){}executed from flash $V_{LDO}$=1.8 V | $I_{DD10}$ | - | 13.6 | - | mA | 3.6 V | 4 MHz | X | V | V |
| | $I_{DD11}$ | - | 6.4 | - | mA | 3.6 V | 4 MHz | X | V | X |
| | $I_{DD12}$ | - | 12.8 | - | mA | 2.2 V | 4 MHz | X | V | V |
| | $I_{DD13}$ | - | 6.3 | - | mA | 2.2 V | 4 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =36 MHz while(1){}executed from flash | $I_{DD14}$ | - | 13.6 | - | mA | $V_{DD}$ | HXT | HIRC1 | PLL | All digital module |
| | | | | | | 3.6 V | X | 36 MHz | X | V |
| | $I_{DD15}$ | - | 6.7 | - | mA | 3.6 V | X | 36 MHz | X | X |

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| V<sub>LDO</sub>=1.8 V | I<sub>DD16</sub> | - | 12.8 | - | mA | 2.2 V | X | 36 MHz | X | V |
| | I<sub>DD17</sub> | - | 6.3 | - | mA | 2.2 V | X | 36 MHz | X | X |
| Operating Current Normal Run Mode HCLK =36 MHz while(1){}executed from flash V<sub>LDO</sub>=1.8 V | I<sub>DD18</sub> | - | 14.5 | - | mA | V<sub>DD</sub> | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | X | 16 MHz | V | V |
| | I<sub>DD19</sub> | - | 6.7 | - | mA | 3.6 V | X | 16 MHz | V | X |
| | I<sub>DD20</sub> | - | 13.6 | - | mA | 2.2 V | X | 16 MHz | V | V |
| | I<sub>DD21</sub> | - | 6.5 | - | mA | 2.2 V | X | 16 MHz | V | X |
| Operating Current Normal Run Mode HCLK =36 MHz while(1){}executed from flash V<sub>LDO</sub>=1.8 V | I<sub>DD22</sub> | - | 14.5 | - | mA | 3.6 V | X | 12 MHz | V | V |
| | I<sub>DD23</sub> | - | 6.7 | - | mA | 3.6 V | X | 12 MHz | V | X |
| | I<sub>DD24</sub> | - | 13.6 | - | mA | 2.2 V | X | 12 MHz | V | V |
| | I<sub>DD25</sub> | - | 6.6 | - | mA | 2.2 V | X | 12 MHz | V | X |
| Operating Current Normal Run Mode HCLK =36 MHz while(1){}executed from flash V<sub>LDO</sub>=1.8 V | I<sub>DD26</sub> | - | 13.3 | - | mA | V<sub>DD</sub> | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | V | V |
| | I<sub>DD27</sub> | - | 6.4 | - | mA | 3.6 V | X | 4 MHz | V | X |
| | I<sub>DD28</sub> | - | 12.6 | - | mA | 2.2 V | X | 4 MHz | V | V |
| | I<sub>DD29</sub> | - | 6.3 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash V<sub>LDO</sub>=1.8 V | I<sub>DD30</sub> | - | 7.3 | - | mA | V<sub>DD</sub> | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | 18 MHz | X | X | V |
| | I<sub>DD31</sub> | - | 3.8 | - | mA | 3.6 V | 18 MHz | X | X | X |
| | I<sub>DD32</sub> | - | 7.1 | - | mA | 2.2 V | 18 MHz | X | X | V |
| | I<sub>DD33</sub> | - | 3.7 | - | mA | 2.2 V | 18 MHz | X | X | X |
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash V<sub>LDO</sub>=1.8 V | I<sub>DD34</sub> | - | 7.5 | - | mA | 3.6 V | 16 MHz | X | V | V |
| | I<sub>DD35</sub> | - | 3.9 | - | mA | 3.6 V | 16 MHz | X | V | X |
| | I<sub>DD36</sub> | - | 7.3 | - | mA | 2.2 V | 16 MHz | X | V | V |
| | I<sub>DD37</sub> | - | 3.8 | - | mA | 2.2 V | 16 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash V<sub>LDO</sub>=1.8 V | I<sub>DD38</sub> | - | 7.3 | - | mA | 3.6 V | 12 MHz | X | V | V |
| | I<sub>DD39</sub> | - | 3.7 | - | mA | 3.6 V | 12 MHz | X | V | X |
| | I<sub>DD40</sub> | - | 7.1 | - | mA | 2.2 V | 12 MHz | X | V | V |
| | I<sub>DD41</sub> | - | 3.7 | - | mA | 2.2 V | 12 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed | I<sub>DD42</sub> | - | 7.1 | - | mA | 3.6 V | 4 MHz | X | V | V |
| | I<sub>DD43</sub> | - | 3.5 | - | mA | 3.6 V | 4 MHz | X | V | X |
| | I<sub>DD44</sub> | - | 6.9 | - | mA | 2.2 V | 4 MHz | X | V | V |

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| from flash $V_{LDO}$=1.8 V | $I_{DD45}$ | - | 3.5 | - | mA | 2.2 V | 4 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash $V_{LDO}$=1.8 V | $I_{DD46}$ | - | 7.9 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | X | 16 MHz | V | V |
| | $I_{DD47}$ | - | 3.7 | - | mA | 3.6 V | X | 16 MHz | V | X |
| | $I_{DD48}$ | - | 7.7 | - | mA | 2.2 V | X | 16 MHz | V | V |
| | $I_{DD49}$ | - | 3.7 | - | mA | 2.2 V | X | 16 MHz | V | X |
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash $V_{LDO1}$=1.8 V | $I_{DD50}$ | - | 7.7 | - | mA | 3.6 V | X | 12 MHz | V | V |
| | $I_{DD51}$ | - | 3.7 | - | mA | 3.6 V | X | 12 MHz | V | X |
| | $I_{DD52}$ | - | 7.5 | - | mA | 2.2 V | X | 12 MHz | V | V |
| | $I_{DD53}$ | - | 3.6 | - | mA | 2.2 V | X | 12 MHz | V | X |
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash $V_{LDO}$=1.8 V | $I_{DD54}$ | - | 6.9 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | V | V |
| | $I_{DD55}$ | - | 3.4 | - | mA | 3.6 V | X | 4 MHz | V | X |
| | $I_{DD56}$ | - | 6.8 | - | mA | 2.2 V | X | 4 MHz | V | V |
| | $I_{DD57}$ | - | 3.4 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash $V_{LDO}$=1.8 V | $I_{DD58}$ | - | 6.5 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | 16 MHz | X | X | V |
| | $I_{DD59}$ | - | 3.3 | - | mA | 3.6 V | 16 MHz | X | X | X |
| | $I_{DD60}$ | - | 6.3 | - | mA | 2.2 V | 16 MHz | X | X | V |
| | $I_{DD61}$ | - | 3.3 | - | mA | 2.2 V | 16 MHz | X | X | X |
| Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash $V_{LDO1}$=1.8 V | $I_{DD62}$ | - | 6.5 | - | mA | 3.6 V | 12 MHz | X | V | V |
| | $I_{DD63}$ | - | 3.4 | - | mA | 3.6 V | 12 MHz | X | V | X |
| | $I_{DD64}$ | - | 6.4 | - | mA | 2.2 V | 12 MHz | X | V | V |
| | $I_{DD65}$ | - | 3.4 | - | mA | 2.2 V | 12 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash $V_{LDO1}$=1.8 V | $I_{DD66}$ | - | 6.3 | - | mA | 3.6 V | 4 MHz | X | V | V |
| | $I_{DD67}$ | - | 3.1 | - | mA | 3.6 V | 4 MHz | X | V | X |
| | $I_{DD68}$ | - | 6.3 | - | mA | 2.2 V | 4 MHz | X | V | V |
| | $I_{DD69}$ | - | 3.1 | - | mA | 2.2 V | 4 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash $V_{LDO}$=1.8 V | $I_{DD70}$ | - | 6.8 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | X | 16 MHz | X | V |
| | $I_{DD71}$ | - | 3.1 | - | mA | 3.6 V | X | 16 MHz | X | X |
| | $I_{DD72}$ | - | 6.7 | - | mA | 2.2 V | X | 16 MHz | X | V |

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| | IDD73 | - | 3.1 | - | mA | 2.2 V | X | 16 MHz | X | X |
| Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash $V_{LDO1}$=1.8 V | IDD74 | - | 7 | - | mA | 3.6 V | X | 12 MHz | V | V |
| | IDD75 | - | 3.3 | - | mA | 3.6 V | X | 12 MHz | V | X |
| | IDD76 | - | 6.8 | - | mA | 2.2 V | X | 12 MHz | V | V |
| | IDD77 | - | 3.2 | - | mA | 2.2 V | X | 12 MHz | V | X |
| Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash $V_{LDO}$=1.8 V | IDD78 | - | 6.2 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | V | V |
| | IDD79 | - | 3.1 | - | mA | 3.6 V | X | 4 MHz | V | X |
| | IDD80 | - | 6.1 | - | mA | 2.2 V | X | 4 MHz | V | V |
| | IDD81 | - | 3.1 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash $V_{LDO}$=1.8 V | IDD82 | - | 4.9 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | 12 MHz | X | X | V |
| | IDD83 | - | 2.5 | - | mA | 3.6 V | 12 MHz | X | X | X |
| | IDD84 | - | 4.8 | - | mA | 2.2 V | 12 MHz | X | X | V |
| | IDD85 | - | 2.5 | - | mA | 2.2 V | 12 MHz | X | X | X |
| Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash $V_{LDO}$=1.8 V | IDD86 | - | 4.9 | - | mA | 3.6 V | 4 MHz | X | V | V |
| | IDD87 | - | 2.5 | - | mA | 3.6 V | 4 MHz | X | V | X |
| | IDD88 | - | 4.8 | - | mA | 2.2 V | 4 MHz | X | V | V |
| | IDD89 | - | 2.5 | - | mA | 2.2 V | 4 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash $V_{LDO}$=1.8 V | IDD90 | - | 5.3 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | X | 12 MHz | X | V |
| | IDD91 | - | 2.5 | - | mA | 3.6 V | X | 12 MHz | X | X |
| | IDD92 | - | 5.2 | - | mA | 2.2 V | X | 12 MHz | X | V |
| | IDD93 | - | 2.5 | - | mA | 2.2 V | X | 12 MHz | X | X |
| Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash $V_{LDO}$=1.8 V | IDD94 | - | 4.8 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | V | V |
| | IDD95 | - | 2.4 | - | mA | 3.6 V | X | 4 MHz | V | X |
| | IDD96 | - | 4.7 | - | mA | 2.2 V | X | 4 MHz | V | V |
| | IDD97 | - | 2.4 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Normal Run Mode HCLK =4 MHz while(1){}executed from flash | IDD98 | - | 1.1 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | 4 MHz | X | X | V |
| | IDD99 | - | 0.7 | - | mA | 3.6 V | 4 MHz | X | X | X |

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{LDO}$=1.8 V | $I_{DD100}$ | - | 1.1 | - | mA | 2.2 V | 4 MHz | X | X | V |
|  | $I_{DD101}$ | - | 0.7 | - | mA | 2.2 V | 4 MHz | X | X | X |
| Operating Current Normal Run Mode HCLK =4 MHz while(1){}executed from flash $V_{LDO}$=1.8 V | $I_{DD102}$ | - | 1.7 | - | mA | 3.6 V | X | 4 MHz | X | V |
|  | $I_{DD103}$ | - | 1 | - | mA | 3.6 V | X | 4 MHz | X | X |
|  | $I_{DD104}$ | - | 1.7 | - | mA | 2.2 V | X | 4 MHz | X | V |
|  | $I_{DD105}$ | - | 0.9 | - | mA | 2.2 V | X | 4 MHz | X | X |
| Operating Current Normal Run Mode HCLK =32.768 kHz while(1){}executed from flash $V_{LDO}$=1.8 V | $I_{DD106}$ | - | 148 | - | uA | $V_{DD}$ | LXT | LIRC | PLL | All digital module |
|  |  |  |  |  |  | 3.6 V | 32.768 kHz | X | X | V |
|  | $I_{DD107}$ | - | 130 | - | uA | 3.6 V | 32.768 kHz | X | X | X |
|  | $I_{DD108}$ | - | 126 | - | uA | 2.2 V | 32.768 kHz | X | X | V |
|  | $I_{DD109}$ | - | 120 | - | uA | 2.2 V | 32.768 kHz | X | X | X |
| Operating Current Normal Run Mode HCLK =10 kHz while(1){}executed from flash $V_{LDO}$=1.8 V | $I_{DD110}$ | - | 128 | - | uA | 3.6 V | X | 10 kHz | X | V |
|  | $I_{DD111}$ | - | 126 | - | uA | 3.6 V | X | 10 kHz | X | X |
|  | $I_{DD112}$ | - | 118 | - | uA | 2.2 V | X | 10 kHz | X | V |
|  | $I_{DD113}$ | - | 116 | - | uA | 2.2 V | X | 10 kHz | X | X |
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash $V_{LDO}$=1.6 V | $I_{DD114}$ | - | 6.5 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
|  |  |  |  |  |  | 3.6 V | 18 MHz | X | X | V |
|  | $I_{DD115}$ | - | 3.4 | - | mA | 3.6 V | 18 MHz | X | X | X |
|  | $I_{DD116}$ | - | 6.4 | - | mA | 2.2 V | 18 MHz | X | X | V |
|  | $I_{DD117}$ | - | 3.3 | - | mA | 2.2 V | 18 MHz | X | X | X |
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash $V_{LDO}$=1.6 V | $I_{DD118}$ | - | 6.6 | - | mA | 3.6 V | 16 MHz | X | V | V |
|  | $I_{DD119}$ | - | 3.5 | - | mA | 3.6 V | 16 MHz | X | V | X |
|  | $I_{DD120}$ | - | 6.6 | - | mA | 2.2 V | 16 MHz | X | V | V |
|  | $I_{DD121}$ | - | 3.4 | - | mA | 2.2 V | 16 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash $V_{LDO}$=1.6 V | $I_{DD122}$ | - | 6.5 | - | mA | 3.6 V | 12 MHz | X | V | V |
|  | $I_{DD123}$ | - | 3.3 | - | mA | 3.6 V | 12 MHz | X | V | X |
|  | $I_{DD124}$ | - | 6.4 | - | mA | 2.2 V | 12 MHz | X | V | V |
|  | $I_{DD125}$ | - | 3.3 | - | mA | 2.2 V | 12 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash $V_{LDO}$=1.6 V | $I_{DD126}$ | - | 6.2 | - | mA | 3.6 V | 4 MHz | X | V | V |
|  | $I_{DD127}$ | - | 3.1 | - | mA | 3.6 V | 4 MHz | X | V | X |
|  | $I_{DD128}$ | - | 6.2 | - | mA | 2.2 V | 4 MHz | X | V | V |
|  | $I_{DD129}$ | - | 3.1 | - | mA | 2.2 V | 4 MHz | X | V | X |

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | VDD | HXT | HIRC0 | PLL | All digital module |
|---|---|---|---|---|---|---|---|---|---|---|
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash V_LDO=1.6 V | I_DD130 | - | 7 | - | mA | 3.6 V | X | 16 MHz | V | V |
| | I_DD131 | - | 3.3 | - | mA | 3.6 V | X | 16 MHz | V | X |
| | I_DD132 | - | 7 | - | mA | 2.2 V | X | 16 MHz | V | V |
| | I_DD133 | - | 3.3 | - | mA | 2.2 V | X | 16 MHz | V | X |
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash V_LDO1=1.6 V | I_DD134 | - | 6.9 | - | mA | 3.6 V | X | 12 MHz | V | V |
| | I_DD135 | - | 3.3 | - | mA | 3.6 V | X | 12 MHz | V | X |
| | I_DD136 | - | 6.8 | - | mA | 2.2 V | X | 12 MHz | V | V |
| | I_DD137 | - | 3.3 | - | mA | 2.2 V | X | 12 MHz | V | X |
| Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash V_LDO=1.6 V | I_DD138 | - | 6.2 | - | mA | 3.6 V | X | 4 MHz | V | V |
| | I_DD139 | - | 3.1 | - | mA | 3.6 V | X | 4 MHz | V | X |
| | I_DD140 | - | 6.1 | - | mA | 2.2 V | X | 4 MHz | V | V |
| | I_DD141 | - | 3 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_LDO=1.6 V | I_DD142 | - | 5.7 | - | mA | 3.6 V | 16 MHz | X | X | V |
| | I_DD143 | - | 2.9 | - | mA | 3.6 V | 16 MHz | X | X | X |
| | I_DD144 | - | 5.7 | - | mA | 2.2 V | 16 MHz | X | X | V |
| | I_DD145 | - | 2.9 | - | mA | 2.2 V | 16 MHz | X | X | X |
| Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_LDO1=1.6 V | I_DD146 | - | 5.8 | - | mA | 3.6 V | 12 MHz | X | V | V |
| | I_DD147 | - | 3 | - | mA | 3.6 V | 12 MHz | X | V | X |
| | I_DD148 | - | 5.7 | - | mA | 2.2 V | 12 MHz | X | V | V |
| | I_DD149 | - | 3 | - | mA | 2.2 V | 12 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_LDO1=1.6 V | I_DD150 | - | 5.6 | - | mA | 3.6 V | 4 MHz | X | V | V |
| | I_DD151 | - | 2.8 | - | mA | 3.6 V | 4 MHz | X | V | X |
| | I_DD152 | - | 5.6 | - | mA | 2.2 V | 4 MHz | X | V | V |
| | I_DD153 | - | 2.8 | - | mA | 2.2 V | 4 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_LDO=1.6 V | I_DD154 | - | 6 | - | mA | 3.6 V | X | 16 MHz | X | V |
| | I_DD155 | - | 2.8 | - | mA | 3.6 V | X | 16 MHz | X | X |
| | I_DD156 | - | 5.9 | - | mA | 2.2 V | X | 16 MHz | X | V |
| | I_DD157 | - | 2.8 | - | mA | 2.2 V | X | 16 MHz | X | X |

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash $V_{LDO1}$=1.6 V | $I_{DD158}$ | - | 6.2 | - | mA | 3.6 V | X | 12 MHz | V | V |
| | $I_{DD159}$ | - | 3 | - | mA | 3.6 V | X | 12 MHz | V | X |
| | $I_{DD160}$ | - | 6.2 | - | mA | 2.2 V | X | 12 MHz | V | V |
| | $I_{DD161}$ | - | 3 | - | mA | 2.2 V | X | 12 MHz | V | X |
| Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash $V_{LDO}$=1.6 V | $I_{DD162}$ | - | 5.5 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | V | V |
| | $I_{DD163}$ | - | 2.8 | - | mA | 3.6 V | X | 4 MHz | V | X |
| | $I_{DD164}$ | - | 5.5 | - | mA | 2.2 V | X | 4 MHz | V | V |
| | $I_{DD165}$ | - | 2.8 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash $V_{LDO}$=1.6 V | $I_{DD166}$ | - | 4.3 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | 12 MHz | X | X | V |
| | $I_{DD167}$ | - | 2.2 | - | mA | 3.6 V | 12 MHz | X | X | X |
| | $I_{DD168}$ | - | 4.3 | - | mA | 2.2 V | 12 MHz | X | X | V |
| | $I_{DD169}$ | - | 2.2 | - | mA | 2.2 V | 12 MHz | X | X | X |
| Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash $V_{LDO}$=1.6 V | $I_{DD170}$ | - | 4.3 | - | mA | 3.6 V | 4 MHz | X | V | V |
| | $I_{DD171}$ | - | 2.3 | - | mA | 3.6 V | 4 MHz | X | V | X |
| | $I_{DD172}$ | - | 4.3 | - | mA | 2.2 V | 4 MHz | X | V | V |
| | $I_{DD173}$ | - | 2.3 | - | mA | 2.2 V | 4 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash $V_{LDO}$=1.6 V | $I_{DD174}$ | - | 4.7 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | X | 12 MHz | X | V |
| | $I_{DD175}$ | - | 2.2 | - | mA | 3.6 V | X | 12 MHz | X | X |
| | $I_{DD176}$ | - | 4.7 | - | mA | 2.2 V | X | 12 MHz | X | V |
| | $I_{DD177}$ | - | 2.2 | - | mA | 2.2 V | X | 12 MHz | X | X |
| Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash $V_{LDO}$=1.6 V | $I_{DD178}$ | - | 4.3 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | V | V |
| | $I_{DD179}$ | - | 2.2 | - | mA | 3.6 V | X | 4 MHz | V | X |
| | $I_{DD180}$ | - | 4.2 | - | mA | 2.2 V | X | 4 MHz | V | V |
| | $I_{DD181}$ | - | 2.2 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Normal Run Mode HCLK =4 MHz while(1){}executed from flash $V_{LDO}$=1.6 V | $I_{DD182}$ | - | 1 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | 4 MHz | X | X | V |
| | $I_{DD183}$ | - | 0.6 | - | mA | 3.6 V | 4 MHz | X | X | X |
| | $I_{DD184}$ | - | 1 | - | mA | 2.2 V | 4 MHz | X | X | V |

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $I_{DD185}$ | - | 0.6 | - | mA | 2.2 V | 4 MHz | X | X | X |
| Operating Current Normal Run Mode HCLK =4 MHz while(1){}executed from flash $V_{LDO}$=1.6 V | $I_{DD186}$ | - | 1.6 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | X | V |
| | $I_{DD187}$ | - | 0.9 | - | mA | 3.6 V | X | 4 MHz | X | X |
| | $I_{DD188}$ | - | 1.5 | - | mA | 2.2 V | X | 4 MHz | X | V |
| | $I_{DD189}$ | - | 0.9 | - | mA | 2.2 V | X | 4 MHz | X | X |
| Operating Current Normal Run Mode HCLK =32.768 kHz while(1){}executed from flash $V_{LDO}$=1.6 V | $I_{DD190}$ | - | 147 | - | uA | $V_{DD}$ | LXT | LIRC | PLL | All digital module |
| | | | | | | 3.6 V | 32.768 kHz | X | X | V |
| | $I_{DD191}$ | - | 141 | - | uA | 3.6 V | 32.768 kHz | X | X | X |
| | $I_{DD192}$ | - | 124 | - | uA | 2.2 V | 32.768 kHz | X | X | V |
| | $I_{DD193}$ | - | 119 | - | uA | 2.2 V | 32.768 kHz | X | X | X |
| Operating Current Normal Run Mode HCLK =10 kHz while(1){}executed from flash $V_{LDO}$=1.6 V | $I_{DD194}$ | - | 139 | - | uA | 3.6 V | X | 10 kHz | X | V |
| | $I_{DD195}$ | - | 137 | - | uA | 3.6 V | X | 10 kHz | X | X |
| | $I_{DD196}$ | - | 117 | - | uA | 2.2 V | X | 10 kHz | X | V |
| | $I_{DD197}$ | - | 115 | - | uA | 2.2 V | X | 10 kHz | X | X |
| Operating Current Normal Run Mode HCLK =2 MHz while(1){}executed from flash $V_{LDO}$=1.2 V | $I_{DD198}$ | - | 0.9 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | 4 MHz | X | X | V |
| | $I_{DD199}$ | - | 0.6 | - | mA | 3.6 V | 4 MHz | X | X | X |
| | $I_{DD200}$ | - | 0.9 | - | mA | 2.2 V | 4 MHz | X | X | V |
| | $I_{DD4}$ | - | 0.6 | - | mA | 2.2 V | 4 MHz | X | X | X |
| Operating Current Normal Run Mode HCLK =2 MHz while(1){}executed from flash $V_{LDO}$=1.2 V | $I_{DD201}$ | - | 0.8 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | X | V |
| | $I_{DD202}$ | - | 0.5 | - | mA | 3.6 V | X | 4 MHz | X | X |
| | $I_{DD203}$ | - | 0.8 | - | mA | 2.2 V | X | 4 MHz | X | V |
| | $I_{DD204}$ | - | 0.5 | - | mA | 2.2 V | X | 4 MHz | X | X |
| Operating Current Normal Run Mode HCLK =32 kHz while(1){}executed from flash $V_{LDO}$=1.2 V | $I_{DD205}$ | - | 218 | - | uA | $V_{DD}$ | LXT | LIRC | PLL | All digital module |
| | | | | | | 3.6 V | 32.768 kHz | X | X | V |
| | $I_{DD206}$ | - | 225 | - | uA | 3.6 V | 32.768 kHz | X | X | X |
| | $I_{DD207}$ | - | 206 | - | uA | 2.2 V | 32.768 kHz | X | X | V |
| | $I_{DD208}$ | - | 202 | - | uA | 2.2 V | 32.768 kHz | X | X | X |
| Operating Current Normal Run Mode HCLK =10 kHz | $I_{DD209}$ | - | 122 | - | uA | $V_{DD}$ | LXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 10 kHz | X | V |

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| while(1){}executed from flash $V_{LDO}$=1.2 V | $I_{DD210}$ | - | 121 | - | uA | 3.6 V | X | 10 kHz | X | X |
| | $I_{DD211}$ | - | 112 | - | uA | 2.2 V | X | 10 kHz | X | V |
| | $I_{DD212}$ | - | 111 | - | uA | 2.2 V | X | 10 kHz | X | X |
| Operating Current Idle Mode HCLK =36 MHz $V_{LDO}$=1.8 V | $I_{IDLE1}$ | - | 9.5 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | 16 MHz | X | V | V |
| | $I_{IDLE2}$ | - | 2.4 | - | mA | 3.6 V | 16 MHz | X | V | X |
| | $I_{IDLE3}$ | - | 9.1 | - | mA | 2.2 V | 16 MHz | X | V | V |
| | $I_{IDLE4}$ | - | 2.4 | - | mA | 2.2 V | 16 MHz | X | V | X |
| Operating Current Idle Mode HCLK =36 MHz $V_{LDO}$=1.8 V | $I_{IDLE5}$ | - | 9.3 | - | mA | 3.6 V | 12 MHz | X | V | V |
| | $I_{IDLE6}$ | - | 2.2 | - | mA | 3.6 V | 12 MHz | X | V | X |
| | $I_{IDLE7}$ | - | 9 | - | mA | 2.2 V | 12 MHz | X | V | V |
| | $I_{IDLE8}$ | - | 2.2 | - | mA | 2.2 V | 12 MHz | X | V | X |
| Operating Current Idle Mode HCLK =36 MHz $V_{LDO}$=1.8 V | $I_{IDLE9}$ | - | 9.1 | - | mA | 3.6 V | 4 MHz | X | V | V |
| | $I_{IDLE10}$ | - | 2 | - | mA | 3.6 V | 4 MHz | X | V | X |
| | $I_{IDLE11}$ | - | 8.8 | - | mA | 2.2 V | 4 MHz | X | V | V |
| | $I_{IDLE12}$ | - | 2 | - | mA | 2.2 V | 4 MHz | X | V | X |
| Operating Current Idle Mode HCLK =36 MHz $V_{LDO}$=1.8 V | $I_{IDLE13}$ | - | 9 | - | mA | $V_{DD}$ | HXT | HIRC1 | PLL | All digital module |
| | | | | | | 3.6 V | X | 36 MHz | X | V |
| | $I_{IDLE14}$ | - | 1.9 | - | mA | 3.6 V | X | 36 MHz | X | X |
| | $I_{IDLE15}$ | - | 8.8 | - | mA | 2.2 V | X | 36 MHz | X | V |
| | $I_{IDLE16}$ | - | 1.9 | - | mA | 2.2 V | X | 36 MHz | X | X |
| Operating Current Idle Mode HCLK =36 MHz $V_{LDO}$=1.8 V | $I_{IDLE17}$ | - | 10.1 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | X | 16 MHz | V | V |
| | $I_{IDLE18}$ | - | 2.3 | - | mA | 3.6 V | X | 16 MHz | V | X |
| | $I_{IDLE19}$ | - | 9.7 | - | mA | 2.2 V | X | 16 MHz | V | V |
| | $I_{IDLE20}$ | - | 2.2 | - | mA | 2.2 V | X | 16 MHz | V | X |
| Operating Current Idle Mode HCLK =36 MHz $V_{LDO}$=1.8 V | $I_{IDLE21}$ | - | 10 | - | mA | 3.6 V | X | 12 MHz | V | V |
| | $I_{IDLE22}$ | - | 2.2 | - | mA | 3.6 V | X | 12 MHz | V | X |
| | $I_{IDLE23}$ | - | 9.6 | - | mA | 2.2 V | X | 12 MHz | V | V |
| | $I_{IDLE24}$ | - | 2.2 | - | mA | 2.2 V | X | 12 MHz | V | X |
| Operating Current Idle Mode HCLK =36 MHz | $I_{IDLE25}$ | - | 9 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | V | V |

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{LDO}$=1.8 V | $I_{IDLE26}$ | - | 6.3 | - | mA | 3.6 V | X | 4 MHz | V | X |
|  | $I_{IDLE27}$ | - | 8.7 | - | mA | 2.2 V | X | 4 MHz | V | V |
|  | $I_{IDLE28}$ | - | 6.2 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Idle Mode HCLK =18 MHz $V_{LDO}$=1.8 V | $I_{IDLE29}$ | - | 5 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
|  |  |  |  |  |  | 3.6 V | 18 MHz | X | X | V |
|  | $I_{IDLE30}$ | - | 1.5 | - | mA | 3.6 V | 18 MHz | X | X | X |
|  | $I_{IDLE31}$ | - | 5 | - | mA | 2.2 V | 18 MHz | X | X | V |
|  | $I_{IDLE32}$ | - | 1.5 | - | mA | 2.2 V | 18 MHz | X | X | X |
| Operating Current Idle Mode HCLK =18 MHz $V_{LDO}$=1.8 V | $I_{IDLE33}$ | - | 5.2 | - | mA | 3.6 V | 16 MHz | X | V | V |
|  | $I_{IDLE34}$ | - | 1.7 | - | mA | 3.6 V | 16 MHz | X | V | X |
|  | $I_{IDLE35}$ | - | 5.1 | - | mA | 2.2 V | 16 MHz | X | V | V |
|  | $I_{IDLE36}$ | - | 1.6 | - | mA | 2.2 V | 16 MHz | X | V | X |
| Operating Current Idle Mode HCLK =18 MHz $V_{LDO}$=1.8 V | $I_{IDLE37}$ | - | 5.1 | - | mA | 3.6 V | 12 MHz | X | V | V |
|  | $I_{IDLE38}$ | - | 1.5 | - | mA | 3.6 V | 12 MHz | X | V | X |
|  | $I_{IDLE39}$ | - | 5. | - | mA | 2.2 V | 12 MHz | X | V | V |
|  | $I_{IDLE40}$ | - | 1.5 | - | mA | 2.2 V | 12 MHz | X | V | X |
| Operating Current Idle Mode HCLK =18 MHz $V_{LDO}$=1.8 V | $I_{IDLE41}$ | - | 4.8 | - | mA | 3.6 V | 4 MHz | X | V | V |
|  | $I_{IDLE42}$ | - | 1.3 | - | mA | 3.6 V | 4 MHz | X | V | X |
|  | $I_{IDLE43}$ | - | 4.8 | - | mA | 2.2 V | 4 MHz | X | V | V |
|  | $I_{IDLE44}$ | - | 1.2 | - | mA | 2.2 V | 4 MHz | X | V | X |
| Operating Current Idle Mode HCLK =18 MHz $V_{LDO}$=1.8 V | $I_{IDLE45}$ | - | 5.6 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
|  |  |  |  |  |  | 3.6 V | X | 16 MHz | V | V |
|  | $I_{IDLE46}$ | - | 1.5 | - | mA | 3.6 V | X | 16 MHz | V | X |
|  | $I_{IDLE47}$ | - | 5.6 | - | mA | 2.2 V | X | 16 MHz | V | V |
|  | $I_{IDLE48}$ | - | 1.5 | - | mA | 2.2 V | X | 16 MHz | V | X |
| Operating Current Idle Mode HCLK =18 MHz $V_{LDO}$=1.8 V | $I_{IDLE49}$ | - | 5.5 | - | mA | 3.6 V | X | 12 MHz | V | V |
|  | $I_{IDLE50}$ | - | 3.7 | - | mA | 3.6 V | X | 12 MHz | V | X |
|  | $I_{IDLE51}$ | - | 5.4 | - | mA | 2.2 V | X | 12 MHz | V | V |
|  | $I_{IDLE52}$ | - | 3.6 | - | mA | 2.2 V | X | 12 MHz | V | X |
| Operating Current Idle Mode HCLK =18 MHz $V_{LDO}$=1.8 V | $I_{IDLE53}$ | - | 4.7 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
|  |  |  |  |  |  | 3.6 V | X | 4 MHz | V | V |
|  | $I_{IDLE54}$ | - | 1.2 | - | mA | 3.6 V | X | 4 MHz | V | X |

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| | $I_{IDLE55}$ | - | 4.7 | - | mA | 2.2 V | X | 4 MHz | V | V |
| | $I_{IDLE56}$ | - | 1.2 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Idle Mode HCLK =16 MHz $V_{LDO}$=1.8 V | $I_{IDLE57}$ | - | 4.5 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | 16 MHz | X | X | V |
| | $I_{IDLE58}$ | - | 1.3 | - | mA | 3.6 V | 16 MHz | X | X | X |
| | $I_{IDLE59}$ | - | 4.4 | - | mA | 2.2 V | 16 MHz | X | X | V |
| | $I_{IDLE60}$ | - | 1.3 | - | mA | 2.2 V | 16 MHz | X | X | X |
| Operating Current Idle Mode HCLK =16 MHz $V_{LDO}$=1.8 V | $I_{IDLE61}$ | - | 4.6 | - | mA | 3.6 V | 12 MHz | X | V | V |
| | $I_{IDLE62}$ | - | 1.4 | - | mA | 3.6 V | 12 MHz | X | V | X |
| | $I_{IDLE63}$ | - | 4.5 | - | mA | 2.2 V | 12 MHz | X | V | V |
| | $I_{IDLE64}$ | - | 1.4 | - | mA | 2.2 V | 12 MHz | X | V | X |
| Operating Current Idle Mode HCLK =16 MHz $V_{LDO}$=1.8 V | $I_{IDLE65}$ | - | 4.3 | - | mA | 3.6 V | 4 MHz | X | V | V |
| | $I_{IDLE66}$ | - | 1.2 | - | mA | 3.6 V | 4 MHz | X | V | X |
| | $I_{IDLE67}$ | - | 4.3 | - | mA | 2.2 V | 4 MHz | X | V | V |
| | $I_{IDLE68}$ | - | 1.2 | - | mA | 2.2 V | 4 MHz | X | V | X |
| Operating Current Idle Mode HCLK =16 MHz $V_{LDO}$=1.8 V | $I_{IDLE69}$ | - | 4.9 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | X | 16 MHz | X | V |
| | $I_{IDLE70}$ | - | 1.2 | - | mA | 3.6 V | X | 16 MHz | X | X |
| | $I_{IDLE71}$ | - | 4.8 | - | mA | 2.2 V | X | 16 MHz | X | V |
| | $I_{IDLE72}$ | - | 1.2 | - | mA | 2.2 V | X | 16 MHz | X | X |
| Operating Current Idle Mode HCLK =16 MHz $V_{LDO}$=1.8 V | $I_{IDLE73}$ | - | 5 | - | mA | 3.6 V | X | 12 MHz | V | V |
| | $I_{IDLE74}$ | - | 1.4 | - | mA | 3.6 V | X | 12 MHz | V | X |
| | $I_{IDLE75}$ | - | 5 | - | mA | 2.2 V | X | 12 MHz | V | V |
| | $I_{IDLE76}$ | - | 1.4 | - | mA | 2.2 V | X | 12 MHz | V | X |
| Operating Current Idle Mode HCLK =16 MHz $V_{LDO}$=1.8 V | $I_{IDLE77}$ | - | 4.3 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | V | V |
| | $I_{IDLE78}$ | - | 1.1 | - | mA | 3.6 V | X | 4 MHz | V | X |
| | $I_{IDLE79}$ | - | 4.2 | - | mA | 2.2 V | X | 4 MHz | V | V |
| | $I_{IDLE80}$ | - | 1.1 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Idle Mode HCLK =12 MHz $V_{LDO}$=1.8 V | $I_{IDLE81}$ | - | 3.4 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | 12 MHz | X | X | V |
| | $I_{IDLE82}$ | - | 1 | - | mA | 3.6 V | 12 MHz | X | X | X |

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| | $I_{IDLE83}$ | - | 3.3 | - | mA | 2.2 V | 12 MHz | X | X | V |
| | $I_{IDLE84}$ | - | 1 | - | mA | 2.2 V | 12 MHz | X | X | X |
| Operating Current Idle Mode HCLK =12 MHz $V_{LDO}$=1.8 V | $I_{IDLE85}$ | - | 3.4 | - | mA | 3.6 V | 4 MHz | X | V | V |
| | $I_{IDLE86}$ | - | 1 | - | mA | 3.6 V | 4 MHz | X | V | X |
| | $I_{IDLE87}$ | - | 3.3 | - | mA | 2.2 V | 4 MHz | X | V | V |
| | $I_{IDLE88}$ | - | 1 | - | mA | 2.2 V | 4 MHz | X | V | X |
| Operating Current Idle Mode HCLK =12 MHz $V_{LDO}$=1.8 V | $I_{IDLE89}$ | - | 3.8 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | X | 12 MHz | X | V |
| | $I_{IDLE90}$ | - | 1 | - | mA | 3.6 V | X | 12 MHz | X | X |
| | $I_{IDLE91}$ | - | 3.7 | - | mA | 2.2 V | X | 12 MHz | X | V |
| | $I_{IDLE92}$ | - | 1 | - | mA | 2.2 V | X | 12 MHz | X | X |
| Operating Current Idle Mode HCLK =12 MHz $V_{LDO}$=1.8 V | $I_{IDLE93}$ | - | 3.3 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | V | V |
| | $I_{IDLE94}$ | - | 1 | - | mA | 3.6 V | X | 4 MHz | V | X |
| | $I_{IDLE95}$ | - | 3.3 | - | mA | 2.2 V | X | 4 MHz | V | V |
| | $I_{IDLE96}$ | - | 0.9 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Idle Mode HCLK =4 MHz $V_{LDO}$=1.8 V | $I_{IDLE97}$ | - | 0.9 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | 4 MHz | X | X | V |
| | $I_{IDLE98}$ | - | 0.5 | - | mA | 3.6 V | 4 MHz | X | X | X |
| | $I_{IDLE99}$ | - | 0.9 | - | mA | 2.2 V | 4 MHz | X | X | V |
| | $I_{IDLE100}$ | - | 0.4 | - | mA | 2.2 V | 4 MHz | X | X | X |
| Operating Current Idle Mode HCLK =4 MHz $V_{LDO}$=1.8 V | $I_{IDLE101}$ | - | 1.2 | - | mA | 3.6 V | X | 4 MHz | X | V |
| | $I_{IDLE102}$ | - | 0.5 | - | mA | 3.6 V | X | 4 MHz | X | X |
| | $I_{IDLE103}$ | - | 1.2 | - | mA | 2.2 V | X | 4 MHz | X | V |
| | $I_{IDLE104}$ | - | 0.4 | - | mA | 2.2 V | X | 4 MHz | X | X |
| Operating Current Idle Mode HCLK =32.768 kHz $V_{LDO}$=1.8 V | $I_{IDLE105}$ | - | 132 | - | uA | $V_{DD}$ | LXT | LIRC | PLL | All digital module |
| | | | | | | 3.6 V | 32.768 kHz | X | X | V |
| | $I_{IDLE106}$ | - | 126 | - | uA | 3.6 V | 32.768 kHz | X | X | X |
| | $I_{IDLE107}$ | - | 122 | - | uA | 2.2 V | 32.768 kHz | X | X | V |
| | $I_{IDLE108}$ | - | 116 | - | uA | 2.2 V | 32.768 kHz | X | X | X |
| Operating Current Operating Current Idle Mode | $I_{IDLE109}$ | - | 127 | - | uA | 3.6 V | X | 10 kHz | X | V |
| | $I_{IDLE110}$ | - | 125 | - | uA | 3.6 V | X | 10 kHz | X | X |

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| HCLK =10 kHz V$_{LDO}$=1.8 V | I$_{IDLE111}$ | - | 116 | - | uA | 2.2 V | X | 10 kHz | X | V |
| | I$_{IDLE112}$ | - | 114 | - | uA | 2.2 V | X | 10 kHz | X | X |
| Operating Current Idle Mode HCLK =18 MHz V$_{LDO}$=1.6 V | I$_{IDLE113}$ | - | 4.5 | - | mA | V$_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | 18 MHz | X | X | V |
| | I$_{IDLE114}$ | - | 1.3 | - | mA | 3.6 V | 18 MHz | X | X | X |
| | I$_{IDLE115}$ | - | 4.4 | - | mA | 2.2 V | 18 MHz | X | X | V |
| | I$_{IDLE116}$ | - | 1.3 | - | mA | 2.2 V | 18 MHz | X | X | X |
| Operating Current Idle Mode HCLK =18 MHz V$_{LDO}$=1.6 V | I$_{IDLE117}$ | - | 4.6 | - | mA | 3.6 V | 16 MHz | X | V | V |
| | I$_{IDLE118}$ | | 1.5 | | mA | 3.6 V | 16 MHz | X | V | X |
| | I$_{IDLE119}$ | - | 4.6 | - | mA | 2.2 V | 16 MHz | X | V | V |
| | I$_{IDLE120}$ | - | 1.4 | - | mA | 2.2 V | 16 MHz | X | V | X |
| Operating Current Idle Mode HCLK =18 MHz V$_{LDO}$=1.6 V | I$_{IDLE121}$ | - | 4.5 | - | mA | 3.6 V | 12 MHz | X | V | V |
| | I$_{IDLE122}$ | | 1.4 | | mA | 3.6 V | 12 MHz | X | V | X |
| | I$_{IDLE123}$ | - | 4.4 | - | mA | 2.2 V | 12 MHz | X | V | V |
| | I$_{IDLE124}$ | - | 1.3 | - | mA | 2.2 V | 12 MHz | X | V | X |
| Operating Current Idle Mode HCLK =18 MHz V$_{LDO}$=1.6 V | I$_{IDLE125}$ | - | 4.3 | - | mA | 3.6 V | 4 MHz | X | V | V |
| | I$_{IDLE126}$ | | 1.1 | | mA | 3.6 V | 4 MHz | X | V | X |
| | I$_{IDLE127}$ | - | 4.2 | - | mA | 2.2 V | 4 MHz | X | V | V |
| | I$_{IDLE128}$ | - | 1.1 | - | mA | 2.2 V | 4 MHz | X | V | X |
| Operating Current Idle Mode HCLK =18 MHz V$_{LDO}$=1.6 V | I$_{IDLE129}$ | - | 5 | - | mA | V$_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | X | 16 MHz | V | V |
| | I$_{IDLE130}$ | - | 1.4 | - | mA | 3.6 V | X | 16 MHz | V | X |
| | I$_{IDLE131}$ | - | 5 | - | mA | 2.2 V | X | 16 MHz | V | V |
| | I$_{IDLE132}$ | - | 1.3 | - | mA | 2.2 V | X | 16 MHz | V | X |
| Operating Current Idle Mode HCLK =18 MHz V$_{LDO}$=1.6 V | I$_{IDLE133}$ | - | 4.9 | - | mA | 3.6 V | X | 12 MHz | V | V |
| | I$_{IDLE134}$ | | 3.3 | | mA | 3.6 V | X | 12 MHz | V | X |
| | I$_{IDLE135}$ | - | 4.8 | - | mA | 2.2 V | X | 12 MHz | V | V |
| | I$_{IDLE136}$ | - | 3.3 | - | mA | 2.2 V | X | 12 MHz | V | X |
| Operating Current Idle Mode HCLK =18 MHz V$_{LDO}$=1.6 V | I$_{IDLE137}$ | - | 4.2 | - | mA | V$_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | V | V |
| | I$_{IDLE138}$ | - | 1.1 | - | mA | 3.6 V | X | 4 MHz | V | X |
| | I$_{IDLE139}$ | - | 4.2 | - | mA | 2.2 V | X | 4 MHz | V | V |

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| | $I_{IDLE140}$ | - | 1.1 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Idle Mode HCLK =16 MHz $V_{LDO}$=1.6 V | $I_{IDLE141}$ | - | 3.9 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | 16 MHz | X | X | V |
| | $I_{IDLE142}$ | - | 1.2 | - | mA | 3.6 V | 16 MHz | X | X | X |
| | $I_{IDLE143}$ | - | 3.9 | - | mA | 2.2 V | 16 MHz | X | X | V |
| | $I_{IDLE144}$ | - | 1.1 | - | mA | 2.2 V | 16 MHz | X | X | X |
| Operating Current Idle Mode HCLK =16 MHz $V_{LDO}$=1.6 V | $I_{IDLE145}$ | - | 4.1 | - | mA | 3.6 V | 12 MHz | X | V | V |
| | $I_{IDLE146}$ | - | 1.3 | - | mA | 3.6 V | 12 MHz | X | V | X |
| | $I_{IDLE147}$ | - | 4 | - | mA | 2.2 V | 12 MHz | X | V | V |
| | $I_{IDLE148}$ | - | 1.3 | - | mA | 2.2 V | 12 MHz | X | V | X |
| Operating Current Idle Mode HCLK =16 MHz $V_{LDO}$=1.6 V | $I_{IDLE149}$ | - | 3.9 | - | mA | 3.6 V | 4 MHz | X | V | V |
| | $I_{IDLE150}$ | - | 1.1 | - | mA | 3.6 V | 4 MHz | X | V | X |
| | $I_{IDLE151}$ | - | 3.8 | - | mA | 2.2 V | 4 MHz | X | V | V |
| | $I_{IDLE152}$ | - | 1 | - | mA | 2.2 V | 4 MHz | X | V | X |
| Operating Current Idle Mode HCLK =16 MHz $V_{LDO}$=1.6 V | $I_{IDLE153}$ | - | 4.3 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | X | 16 MHz | X | V |
| | $I_{IDLE154}$ | - | 1.1 | - | mA | 3.6 V | X | 16 MHz | X | X |
| | $I_{IDLE155}$ | - | 4.3 | - | mA | 2.2 V | X | 16 MHz | X | V |
| | $I_{IDLE156}$ | - | 1 | - | mA | 2.2 V | X | 16 MHz | X | X |
| Operating Current Idle Mode HCLK =16 MHz $V_{LDO}$=1.6 V | $I_{IDLE157}$ | - | 4.4 | - | mA | 3.6 V | X | 12 MHz | V | V |
| | $I_{IDLE158}$ | - | 1.3 | - | mA | 3.6 V | X | 12 MHz | V | X |
| | $I_{IDLE159}$ | - | 4.4 | - | mA | 2.2 V | X | 12 MHz | V | V |
| | $I_{IDLE160}$ | - | 1.2 | - | mA | 2.2 V | X | 12 MHz | V | X |
| Operating Current Idle Mode HCLK =16 MHz $V_{LDO}$=1.6 V | $I_{IDLE161}$ | - | 3.8 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | V | V |
| | $I_{IDLE162}$ | - | 1 | - | mA | 3.6 V | X | 4 MHz | V | X |
| | $I_{IDLE163}$ | - | 3.8 | - | mA | 2.2 V | X | 4 MHz | V | V |
| | $I_{IDLE164}$ | - | 1 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Idle Mode HCLK =12 MHz $V_{LDO}$=1.6 V | $I_{IDLE165}$ | - | 3 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | 12 MHz | X | X | V |
| | $I_{IDLE166}$ | - | 0.9 | - | mA | 3.6 V | 12 MHz | X | X | X |
| | $I_{IDLE167}$ | - | 3 | - | mA | 2.2 V | 12 MHz | X | X | V |

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $I_{IDLE168}$ | - | 0.9 | - | mA | 2.2 V | 12 MHz | X | X | X |
| Operating Current Idle Mode HCLK =12 MHz $V_{LDO}$=1.6 V | $I_{IDLE169}$ | - | 3 | - | mA | 3.6 V | 4 MHz | X | V | V |
| | $I_{IDLE170}$ | - | 0.9 | - | mA | 3.6 V | 4 MHz | X | V | X |
| | $I_{IDLE171}$ | - | 3 | - | mA | 2.2 V | 4 MHz | X | V | V |
| | $I_{IDLE172}$ | - | 0.9 | - | mA | 2.2 V | 4 MHz | X | V | X |
| Operating Current Idle Mode HCLK =12 MHz $V_{LDO}$=1.6 V | $I_{IDLE173}$ | - | 3.4 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | X | 12 MHz | X | V |
| | $I_{IDLE174}$ | - | 0.9 | - | mA | 3.6 V | X | 12 MHz | X | X |
| | $I_{IDLE175}$ | - | 3.3 | - | mA | 2.2 V | X | 12 MHz | X | V |
| | $I_{IDLE176}$ | - | 0.9 | - | mA | 2.2 V | X | 12 MHz | X | X |
| Operating Current Idle Mode HCLK =12 MHz $V_{LDO}$=1.6 V | $I_{IDLE177}$ | - | 3 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | V | V |
| | $I_{IDLE178}$ | - | 0.9 | - | mA | 3.6 V | X | 4 MHz | V | X |
| | $I_{IDLE179}$ | - | 2.9 | - | mA | 2.2 V | X | 4 MHz | V | V |
| | $I_{IDLE180}$ | - | 0.9 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Idle Mode HCLK =4 MHz $V_{LDO}$=1.6 V | $I_{IDLE181}$ | - | 0.8 | - | mA | $V_{DD}$ | HXT | HIRC0 | PLL | All digital module |
| | | | | | | 3.6 V | 4 MHz | X | X | V |
| | $I_{IDLE182}$ | - | 0.4 | - | mA | 3.6 V | 4 MHz | X | X | X |
| | $I_{IDLE183}$ | - | 0.8 | - | mA | 2.2 V | 4 MHz | X | X | V |
| | $I_{IDLE184}$ | - | 0.4 | - | mA | 2.2 V | 4 MHz | X | X | X |
| Operating Current Idle Mode HCLK =4 MHz $V_{LDO}$=1.6 V | $I_{IDLE185}$ | - | 1.1 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | V | V |
| | $I_{IDLE186}$ | - | 0.4 | - | mA | 3.6 V | X | 4 MHz | V | X |
| | $I_{IDLE187}$ | - | 1.1 | - | mA | 2.2 V | X | 4 MHz | V | V |
| | $I_{IDLE188}$ | - | 0.4 | - | mA | 2.2 V | X | 4 MHz | V | X |
| Operating Current Idle Mode HCLK =32.768 kHz $V_{LDO}$=1.6 V | $I_{IDLE189}$ | - | 143 | - | uA | $V_{DD}$ | LXT | LIRC | PLL | All digital module |
| | | | | | | 3.6 V | 32.768 kHz | X | X | V |
| | $I_{IDLE190}$ | - | 138 | - | uA | 3.6 V | 32.768 kHz | X | X | X |
| | $I_{IDLE191}$ | - | 120 | - | uA | 2.2 V | 32.768 kHz | X | X | V |
| | $I_{IDLE192}$ | - | 115 | - | uA | 2.2 V | 32.768 kHz | X | X | X |
| Operating Current Idle Mode HCLK =10 kHz | $I_{IDLE193}$ | - | 138 | - | uA | 3.6 V | X | 10 kHz | X | V |
| | $I_{IDLE194}$ | - | 136 | - | uA | 3.6 V | X | 10 kHz | X | X |

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| $V_{LDO}$=1.6 V | $I_{IDLE195}$ | - | 116 | - | uA | 2.2 V | X | 10 kHz | X | V |
| | $I_{IDLE196}$ | - | 114 | - | uA | 2.2 V | X | 10 kHz | X | X |
| Operating Current Idle Mode HCLK =2 MHz $V_{LDO}$=1.2 V | $I_{IDLE197}$ | - | 0.7 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | 4 MHz | X | X | V |
| | $I_{IDLE198}$ | - | 0.4 | - | mA | 3.6 V | 4 MHz | X | X | X |
| | $I_{IDLE199}$ | - | 0.7 | - | mA | 2.2 V | 4 MHz | X | X | V |
| | $I_{IDLE200}$ | - | 0.4 | - | mA | 2.2 V | 4 MHz | X | X | X |
| Operating Current Idle Mode HCLK =2 MHz $V_{LDO}$=1.2 V | $I_{IDLE201}$ | - | 0.7 | - | mA | $V_{DD}$ | HXT | MIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 4 MHz | X | V |
| | $I_{IDLE202}$ | - | 0.3 | - | mA | 3.6 V | X | 4 MHz | X | X |
| | $I_{IDLE203}$ | - | 0.7 | - | mA | 2.2 V | X | 4 MHz | X | V |
| | $I_{IDLE204}$ | - | 0.3 | - | mA | 2.2 V | X | 4 MHz | X | X |
| Operating Current Idle Mode HCLK =32.768 kHz $V_{LDO}$=1.2 V | $I_{IDLE205}$ | - | 215 | - | uA | $V_{DD}$ | LXT | LIRC | PLL | All digital module |
| | | | | | | 3.6 V | 32.768 kHz | X | X | V |
| | $I_{IDLE206}$ | - | 211 | - | uA | 3.6 V | 32.768 kHz | X | X | X |
| | $I_{IDLE207}$ | - | 204 | - | uA | 2.2 V | 32.768 kHz | X | X | V |
| | $I_{IDLE208}$ | - | 200 | - | uA | 2.2 V | 32.768 kHz | X | X | X |
| Operating Current Idle Mode HCLK =10 kHz $V_{LDO}$=1.2 V | $I_{IDLE209}$ | - | 122 | - | uA | $V_{DD}$ | LXT | LIRC | PLL | All digital module |
| | | | | | | 3.6 V | X | 10 kHz | X | V |
| | $I_{IDLE210}$ | - | 132 | - | uA | 3.6 V | X | 10 kHz | X | X |
| | $I_{IDLE211}$ | - | 112 | - | uA | 2.2 V | X | 10 kHz | X | V |
| | $I_{IDLE212}$ | - | 111 | - | uA | 2.2 V | X | 10 kHz | X | X |
| Standby Current Power-down Mode $V_{LDO}$=1.8 V | $I_{PWD1}$ | - | 1.7 | - | uA | $V_{DD}$ | HXT/HIRC/PLL | LXT(kHz) | RTC | RAM retention |
| | | | | | | 3.6 V | X | X | X | V |
| | $I_{PWD2}$ | - | 2.3 | - | uA | 3.6 V | X | 32.768 | V | V |
| | $I_{PWD3}$ | - | 1.6 | - | uA | 2.2 V | X | X | X | V |
| | $I_{PWD4}$ | - | 2.2 | - | uA | 2.2 V | X | 32.768 | V | V |
| Standby Current Power-down Mode $V_{LDO}$=1.6 V | $I_{PWD5}$ | - | 1.6 | - | uA | 3.6 V | X | X | X | V |
| | $I_{PWD6}$ | - | 2.2 | - | uA | 3.6 V | X | 32.768 | V | V |
| | $I_{PWD7}$ | - | 1.5 | - | uA | 2.2 V | X | X | X | V |
| | $I_{PWD8}$ | - | 2.1 | - | uA | 2.2 V | X | 32.768 | V | V |
| Standby Current | $I_{PWD9}$ | - | 1.6 | - | uA | 3.6 V | X | X | X | V |

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| Power-down Mode $V_{LDO}$=1.2 V | $I_{PWD10}$ | - | 2.1 | - | uA | 3.6 V | X | 32.768 | V | V |
| | $I_{PWD11}$ | - | 1.4 | - | uA | 2.2 V | X | X | X | V |
| | $I_{PWD12}$ | - | 2.0 | - | uA | 2.2 V | X | 32.768 | V | V |

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Input Pull Up Resistor PA, PB, PC, PD, PE, PF | $R_{IN}$ | - | 42 | - | KΩ | $V_{DD}$ = 3.3V |
| | | - | 106 | - | KΩ | $V_{DD}$ = 2.2V |
| Input Leakage Current PA, PB, PC, PD, PE, PF | $I_{LK}$ | -1 | - | 1 | µA | $V_{DD}$ = 3.3V, 0<$V_{IN}$<$V_{DD}$ |
| Input Low Voltage PA, PB, PC, PD, PE, PF (Schmitt input) | $V_{IL1}$ | - | - | $0.3*V_{DD}$ | V | |
| Input High Voltage PA, PB, PC, PD, PE, PF (Schmitt input) | $V_{IH1}$ | $0.7*V_{DD}$ | - | - | V | ADC/ACMP/HXT/LXT shared pins and PA.8/PB.4/PB.5 pins without Input 5V tolerance. |
| Hysteresis voltage of PA~PF (Schmitt input) | $V_{HY}$ | - | $0.4*V_{DD}$ | - | V | |
| Negative going threshold (Schmitt input), /RESET | $V_{ILS}$ | - | - | $0.3*V_{DD}$ | V | $V_{DD}$ = 3.3V |
| Positive going threshold (Schmitt Input), /RESET | $V_{IHS}$ | $0.7*V_{DD}$ | - | - | V | $V_{DD}$ = 3.3V |
| Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode) | $I_{SR21}$ | - | -18 | - | mA | $V_{DD}$ = 3.3V, $V_S$ = 2.4V |
| | $I_{SR22}$ | - | -2.5 | - | mA | $V_{DD}$ = 2.2V, $V_S$ = 1.6V |
| Sink Current PA, PB, PC, PD, PE, PF (Push-pull Mode) | $I_{SK21}$ | - | 12 | - | mA | $V_{DD}$ = 3.3V, $V_S$ = 0.45V |
| | $I_{SK22}$ | - | 6 | - | mA | $V_{DD}$ = 2.2V, $V_S$ = 0.45V |

**Note:**

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.
4. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device. Also a 100nF bypass capacitor between LDO and VSS help suppressing output noise.

5. All peripherals' clock source is from HXT (12 MHz), except SPI from HCLK.
6. The Operating Current (Normal Run Mode and Idle Mode) test condition is enable LVR and Clock filter.

## 9.3 AC Electrical Characteristics

### 9.3.1　External Input Clock

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Clock High Time | $t_{CHCX}$ | 10 | - | - | nS | |
| Clock Low Time | $t_{CLCX}$ | 10 | - | - | nS | |
| Clock Rise Time | $t_{CLCH}$ | 2 | - | 15 | nS | |
| Clock Fall Time | $t_{CHCL}$ | 2 | - | 15 | nS | |
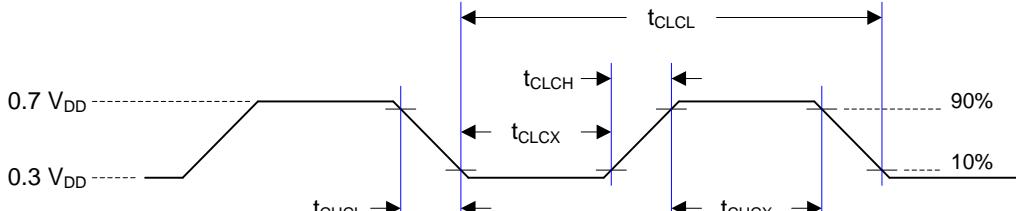
Note: Duty cycle is 50%.

### 9.3.2　External 4~24 MHz XTAL Oscillator

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Oscillator frequency | $f_{HXT}$ | 4 | 12 | 24 | MHz | VDD = 2.2V ~ 3.6V |
| Temperature | $T_{HXT}$ | -40 | - | +105 | °C | |
| Operating current | $I_{HXT}$ | - | 450 | - | uA | VDD = 3.3V |

*9.3.2.1　Typical Crystal Application Circuits*

| CRYSTAL | C1 | C2 | R1 |
|---|---|---|---|
| 4MHz ~ 24 MHz | 20pF | 20pF | without |
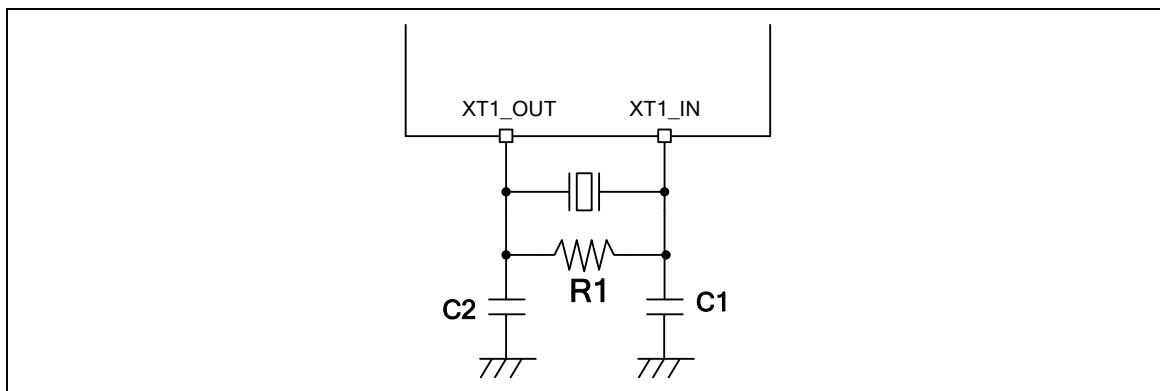
Figure 9‑1 Typical Crystal Application Circuit

### 9.3.3 External 32.768 kHz Crystal

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Oscillator frequency | $f_{LXT}$ | - | 32.768 | - | kHz | VDD = 2.2V ~ 3.6V |
| Temperature | $T_{LXT}$ | -40 | - | +105 | °C | |
| Operating current | $I_{LXT}$ | - | 1.42 | - | μA | VDD = 3.3V, Testing crystal ESR = 50kΩ |

**Note:** The 32.768 kHz crystal must fit the specifications for working in any situation normally.

1. Equivalent series resistance (ESR) of crystal should be less than 50 kΩ (max. 50 kΩ).

2. The load capacitance should be 12.5 pF.

3. The specifications based on crystal "XD36RU000032C9" from vendor Aurumtec.

#### 9.3.3.1 Typical Crystal Application Circuits

| CRYSTAL | C3 | C4 | R2 |
|---|---|---|---|
| 32.768 kHz | 20pF | 20pF | without |
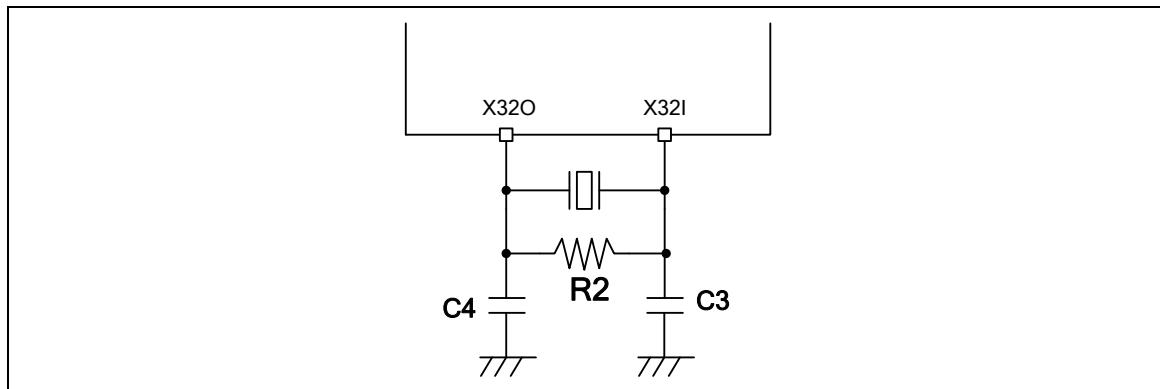


Figure 9‑2 Typical Crystal Application Circuit

### 9.3.4　Internal 36 MHz Oscillator

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Supply voltage[1] | $V_{HRC}$ | - | 1.5 | - | V | |
| Calibrated Internal Oscillator Frequency | $F_{HRC}$ | 35.64 | 36 | 36.36 | MHz | 25°C, VDD = 3.3V |
| | | 35.28 | 36 | 36.72 | MHz | -40°C ~ +105°C, VDD = 2.2V~3.6V |
| | | 35.64 | 36 | 35.36 | MHz | -40°C ~ +105 °C, VDD = 2.2V~3.6V<br><br>Enable 32.768K crystal oscillator and set TRIM_SEL[1:0]="10" |
| Operating current | $I_{HRC}$ | - | 85 | - | μA | |

### 9.3.5　Internal 12 MHz Oscillator

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Supply voltage[1] | $V_{HRC}$ | - | 1.8 | - | V | |
| Calibrated Internal Oscillator Frequency | $F_{HRC}$ | 11.88 | 12 | 12.12 | MHz | 25°C, VDD = 3.3V |
| | | 11.76 | 12 | 12.24 | MHz | -40°C ~ +105°C, VDD = 2.2V~3.6V |
| | | 11.88 | 12 | 12.12 | MHz | -40°C ~ +105 °C, VDD = 2.2V~3.6V<br><br>Enable 32.768K crystal oscillator and set TRIM_SEL[1:0]="10" |
| Operating current | $I_{HRC}$ | - | 210 | - | μA | |

Note: Internal oscillator operation voltage comes from LDO.

### 9.3.6 Internal 4 MHz Oscillator

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Supply voltage[1] | $V_{HRC}$ | - | 1.5 | - | V | |
| Calibrated Internal Oscillator Frequency | $F_{HRC}$ | 3.96 | 4 | 4.04 | MHz | 25°C, VDD = 3.3V |
| | | 3.88 | 4 | 4.08 | MHz | -40°C ~ +105°C, VDD = 2.2V~3.6V |
| | | 3.92 | 4 | 4.04 | MHz | -40°C ~ +105 °C, VDD = 2.2V~3.6V Enable 32.768K crystal oscillator and set TRIM_SEL[1:0]="10" |
| Operating current | $I_{HRC}$ | - | 20 | - | μA | |

### 9.3.7    Internal 10 kHz Oscillator

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Supply voltage[1] | $V_{LRC}$ | - | 1.8 | - | V | |
| Center Frequency | $F_{LRC}$ | 7 | 10 | 13 | kHz | 25°C, VDD = 3.3V |
| | | 5 | 10 | 15 | kHz | -40°C ~+105 °C, VDD = 2.2V~3.6V |
| Operating current | $I_{LRC}$ | - | 0.5 | - | μA | VDD = 3.3V |

Note: Internal oscillator operation voltage comes from LDO.

## 9.4 Analog Characteristics

### 9.4.1    12-bit ADC

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Operating voltage | $AV_{DD}$ | 2.2 | - | 3.6 | V | $AV_{DD} = V_{DD}$ |
| Operating current ($AV_{DD}$ current) (Enable ADC and disable all other analog modules) | $I_{ADC32}$ | - | 125 | - | μA | $AV_{DD} = V_{DD} = 3.6V$ ADC_VREF = $AV_{DD}$ ADC Clock Rate = 36 MHz |
| | $I_{ADC2}$ | - | 20 | - | μA | $AV_{DD} = V_{DD} = 3.6V$ ADC_VREF = $AV_{DD}$ ADC Clock Rate = 6 MHz |
| Resolution | $R_{ADC}$ | - | - | 12 | Bit | |
| Reference voltage | $V_{REF}$ | 2.2 | - | $A_{VDD}$ | V | |
| Reference input current (Avg.) | $I_{REF}$ | - | - | 1 | μA | |
| ADC input voltage | $V_{IN}$ | 0 | - | $V_{REF}$ | V | |
| Conversion time | $T_{CONV}$ | 1 | - | - | μS | |
| Conversion Rate | $F_{SPS}$ | - | - | 1.8M | Hz | $V_{DD} = 3.6V$ |
| Integral Non-Linearity Error | INL | - | ±1 | - | LSB | $V_{REF}$ is external Vref pin |
| Differential Non-Linearity | DNL | - | ±0.8 | - | LSB | $V_{REF}$ is external Vref pin |
| Gain error | $E_G$ | - | ±2 | - | LSB | $V_{REF}$ is external Vref pin |
| Offset error | $E_{OFFSET}$ | - | ±1.5 | - | LSB | $V_{REF}$ is external Vref pin |
| Absolute error | $E_{ABS}$ | - | - | ±6 | LSB | $V_{REF}$ is external Vref pin |
| ADC Clock frequency | $F_{ADC}$ | 0.25 | - | 36 | MHz | |
| Clock cycle | $AD_{CYC}$ | 20 | - | - | Cycle | |
| Internal Capacitance | $C_{IN}$ | - | 5 | - | pF | |
| Monotonic | - | Guaranteed | | | - | |

### 9.4.2 Brown-out Detector

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $AV_{DD}$ | Supply Voltage | 0 | - | 3.6 | V | - |
| $T_A$ | Temperature | -40 | 25 | 105 | ℃ | - |
| $I_{BOD}$ | Quiescent Current | - | 40 | - | µA | $AV_{DD}$ = 3.6V |
| $I_{LPBOD}$ | Quiescent Current | - | 0.5 | - | µA | $AV_{DD}$ = 3.6V |
| $V_{BOD}$ | Brown-out Voltage 25℃ | 1.75 | 1.8 | 1.79 | V | BODCTL[15:12] = 0001 |
| | | 1.84 | 1.9 | 1.89 | V | BODCTL[15:12] = 0010 |
| | | 1.94 | 2.0 | 1.99 | V | BODCTL[15:12] = 0011 |
| | | 2.04 | 2.1 | 2.09 | V | BODCTL[15:12] = 0100 |
| | | 2.14 | 2.2 | 2.19 | V | BODCTL[15:12] = 0101 |
| | | 2.23 | 2.3 | 2.29 | V | BODCTL[15:12] = 0110 |
| | | 2.33 | 2.4 | 2.39 | V | BODCTL[15:12] = 0111 |
| | | 2.43 | 2.5 | 2.49 | V | BODCTL[15:12] = 1000 |
| | | 2.53 | 2.6 | 2.59 | V | BODCTL[15:12] = 1001 |
| | | 2.62 | 2.7 | 2.69 | V | BODCTL[15:12] = 1010 |
| | | 2.72 | 2.8 | 2.79 | V | BODCTL[15:12] = 1011 |
| | | 2.82 | 2.9 | 2.89 | V | BODCTL[15:12] = 1100 |
| | | 2.92 | 3 | 2.99 | V | BODCTL[15:12] = 1101 |
| | | 3.02 | 3.1 | 3.09 | V | BODCTL[15:12] = 1110 |
| $V_{LPBOD}$ | Low Power Mode Brown-out Voltage 25℃ | 2.01 | 2.0 | 2.07 | V | BODCTL[9] = 0 |
| | | 2.42 | 2.5 | 2.79 | V | BODCTL[9] = 1 |

### 9.4.3 Power-on Reset

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|--------|-----------|-----|-----|-----|------|----------------|
| $T_A$ | Temperature | -40 | 25 | 105 | ℃ | - |
| $V_{POR}$ | Threshold Voltage | - | 1.5 | - | V | - |

### 9.4.4 Low-Voltage Reset

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|--------|-----------|-----|-----|-----|------|----------------|
| $T_A$ | Temperature | -40 | 25 | 105 | ℃ | - |
| $V_{POR}$ | Threshold Voltage | - | 1.68 | - | V | - |

### 9.4.5 Temperature Sensor

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITION (supply voltage = 3V) |
|-----------|------|------|------|------|------|----------------|
| | | MIN. | TYP. | MAX. | UNIT | |
| Detection Temperature | $T_{DET}$ | -40 | | +105 | $^{o}C$ | |
| Operating current | $I_{TEMP}$ | - | 5 | - | μA | |
| Gain | $V_{TG}$ | -1.64 | -1.70 | -1.76 | mV/$^{o}$C | |
| Offset | $V_{TO}$ | 735 | 745 | 755 | mV | Temperature at 0 $^{o}$C |

Note: Internal operation voltage comes from LDO.

### 9.4.6 Internal Voltage Reference

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Operating voltage | $AV_{DD}$ | 2.2 | - | 3.6 | V | |
| 1.5V voltage reference | $V_{REF1}$ | 1.43 | 1.5 | 1.58 | V | $AV_{DD} \geq 2.2V$ (-40°C ~105°C) |
| 1.8V voltage reference | $V_{REF2}$ | 1.71 | 1.8 | 1.89 | V | $AV_{DD} \geq 2.2V$ (-40°C ~105°C) |
| 2.5V voltage reference | $V_{REF3}$ | 2.37 | 2.5 | 2.63 | V | $AV_{DD} \geq 2.8V$ (-40°C ~105°C) |
| Stable Time | $T_{REFTAB}$ | - | 1 | - | ms | $I_{LOAD}$=1mA, C=1uF |
| 1.5V operating current | $I_{VREF1}$ | - | 125 | - | μA | $AV_{DD}$ = 3.3V |
| 1.8V operating current | $I_{VREF2}$ | - | 130 | - | μA | $AV_{DD}$ = 3.3V |
| 2.5V operating current | $I_{VREF3}$ | - | 140 | - | μA | $AV_{DD}$ = 3.3V |

### 9.4.7 Comparator

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $V_{CMP}$ | Supply Voltage | 2.2 | - | 3.6 | V | |
| $T_A$ | Temperature | -40 | 25 | 105 | ℃ | - |
| $I_{CMP}$ | Operation Current | - | 40 | - | μA | $AV_{DD}$ = 3.3 V |
| $V_{OFF}$ | Input Offset Voltage | - | 10 | TBD | mV | - |
| $V_{SW}$ | Output Swing | 0.1 | - | $AV_{DD}$ - 0.1 | V | - |
| $V_{COM}$ | Input Common Mode Range | 0.1 | - | $AV_{DD}$ – 0.1 | V | - |
| - | DC Gain | 40 | 70 | - | dB | - |
| $T_{PGD1}$ | Propagation Delay(HYS=0) | - | 280 | TBD | ns | $V_{DIFF}$ = 100mV, |
| $T_{PGD2}$ | Propagation Delay(HYS=1) | - | 440 | TBD | us | $V_{DIFF}$ = 100mV |
| $V_{HYS}$ | Hysteresis | - | ±60 | - | mV | |
| $T_{STB}$ | Stable time | - | 1 | TBD | μs | |

## 10  PACKAGE DIMENSIONS

### 10.1    64S LQFP (7x7x1.4 mm footprint 2.0 mm)
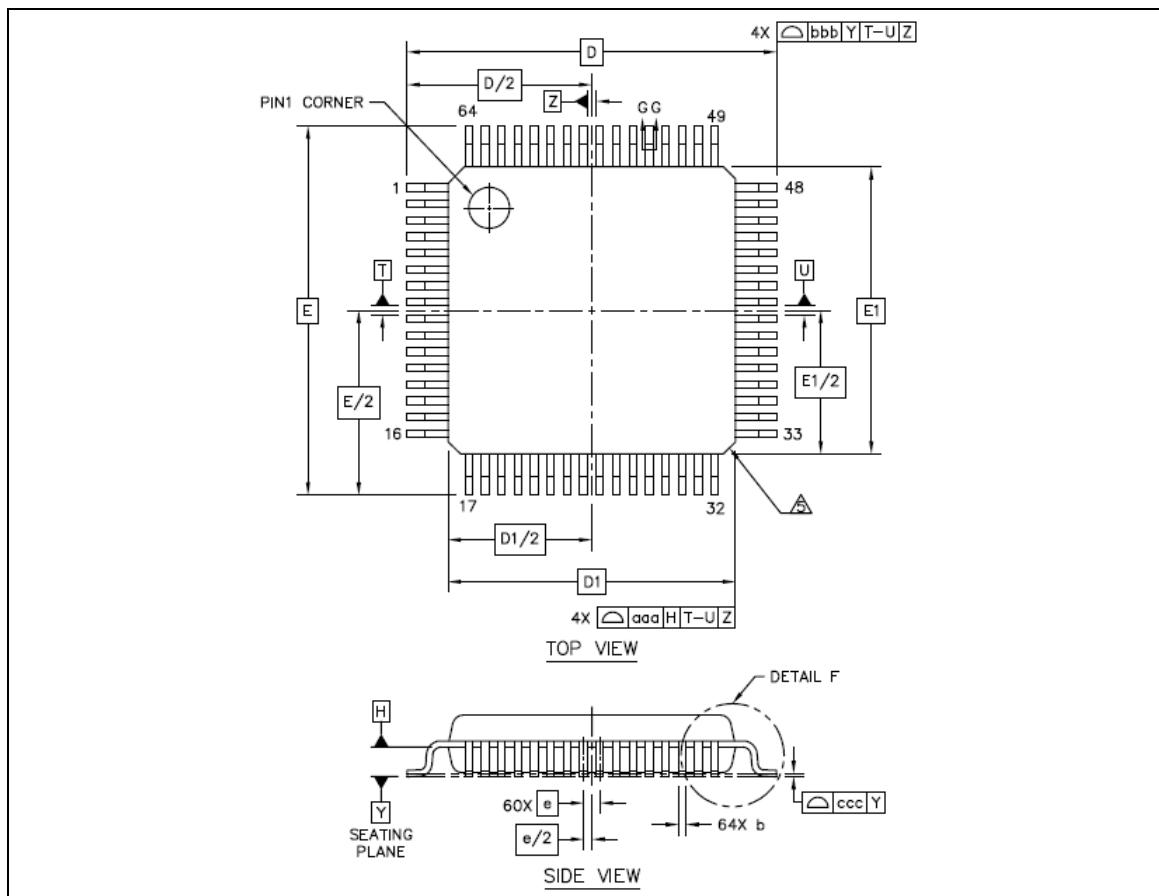
| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | --- | --- | 1.6 |
| STAND OFF | | A1 | 0.05 | --- | 0.15 |
| MOLD THICKNESS | | A2 | 1.35 | 1.4 | 1.45 |
| LEAD WIDTH(PLATING) | | b | 0.13 | 0.18 | 0.23 |
| LEAD WIDTH | | b1 | 0.13 | 0.16 | 0.19 |
| L/F THICKNESS(PLATING) | | c | 0.09 | --- | 0.2 |
| L/F THICKNESS | | c1 | 0.09 | --- | 0.16 |
| BODY SIZE | X | D | 9 BSC | | |
| | Y | E | 9 BSC | | |
| | X | D1 | 7 BSC | | |
| | Y | E1 | 7 BSC | | |
| LEAD PITCH | | e | 0.4 BSC | | |
| | | L | 0.45 | 0.6 | 0.75 |
| FOOTPRINT | | L1 | 1 REF | | |
| | | θ | 0° | 3.5° | 7° |
| | | θ1 | 0° | --- | --- |
| | | θ2 | 11° | 12° | 13° |
| | | θ3 | 11° | 12° | 13° |
| | | R1 | 0.08 | --- | --- |
| | | R2 | 0.08 | --- | 0.2 |
| | | S | 0.2 | --- | --- |
| PACKAGE EDGE TOLERANCE | | aaa | 0.2 | | |
| LEAD EDGE TOLERANCE | | bbb | 0.2 | | |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.07 | | |
| MOLD FLATNESS | | eee | 0.05 | | |
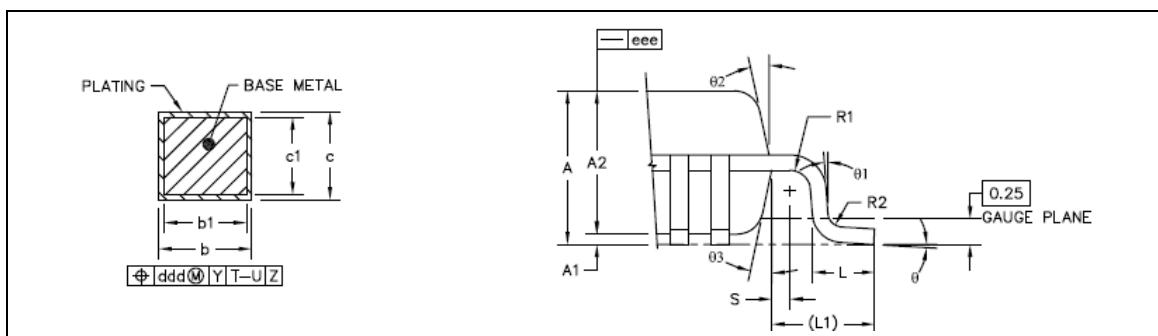
## 10.2  48L LQFP (7x7x1.4 mm footprint 2.0 mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN | NOM. | MAX. | MIN | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D1 | 6.90 | 7.00 | 7.10 | 0.272 | 0.276 | 0.260 |
| E1 | 6.90 | 7.00 | 7.10 | 0.272 | 0.276 | 0.260 |
| e | 0.35 | 0.50 | 0.65 | 0.014 | 0.020 | 0.260 |
| D | 8.9 | 9.00 | 9.10 | 0.350 | 0.354 | 0.358 |
| E | 8.9 | 9.00 | 9.10 | 0.350 | 0.354 | 0.358 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | — | 1.00 | — | — | 0.039 | — |
| C | 0.09 | — | 0.20 | 0.0035 | — | 0.0079 |
| θ | 0° | — | 7° | 0° | — | 7° |
| b | 0.17 | 0.22 | 0.27 | 0.007 | 0.0087 | 0.011 |
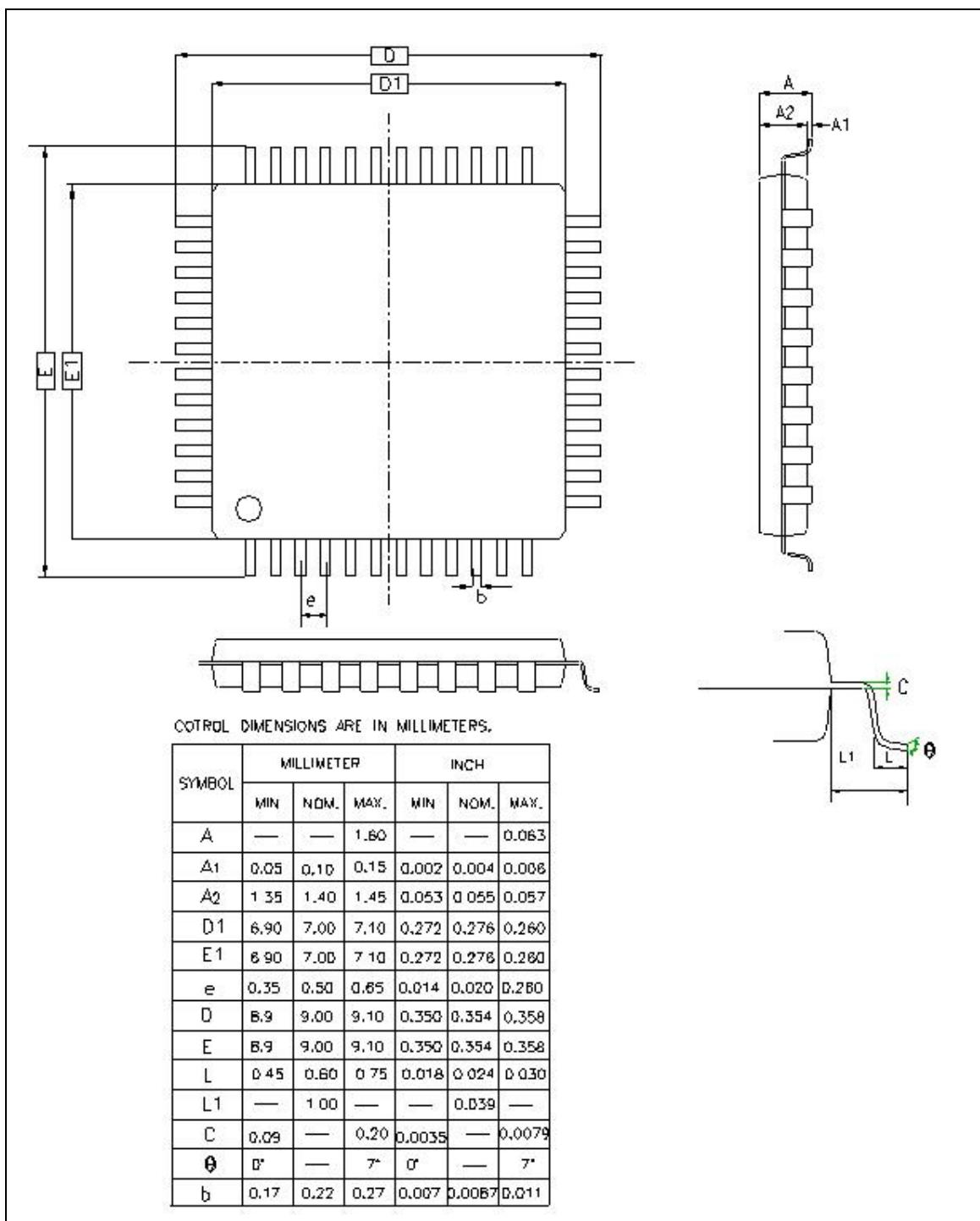
## 10.3    33L QFN (5x5x1.4 mm footprint 2.0 mm)
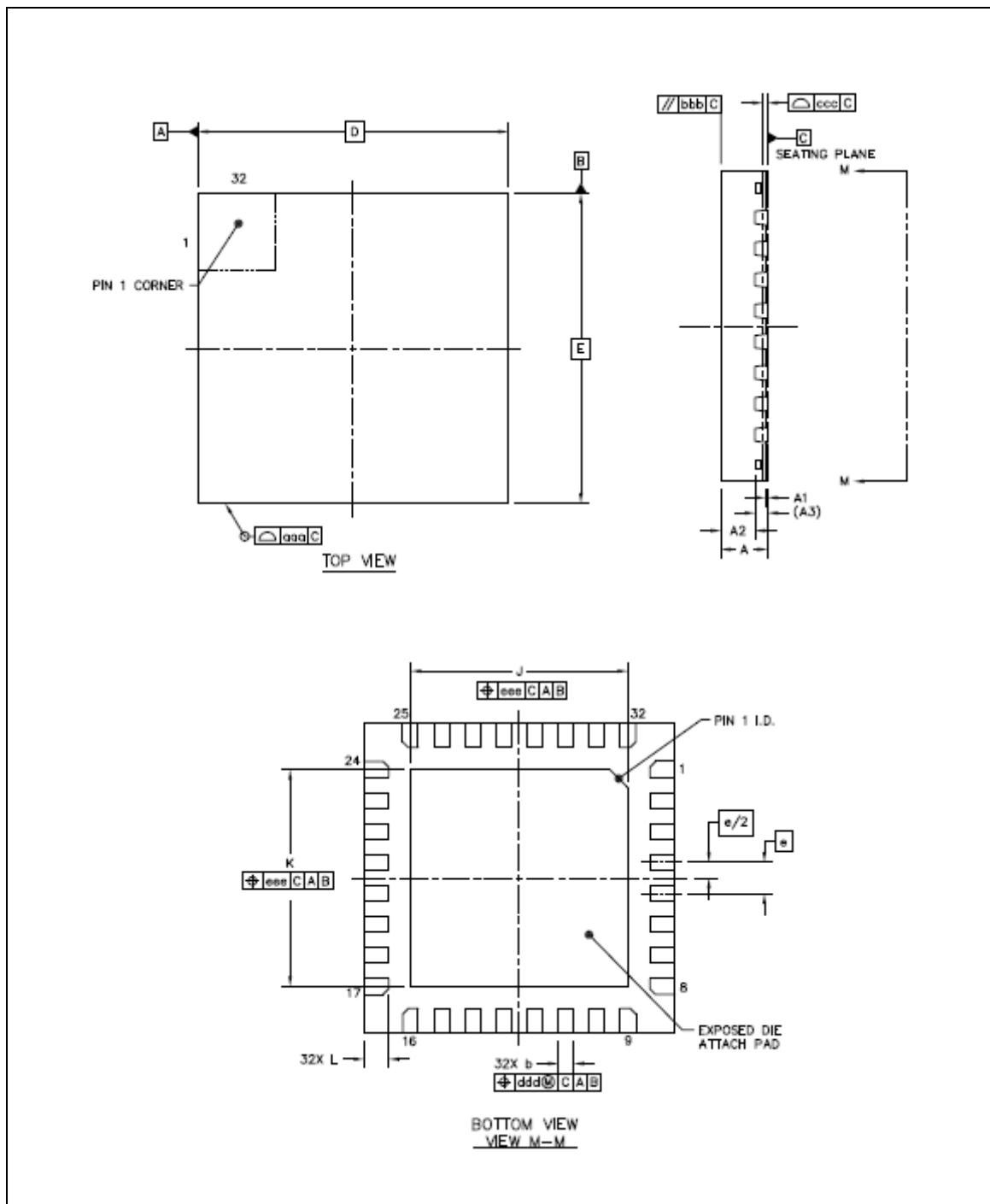
| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.7 | 0.75 | 0.8 |
| STAND OFF | | A1 | 0 | 0.035 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.55 | 0.57 |
| L/F THICKNESS | | A3 | 0.203 REF | | |
| LEAD WIDTH | | b | 0.2 | 0.25 | 0.3 |
| BODY SIZE | X | D | 5 BSC | | |
| | Y | E | 5 BSC | | |
| LEAD PITCH | | e | 0.5 BSC | | |
| EP SIZE | X | J | 3.4 | 3.5 | 3.6 |
| | Y | K | 3.4 | 3.5 | 3.6 |
| LEAD LENGTH | | L | 0.35 | 0.4 | 0.45 |
| PACKAGE EDGE TOLERANCE | | aaa | 0.1 | | |
| MOLD FLATNESS | | bbb | 0.1 | | |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.1 | | |
| EXPOSED PAD OFFSET | | eee | 0.1 | | |

# 11 REVISION HISTORY

| Date | Revision | Description |
|------|----------|-------------|
| 2016.07.01 | 1.00 | Initial version |
| 2018.05.02 | 1.01 | 1. Revised Temperature Selection Code in section 4.1.<br>2. Revised UART channel number in section 4.2.<br>3. Revised I/O ports number in section 5.1.<br>4. Revised Supply Voltage Range in chapter 1, chapter 2, section 6.5 and chapter 9.<br>5. Removed invalid cross-references in section 6.8.1.<br>6. Revised external 32.768 kHz crystal characteristics in section 9.3.3.<br>7. Removed SPROM and KPROM discription in chapter 1, chapter 2, section 5.1 and section 6.4. |

NANO103 SERIES DATASHEET

## Important Notice

**Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".**

**Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.**

**All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.**