

# NCV8660

## Very Low $I_q$ LDO 150 mA Regulator with RESET and Delay Time Select

The NCV8660 is a precision very low  $I_q$  low dropout voltage regulator. Quiescent currents as low as 28  $\mu\text{A}$  typical make it ideal for automotive applications requiring low quiescent current with or without a load. Integrated control features such as Reset and Delay Time Select make it ideal for powering microprocessors.

It is available with a fixed output voltage of 5.0 V and 3.3 V and regulates within  $\pm 2.0\%$ .

### Features

- Fixed Output Voltage of 5 V and 3.3 V
- $\pm 2.0\%$  Output Voltage up to  $V_{\text{BAT}} = 40\text{ V}$
- Output Current up to 150 mA
- Microprocessor Compatible Control Functions:
  - ◆ Delay Time Select
  - ◆ RESET Output
- NCV Prefix for Automotive
  - ◆ Site and Change Control
  - ◆ AEC-Q100 Qualified
- Low Dropout Voltage
- Low Quiescent Current of 28  $\mu\text{A}$  Typical
- Stable Under No Load Conditions
- Protection Features:
  - ◆ Thermal Shutdown
  - ◆ Short Circuit
- These are Pb-Free Devices

### Applications

- Automotive:
  - ◆ Body Control Module
  - ◆ Instrument and Clusters
  - ◆ Occupant Protection and Comfort
  - ◆ Powertrain
- Battery Powered Consumer Electronics

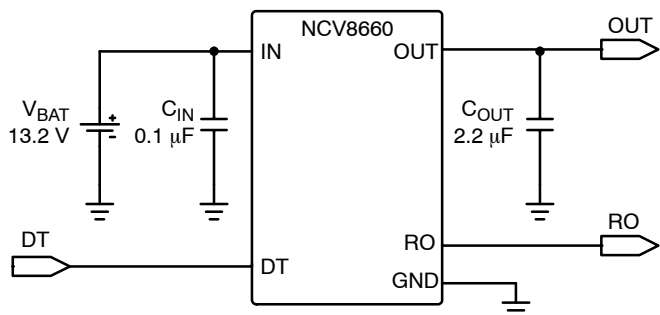


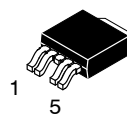
Figure 1. Application Diagram



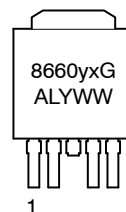
ON Semiconductor®

<http://onsemi.com>

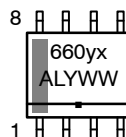
### MARKING DIAGRAMS



DPAK 5-PIN  
DT SUFFIX  
CASE 175AA



SOIC-8 FUSED  
CASE 751



- x = 5 for 5 V Output, 3 for 3.3 V Output
- y = 1 for 8 ms, 128 ms Reset Delay,  
= 3 for 16 ms, 64 ms Reset Delay
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G or ■ = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 12 of this data sheet.

# NCV8660

## PIN DESCRIPTIONS

Pin		Symbol	Function
DPAK	SOIC-8 FUSED		
1	1	IN	Input Supply Voltage. 0.1 $\mu$ F bypass capacitor to GND at the IC.
2	2	RO	Reset Output. CMOS compatible output. Goes low when $V_{OUT}$ drops by more than 7% from nominal.
3, Tab	5-8	GND	Ground
4	3	DT	Reset Delay Time Select. Short to GND or connect to OUT to select time.
5	4	OUT	Regulated Voltage Output. 2.2 $\mu$ F to ground for typical applications.

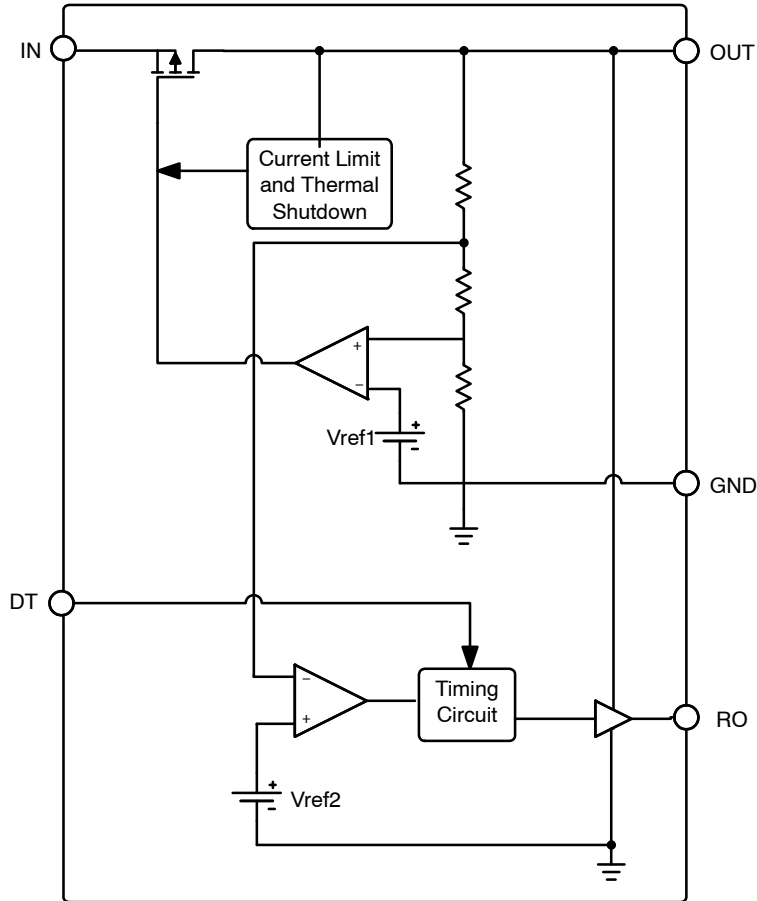


Figure 2. Block Diagram

**ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Min	Max	Unit
Input Voltage (IN)	$V_{IN}$	-0.3	40	V
Input Current	$I_{IN}$	-1.0	-	mA
Output Voltage (OUT) DC Transient, $t < 10$ s (Note 1)	$V_{OUT}$	-0.3 -0.3	5.5 16	V
Output Current (OUT)	$I_{OUT}$	-1.0	Current Limited	mA
Storage Temperature Range	$T_{STG}$	-55	150	°C
DT (Reset Delay Time Select) Voltage (Note 2)	$V_{DT}$	-0.3	16	V
DT (Reset Delay Time Select) Current (Note 2)	$I_{DT}$	-1.0	1.0	mA
RO (Reset Output) Voltage DC Transient, $t < 10$ s	$V_{RO}$	-0.3 -0.3	5.5 16	V
RO (Reset Output) Current	$I_{RO}$	-1.0	1.0	mA

**ESD CAPABILITY**

ESD Capability, Human Body Model (Note 3)	$ESD_{HB}$	-2.0	2.0	kV
ESD Capability, Machine Model (Note 3)	$ESD_{MM}$	-200	200	V
ESD Capability, Charged Device Model (Note 3)	$ESD_{CDM}$	-1.0	1.0	kV

**THERMAL RESISTANCE**

Junction-to-Case (Note 4)	DPAK 5	$R_{\theta JC}$	15	°C/W
Junction-to-Ambient (Note 4)	DPAK 5	$R_{\theta JA}$	66	°C/W
Junction-to-Tab (Note 4)	DPAK 5	$R_{\theta JT}$	4.0	°C/W
Junction-to-Ambient (Note 4)	SOIC-8 FUSED	$R_{\theta JA}$	104	°C/W
Junction-to-Lead (pin 6) (Note 4)	SOIC-8 FUSED	$R_{\theta JT}$	33	°C/W

**LEAD SOLDERING TEMPERATURE AND MSL**

Moisture Sensitivity Level	DPAK 5 SOIC-8 FUSED	MSL	1 3	-
Lead Temperature Soldering: SMD style only, Reflow (Note 5) Pb-Free Part 60 - 150 sec above 217°C, 40 sec max at peak		SLD	-	265 peak °C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- The output voltage must not exceed the input voltage.
- External resistor required to minimize current to less than 1 mA when the control voltage is above 16 V.
- This device series incorporates ESD protection and is tested by the following methods:  
ESD HBM tested per AEC-Q100-002 (EIA/JESD22-A114)  
ESD MM tested per AEC-Q100-003 (EIA/JESD22-A115)  
ESD CDM tested per EIA/JESD22/C101, Field Induced Charge Model
- Values represented typical steady-state thermal performance on 1 oz. copper FR4 PCB with 1 in<sup>2</sup> copper area.
- Per IPC / JEDEC J-STD-020C.

**OPERATING RANGE**

Pin Symbol, Parameter	Symbol	Min	Max	Unit
$V_{IN}$ , Input Voltage Operating Range	$V_{IN}$	4.5	40	V
Junction Temperature Range	$T_J$	-40	150	°C

# NCV8660

## ELECTRICAL CHARACTERISTICS $5.5\text{ V} < V_{IN} < 40\text{ V}$ , $-40^{\circ}\text{C} \leq T_J \leq +150^{\circ}\text{C}$ , unless otherwise specified

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
<b>GENERAL</b>						
Quiescent Current	$I_q$	$100\mu\text{A} < I_{OUT} < 150\text{mA}$ , $V_{IN} = 13.2\text{V}$ , $T_J = 25^{\circ}\text{C}$	-	25	30	$\mu\text{A}$
		$100\mu\text{A} < I_{OUT} < 150\text{mA}$ , $V_{IN} = 13.2\text{V}$ , $T_J \leq 85^{\circ}\text{C}$	-	-	40	
Thermal Shutdown (Note 6)	$T_{SD}$		150	175	195	$^{\circ}\text{C}$
Thermal Hysteresis (Note 6)	$T_{HYS}$		-	25	-	$^{\circ}\text{C}$

### OUT

Output Voltage	$V_{OUT}$	$6\text{ V} \leq V_{IN} \leq 16\text{ V}$ , $0.1\text{ mA} \leq I_{OUT} \leq 150\text{ mA}$	4.9	5.0	5.1	V
		$6\text{ V} \leq V_{IN} \leq 40\text{ V}$ , $0.1\text{ mA} \leq I_{OUT} \leq 100\text{ mA}$	4.9	5.0	5.1	
		$5.6\text{ V} \leq V_{IN} \leq 16\text{ V}$ , $0\text{ mA} \leq I_{OUT} \leq 150\text{ mA}$ , $-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$	4.9	5.0	5.1	
Output Voltage	$V_{OUT}$	$5.5\text{ V} \leq V_{IN} \leq 16\text{ V}$ , $0.1\text{ mA} \leq I_{OUT} \leq 150\text{ mA}$	3.234	3.3	3.366	V
		$5.5\text{ V} \leq V_{IN} \leq 40\text{ V}$ , $0.1\text{ mA} \leq I_{OUT} \leq 100\text{ mA}$	3.234	3.3	3.366	
Output Current Limit	$I_{CL}$	$I_{OUT} = 96\% \times V_{OUT}$ nominal	205	-	525	mA
Output Current Limit, Short Circuit	$I_{SCKT}$	$I_{OUT} = 0\text{ V}$	205	-	525	mA
Load Regulation	$\Delta V_{OUT}$	$V_{IN} = 13.2\text{ V}$ , $I_{OUT} = 0.1\text{ mA}$ to $150\text{ mA}$	-40	10	40	mV
Line Regulation	$\Delta V_{OUT}$	$I_{OUT} = 5\text{ mA}$ , $V_{IN} = 6\text{ V}$ to $28\text{ V}$	-20	0	20	mV
Dropout Voltage – 5.0 V Only	$V_{DR}$	$I_{OUT} = 100\text{ mA}$ , (Note 7) $V_{DR} = V_{IN} - V_{OUT}$ , ( $\Delta V_{OUT} = -100\text{ mV}$ )	-	0.225	0.45	V
		$I_{OUT} = 150\text{ mA}$ , (Note 7) $V_{DR} = V_{IN} - V_{OUT}$ , ( $\Delta V_{OUT} = -100\text{ mV}$ )	-	0.30	0.60	
Output Load Capacitance	$C_O$	Output capacitance for stability	2.2	-	-	$\mu\text{F}$
Power Supply Ripple Rejection	PSRR	$V_{IN} = 13.2\text{ V}$ , $0.5 V_{PP}$ , $100\text{ Hz}$	-	60	-	dB

### DT (Reset Delay Time Select)

Threshold Voltage	High		2	-	-	V
	Low		-	-	0.8	V
Input Current		$DT = 5\text{ V}$	-	-	1.0	$\mu\text{A}$

### RO, Reset Output

RESET Threshold	$V_{Rf}$	$V_{OUT}$ decreasing	90	93	96	$\%V_{OUT}$
RESET Threshold Hysteresis	$V_{Rhys}$		-	2.0	-	$\%V_{OUT}$
RO Output Low	$V_{RL}$	$10\text{ k}\Omega$ RESET to OUT, $V_{OUT} = 4.5\text{ V}$	-	0.2	0.4	V
RO Output High (OUT-RO)	$V_{RH}$	$10\text{ k}\Omega$ RESET to GND	$V_{OUT} - 0.4$	$V_{OUT} - 0.2$	$V_{OUT}$	V
Reset Reaction Time	$t_{RR}$	$V_{OUT}$ into UV to RESET Low	16	25	38	$\mu\text{sec}$
Input Voltage Reset Threshold	$V_{IN\_RT}$	$V_{IN}$ Decreasing, $V_{OUT} > V_{RT}$	-	3.8	4.25	V

### RESET Delay with DT Selection

Delay Time Out of RESET - 8 ms version - 16 ms version - 32 ms version - 64 ms version - 128 ms version	$t_{dRx}$	$V_{OUT}$ into regulation to RO High	5.0	8.0	11.5	msec
			10	16	23	
			20	32	46	
			40	64	92	
			80	128	184	

6. Not production tested, guaranteed by design.

7. Dropout at a given current level is defined as the voltage difference of  $V_{IN}$  to  $V_{OUT}$  with  $V_{IN}$  decreasing until the output drops by 100 mV.

TYPICAL OPERATING CHARACTERISTICS

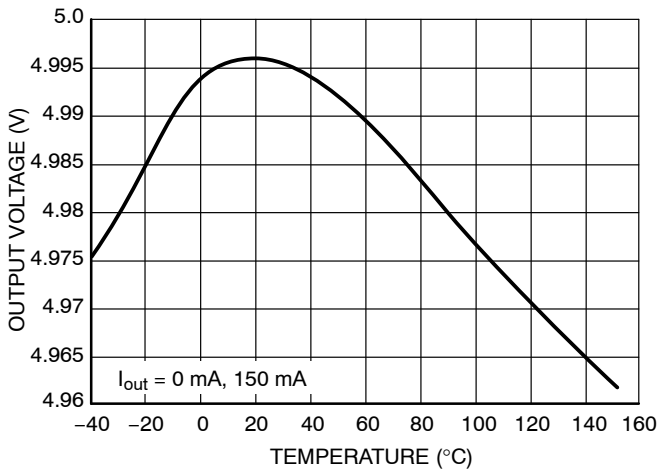


Figure 3. Output Voltage vs. Temperature (OUT = 5 V)

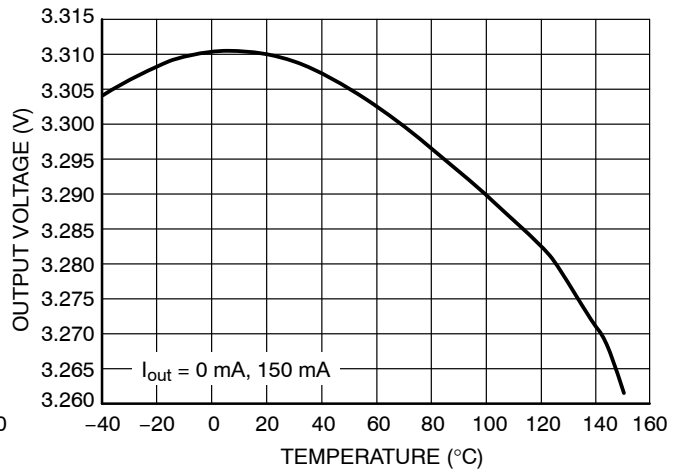


Figure 4. Output Voltage vs. Temperature (OUT = 3.3 V)

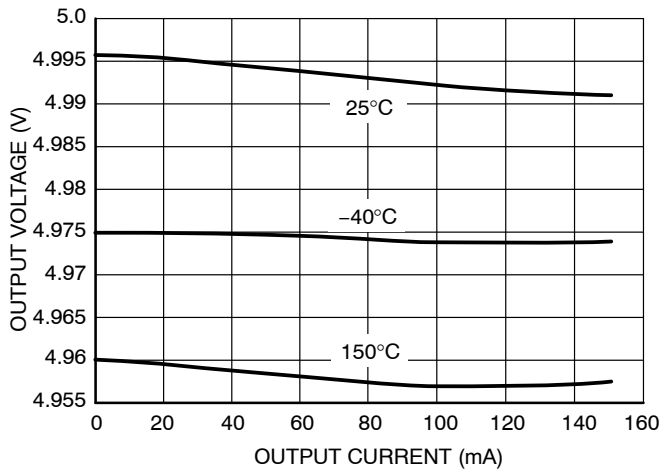


Figure 5. Output Voltage vs. Output Current (OUT = 5 V)

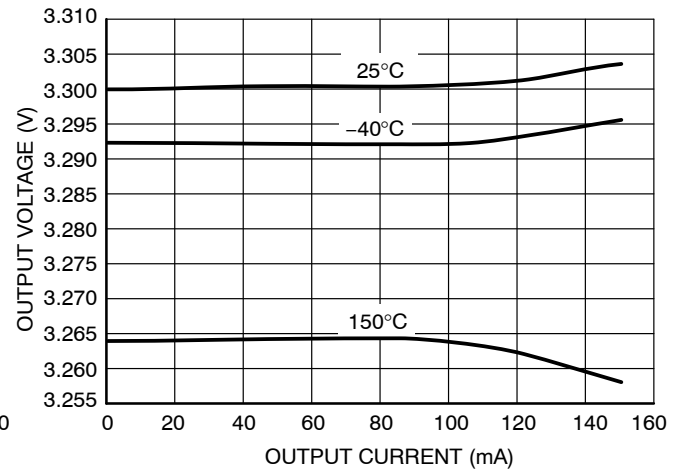


Figure 6. Output Voltage vs. Output Current (OUT = 3.3 V)

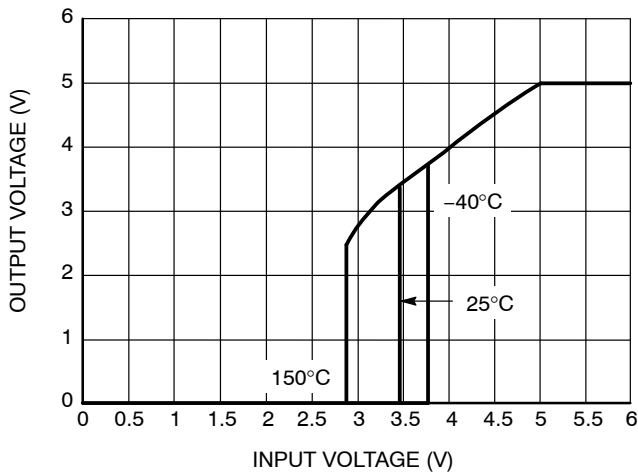


Figure 7. Output Voltage vs. Input Voltage (R<sub>LOAD</sub> = 51 k, I<sub>out</sub> = 100 μA, OUT = 5 V)

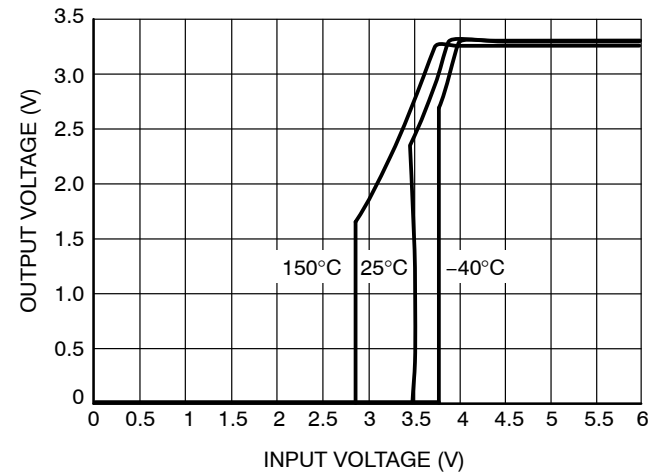


Figure 8. Output Voltage vs. Input Voltage (R<sub>LOAD</sub> = 51 k, I<sub>out</sub> = 100 μA, OUT = 3.3 V)

TYPICAL OPERATING CHARACTERISTICS

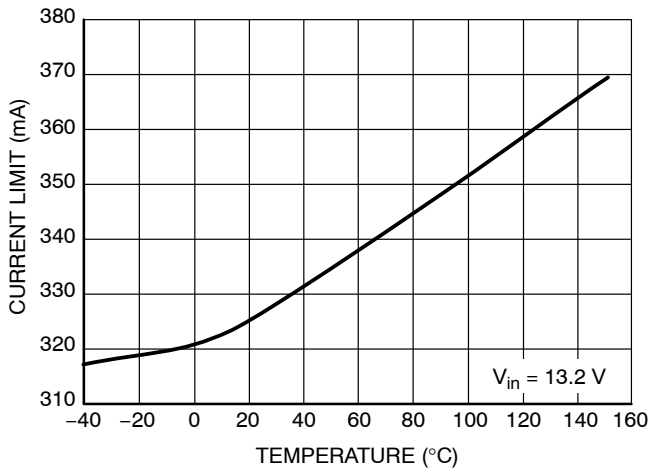


Figure 9. Current Limit vs. Temperature

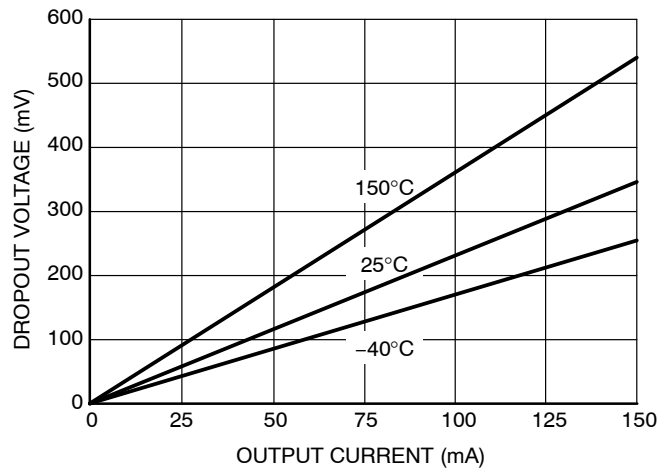


Figure 10. Dropout Voltage vs. Output Current

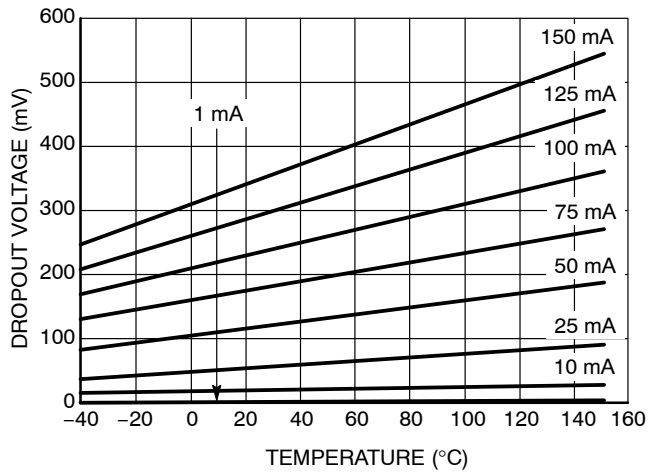


Figure 11. Dropout Voltage vs. Temperature

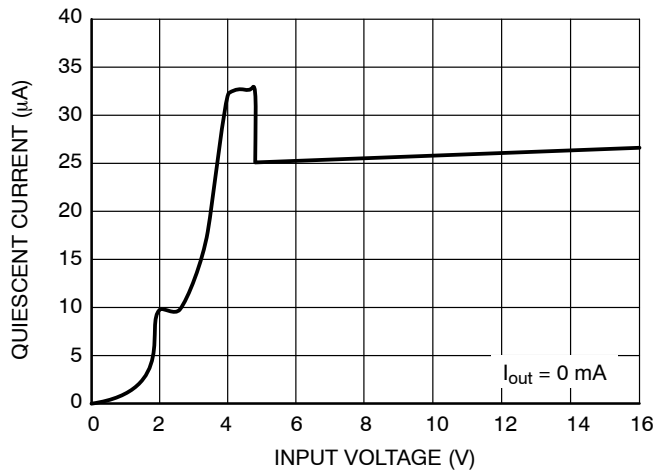


Figure 12. Quiescent Current vs. Input Voltage

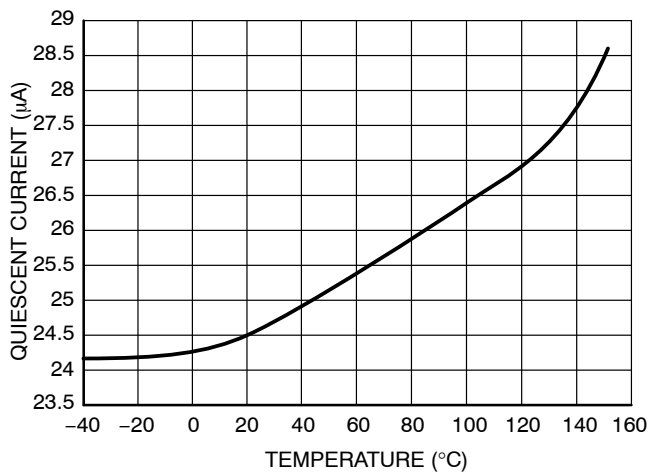


Figure 13. Quiescent Current vs. Temperature

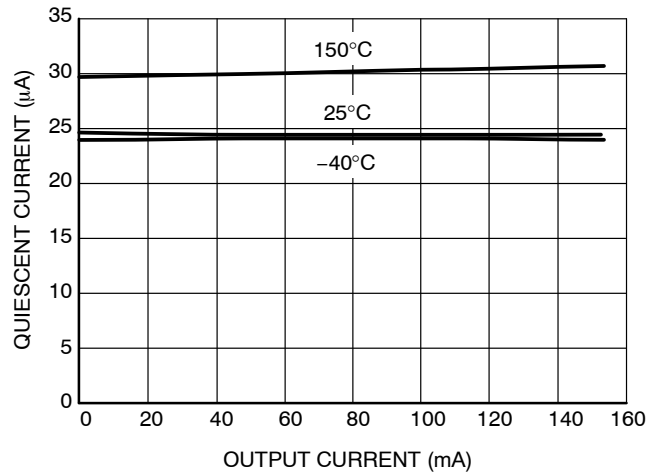


Figure 14. Quiescent Current vs. Output Current

TYPICAL OPERATING CHARACTERISTICS

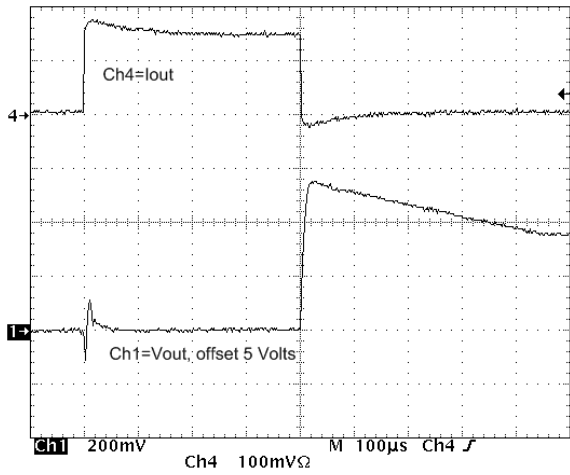


Figure 15. Load Transient  
( $V_{IN} = 13.2\text{ V}$ ,  $OUT = 5\text{ V}$ )

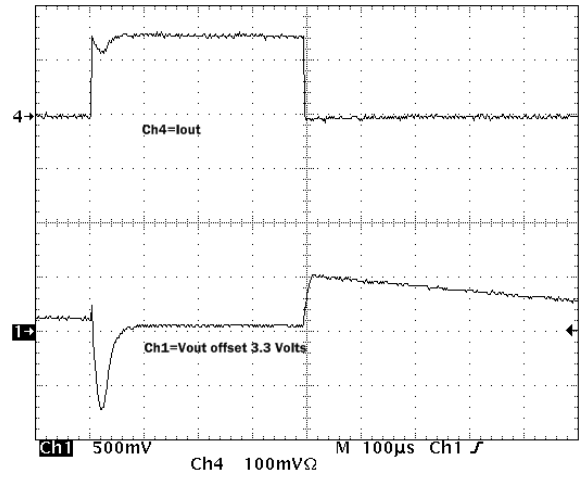


Figure 17. Load Transient  
( $V_{IN} = 13.2\text{ V}$ ,  $OUT = 3.3\text{ V}$ )

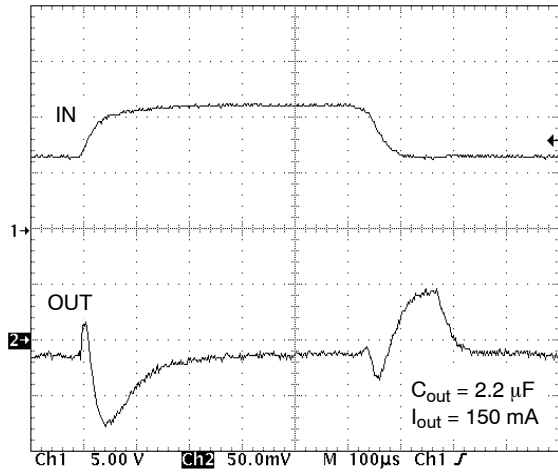


Figure 16. Line Transient ( $OUT = 5\text{ V}$ )

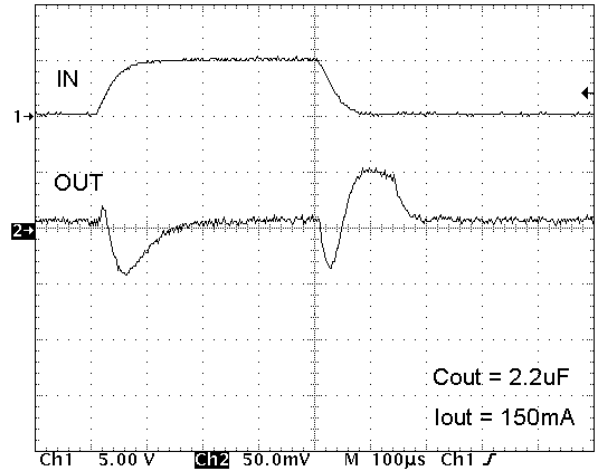


Figure 18. Line Transient ( $OUT = 3.3\text{ V}$ )

TYPICAL OPERATING CHARACTERISTICS

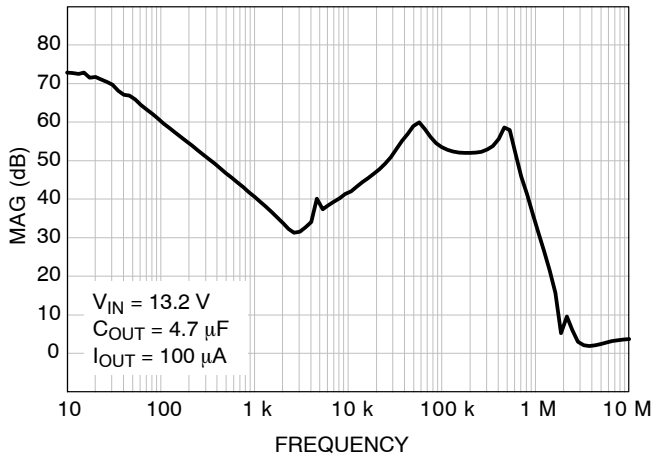


Figure 19. Ripple Rejection vs. Frequency  
( $V_{IN} = 13.2\text{ V}$ ,  $I_{OUT} = 100\ \mu\text{A}$ )

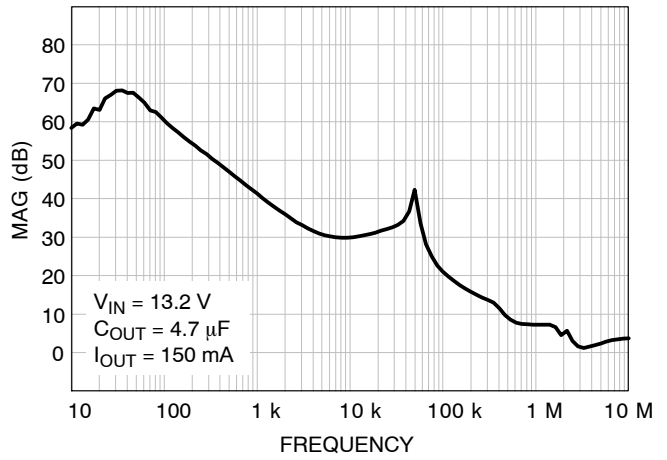


Figure 20. Ripple Rejection vs. Frequency  
( $V_{IN} = 13.2\text{ V}$ ,  $I_{OUT} = 150\text{ mA}$ )

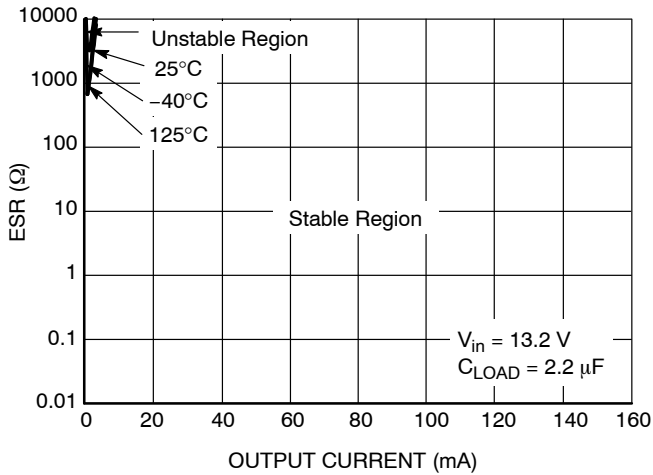


Figure 21. Output Capacitor ESR vs. Output Current (OUT = 5 V)

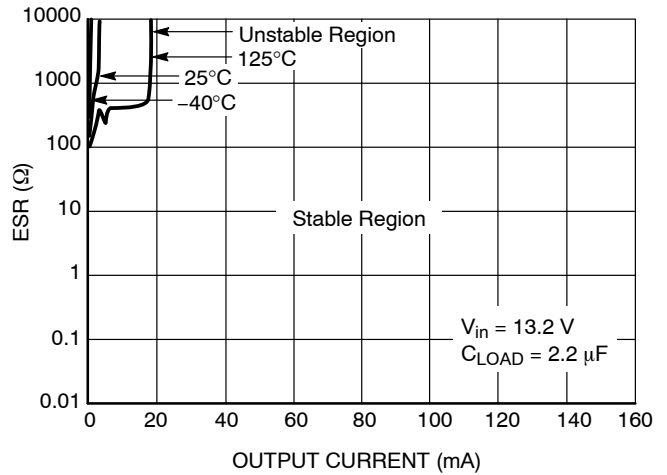


Figure 22. Output Capacitor ESR vs. Output Current (OUT = 3.3 V)

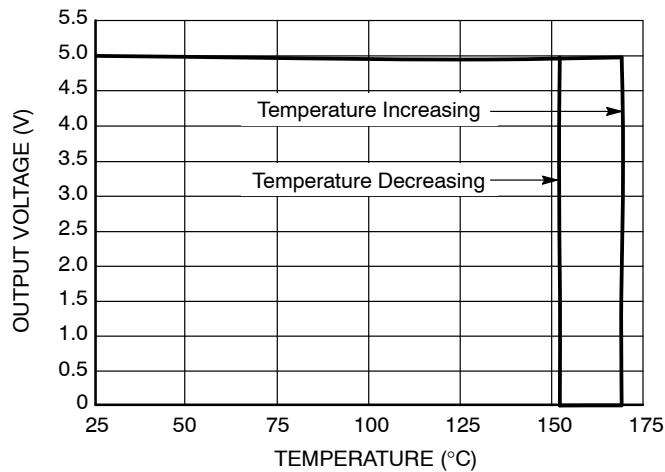


Figure 23. Thermal Shutdown vs. Temperature



DETAILED OPERATING DESCRIPTION

**General**

The NCV8660 is a 5 V and 3.3 V linear regulator providing low drop-out voltage for 150 mA at low quiescent current levels. Also featured in this part is a reset output with selectable delay times. Delay times are selectable via part selection and control through the Delay Time Select (DT) pin. No pull-up resistor is needed on the reset output (RO). Pull-up and pull-down capability are included. Only a small bypass capacitor on the input (IN) supply pin and output (OUT) voltage pin are required for normal operation. Thermal shutdown functionality protects the IC from damage caused from excessively high temperatures appearing on the IC.

**Output Voltage**

Output stability is determined by the capacitor selected from OUT to GND. The NCV8660 has been designed to work with low ESR (equivalent series resistance) ceramic capacitors. The device is extremely stable using virtually any capacitor 2.2  $\mu$ F and above. Reference the Output Capacitor Stability graph in Figure 21.

The output capacitor value will affect overshoot during power-up. A lower value capacitor will cause higher overshoot on the output. System evaluation should be performed with minimum loading for evaluation of overshoot.

Selection of process technology for the NCV8660 allows for low quiescent current independent of loading. Quiescent current will remain flat across the entire range of loads providing a low quiescent current condition in standby and under heavy loads. This is highly beneficial to systems requiring microprocessor interrupts during standby mode as duty cycle and load changes have no impact on the standby current. Reference Figure 14 for Quiescent Current vs Output Current.

**Current Limit**

Current limit is provided on OUT to protect the IC. The minimum specification is 205 mA. Current limit is specified under two conditions ( $OUT = 96\% \times OUT \text{ nominal}$ ) and ( $OUT = 0 \text{ V}$ ). No fold-back circuitry exists. Any measured differences can be attributed to change in die temperature. The part may be operated up to 205 mA provided thermal die temperature is considered and is kept below 150°C. Degradation of electrical parameters at this current is expected at these elevated levels. A reset (RO) will not occur with a load less than 205 mA.

**Reset Output**

A reset signal is provided on the Reset Output (RO) pin to provide feedback to the microprocessor of an out of regulation condition. This is in the form of a logic signal on RO. Output (OUT) voltage conditions below the RESET threshold cause RO to go low. The RO integrity is maintained down to  $OUT = 1.0 \text{ V}$ .

The Reset Output (RO) circuitry includes an active internal pullup to the output (OUT) as shown in Figure 24. No external pullup is necessary.

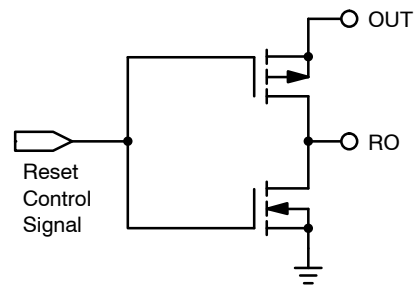
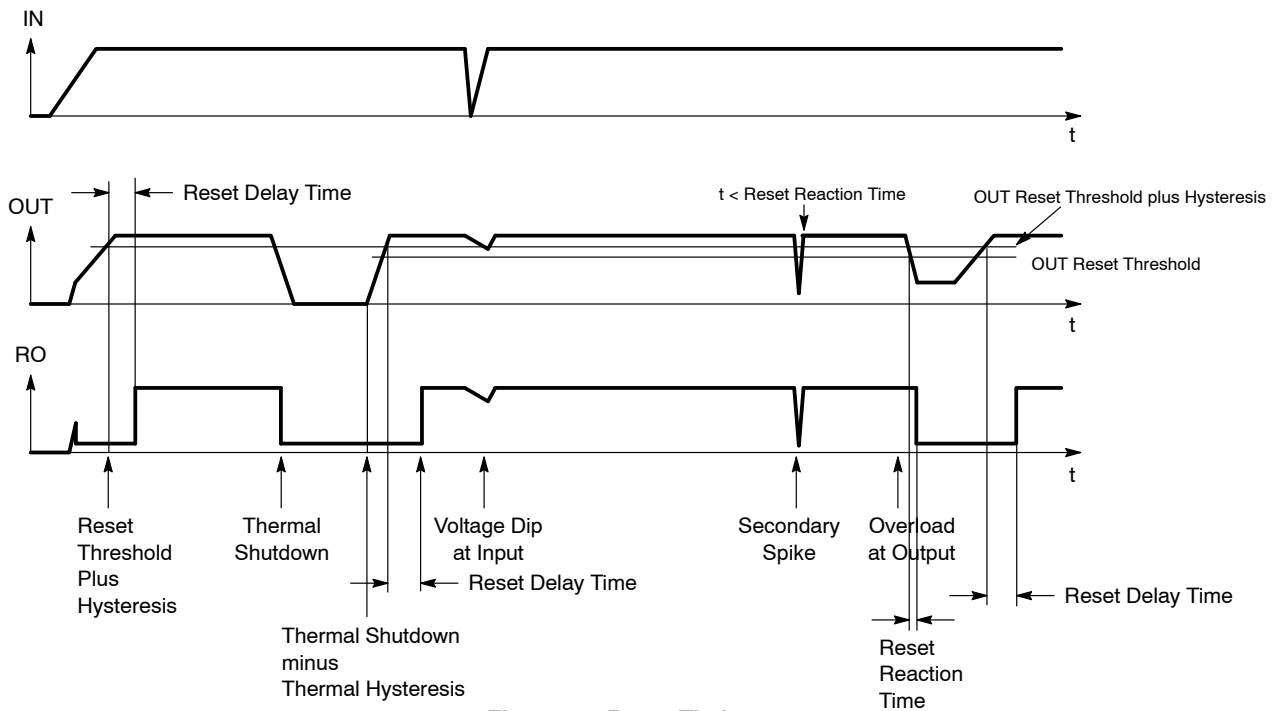


Figure 24. Reset Output Circuitry

# NCV8660



**Figure 25. Reset Timing**

During power-up (or restoring OUT voltage from a reset event), the OUT voltage must be maintained above the Reset threshold for the Reset Delay time before RO goes high. The time for Reset Delay is determined by the choice of IC and the state of the DT pin.

### Reset Delay Time Select

Selection of the NCV8660 device and the state of the DT pin determines the available Reset Delay times. The part is designed for use with DT tied to ground or OUT, but may be controlled by any logic signal which provides a threshold between 0.8 V and 2 V. The default condition for an open DT pin is the slower Reset time (DT = GND condition). Times are in pairs and are highlighted in the chart below. Consult factory for availability.

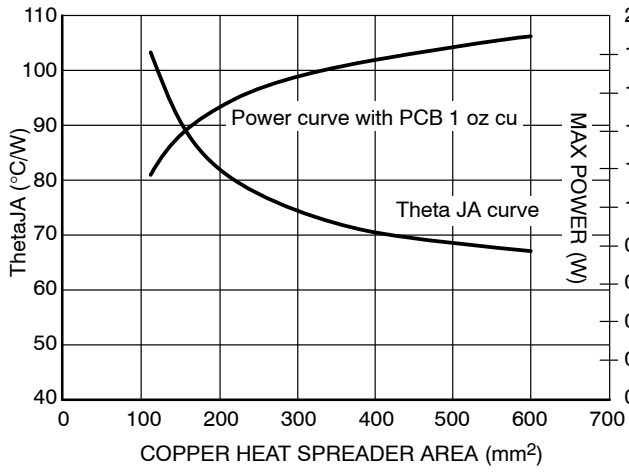
	DT=GND	DT=OUT
	Reset Time	Reset Time
NCV86601	8 ms	128 ms
NCV86602	8 ms	32 ms
NCV86603	16 ms	64 ms
NCV86604	32 ms	128 ms

The Delay Time select (DT) pin is logic level controlled and provides Reset Delay time per the chart. Note the DT pin is sampled only when RO is low, and changes to the DT pin when RO is high will not effect the reset delay time.

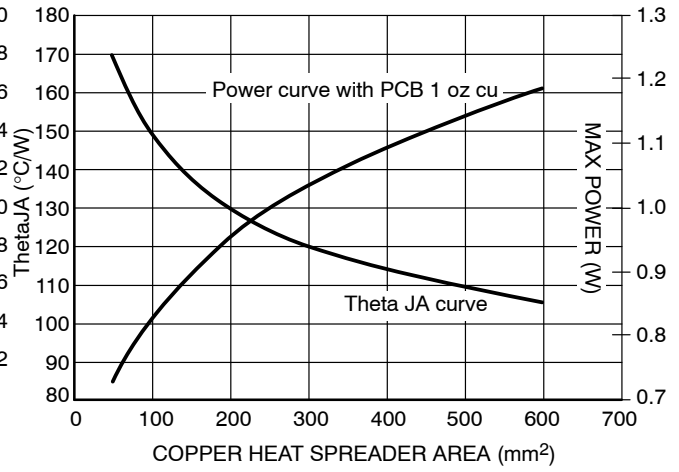
### Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold, a Thermal Shutdown event is detected OUT is turned off, and RO goes low. The IC will remain in this state until the die temperature moves below the shutdown threshold (175°C typical) minus the hysteresis factor (25°C typical). The output will then turn back on and RO will go high after the RESET Delay time.

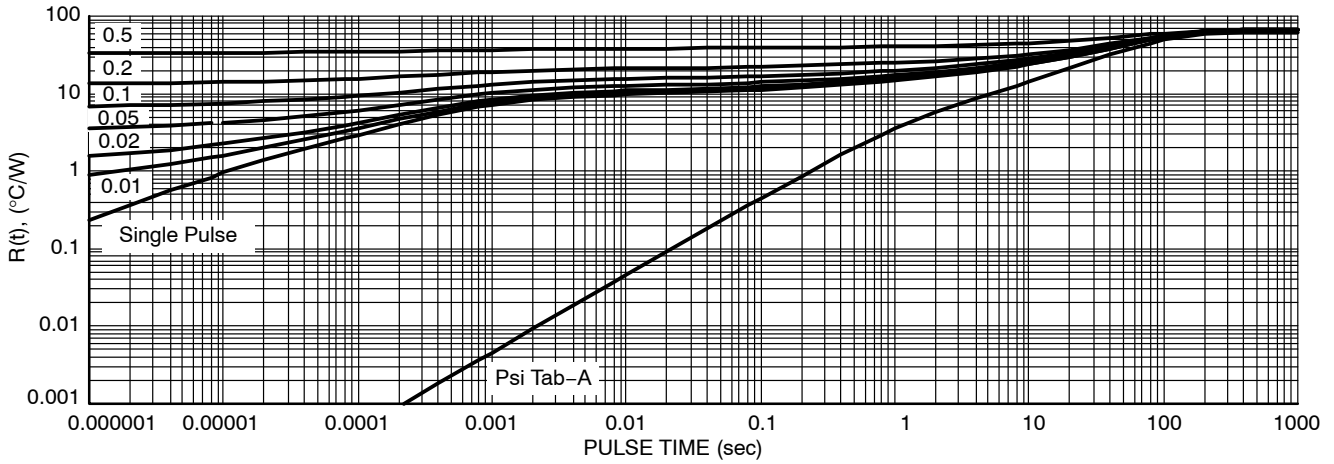
# NCV8660



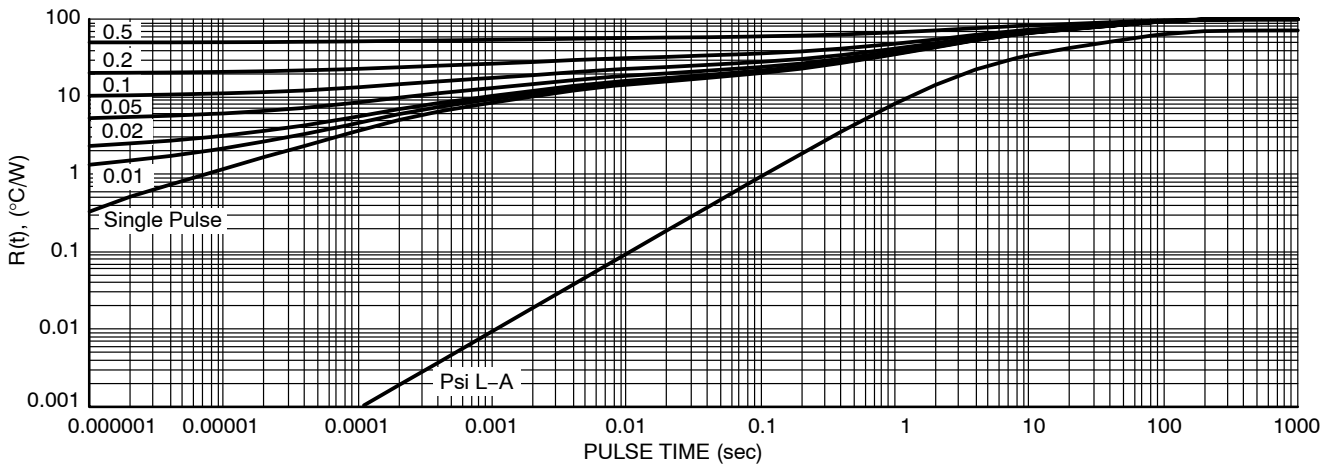
**Figure 26.  $R_{\theta JA}$  vs. PCB Copper Area (DPAK)**



**Figure 28.  $R_{\theta JA}$  vs. PCB Copper Area (SOIC-8 Fused)**



**Figure 27. Transient Thermal Response (DPAK)  
Cu Area = 645 mm<sup>2</sup>**



**Figure 29. Transient Thermal Response (SOIC-8 Fused)  
Cu Area = 645 mm<sup>2</sup>**

# NCV8660

## ORDERING INFORMATION

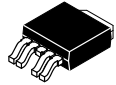
Device	Output Voltage	Reset Delay Time, DT to GND	Reset Delay Time, DT to OUT	Package	Shipping <sup>†</sup>
NCV86601DT50RKG	5.0 V	8 ms	128 ms	DPAK (Pb-Free)	2500 / Tape & Reel
NCV86602DT50RKG		8 ms	32 ms		
NCV86603DT50RKG		16 ms	64 ms		
NCV86604DT50RKG		32 ms	128 ms		
NCV86601D50G		8 ms	128 ms	SOIC-8 FUSED (Pb-Free)	98 Units / Rail
NCV86601D50R2G		8 ms	128 ms		
NCV86602D50R2G		8 ms	32 ms		
NCV86603D50R2G		16 ms	64 ms		
NCV86604D50R2G		32 ms	128 ms		
NCV86604D50R2G		32 ms	128 ms		
NCV86601DT33RKG	3.3 V	8 ms	128 ms	DPAK (Pb-Free)	2500 / Tape & Reel
NCV86602DT33RKG		8 ms	32 ms		
NCV86603DT33RKG		16 ms	64 ms		
NCV86604DT33RKG		32 ms	128 ms		
NCV86601D33R2G		8 ms	128 ms	SOIC-8 FUSED (Pb-Free)	2500 / Tape & Reel
NCV86602D33R2G		8 ms	32 ms		
NCV86603D33R2G		16 ms	64 ms		
NCV86604D33R2G		32 ms	128 ms		

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



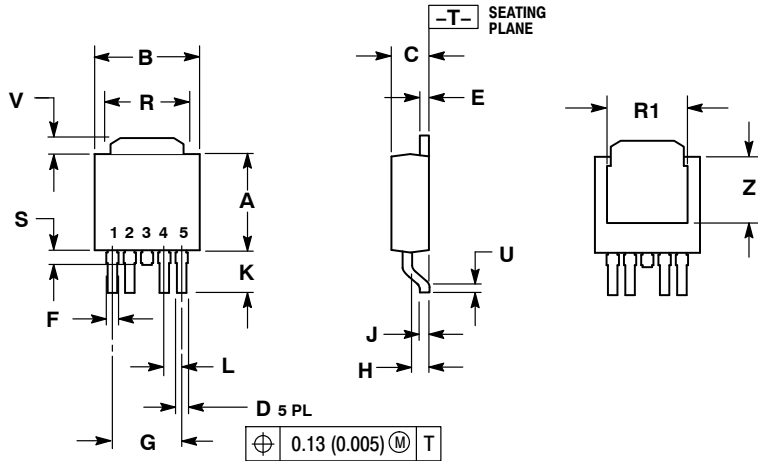
### DPAK-5, CENTER LEAD CROP

#### CASE 175AA

#### ISSUE B

DATE 15 MAY 2014

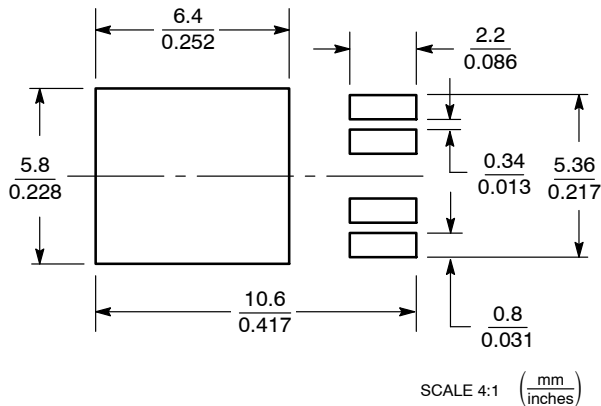
SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

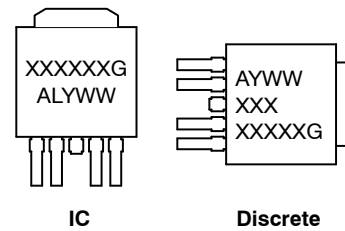
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAMS\*



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

<b>DOCUMENT NUMBER:</b>	<b>98AON12855D</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>DPAK-5 CENTER LEAD CROP</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

## GENERIC MARKING DIAGRAM\*



SCALE 6:1 ( $\frac{\text{mm}}{\text{inches}}$ )



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and ONsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p>STYLE 11:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p>STYLE 12:<br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 13:<br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p>STYLE 14:<br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p>STYLE 19:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p>STYLE 20:<br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 21:<br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p>STYLE 22:<br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p>STYLE 24:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p>STYLE 26:<br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p>STYLE 27:<br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p>STYLE 28:<br/>         PIN 1. SW_TO_GND<br/>         2. DASIC_OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p>STYLE 29:<br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |  |  |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42564B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-8 NB</b>	<b>PAGE 2 OF 2</b>

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative