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APPLICATION NOTE 245

Adding Hysteresis to CPU Supervisor Voltage Sense Inputs Monitoring Upstream Voltage Supplies for Power-Fail Warnings

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Abstract: One of the most important features in any embedded design is ensuring that important data is properly saved and the system reaches a safe/known state as power is failing. A CPU supervisor with a voltage sense input can monitor an upstream voltage supply and provide a warning signal to the microprocessor that signifies that power is failing. This allows the microprocessor time to save critical data and reach a safe/known state before the CPU supervisor, which will also be monitoring the processor's power supply, resets the processor. This application note shows how to add hysteresis to the upstream voltage supply's trip level, which prevents the power-fail warning signal from chattering due to noise. This circuit provides a great tool for producing a sophisticated power-supply monitoring system that will help to produce a robust embedded design.

CPU Supervisor Basics

Basic CPU supervisors monitor a processor's V_{CC}, and reset the processor when V_{CC} drops below a predetermined level, V_{CCTP}. V_{CCTP} is generally 5-20% below the nominal V_{CC} value. This function prevents the processor from operating when V_{CC} is below the processor's specified voltage supply range. Most CPU supervisors also provide a reset delay that holds the processor's reset line active for several milliseconds after V_{CC} has reached its specified value. This allows reset to be held active for a short time after power is applied to the processor for peripherals to ready for communication, and it provides a chance for the power supply to stabilize before the processor begins execution.

By themselves, these functions help to produce a reasonably robust power monitoring system; however, problems can still arise as power is failing because the reset line will be immediately set active as soon as V_{CC} drops below V_{CCTP}. Because there is no warning signal to allow the processor to save important data and reach a safe state, there is no way to ensure the system is ready for the reset to occur.

Voltage Sense Inputs

The voltage sense inputs within CPU supervisors are comparators that have internal temperature and voltage compensated references. The internal reference voltage (referenced as V_{REF} in the equations below) is typically either 1.25V or 2.5V. By using the voltage sense input with an external voltage divider, the supervisor can provide an adjustable trip level monitor that can detect high voltages. **Figure 1** shows a classic voltage monitor with no hysteresis. In this circuit the non-maskable interrupt output ("NMI-bar") is asserted whenever V_{IN} drops below the V_{IN} trip level (V_{INTP}) calculated using Equation 1.
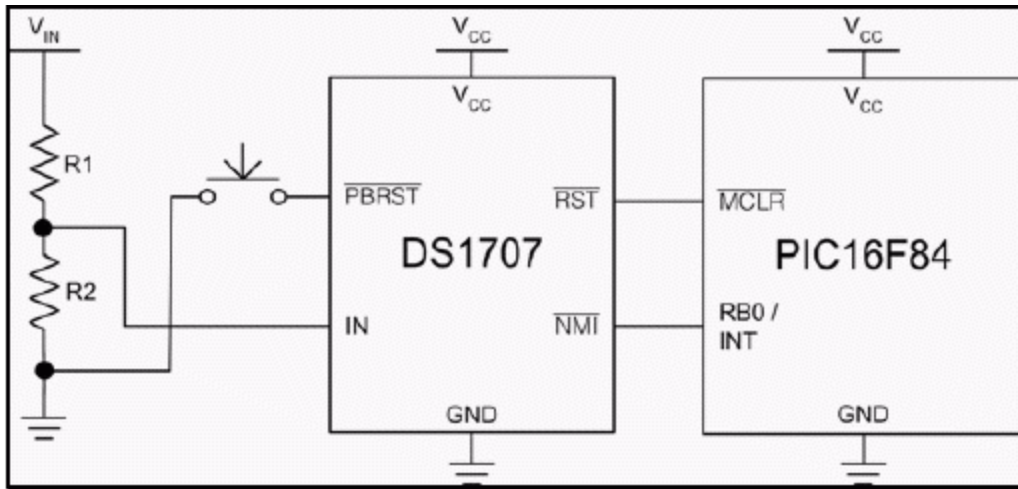
Figure 1. The classic voltage detection circuit.

$$V_{INTP} = \frac{V_{REF}\,(R1 + R2)}{R2}$$

(Eq. 1)

In systems that utilize a regulator to generate the microprocessor's V_{CC} from an upstream power source, the upstream supply can be monitored using a CPU supervisor with a voltage sense input. When the upstream supply begins to drop in voltage, it is detected before the microprocessor's voltage regulator output falls out of specification. This provides time for the microprocessor to ready for the impending power failure.

On Dallas Semiconductor's CPU supervisors, the voltage sense inputs are generally labeled as IN, and their corresponding outputs, which are intended to be routed to a microprocessor's non-maskable interrupt input, are labeled "NMI-bar". It should be noted that the "NMI-bar" outputs of these devices are not always complementary outputs. The DS1831 for example has open drain outputs, and will require a pull-up resistor on both "RST-bar" and "NMI-bar". See **Figure 2** for a list of supervisors with voltage sense inputs.

Figure 2. CPU supervisors with voltage sense inputs

DS1231	DS1238	DS1238A	DS1239
DS1705	DS1706	DS1707	DS1708
DS1831	DS1831A	DS1831B	DS1831C
DS1831D	DS1831E		

Adding Hysteresis to CPU Supervisor Voltage Sense Inputs

The voltage sense inputs on Dallas Semiconductor's CPU supervisors do not provide any internal hysteresis, but with the addition of a feedback resistor as shown in **Figure 3**, hysteresis can be added. Equations 2 and 3 calculate the V_{IN} trip points with the added hysteresis. Voltages above V_{INTP_PG} will result in "NMI-bar" being deasserted because the power supply is at an adequate level. Voltages below V_{INTP_PF} will assert "NMI-bar" to indicate a failing supply. Equation 4 calculates the amount of the hysteresis added to the circuit by the feedback resistor. This shows that decreasing the value of the

feedback resistor will increase the amount of the hysteresis. **Figure 4** shows the hysteresis as a function of V_{IN}.
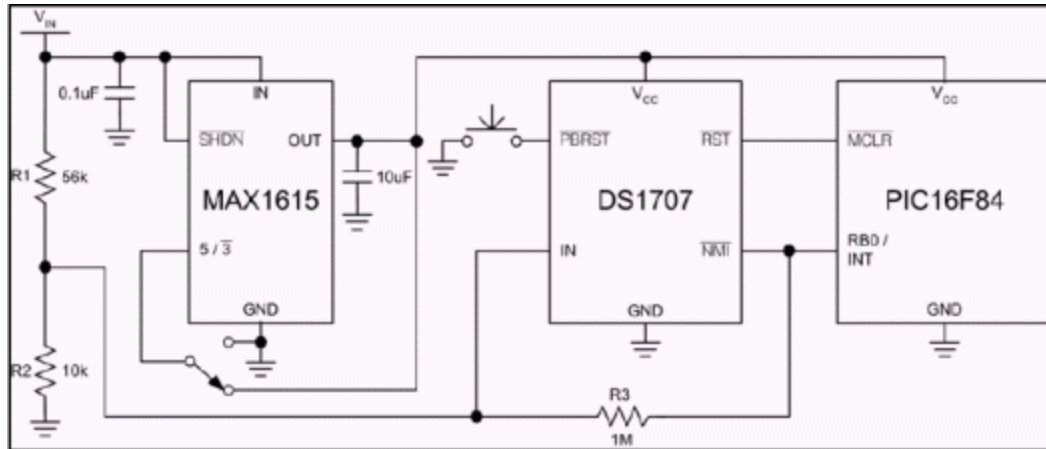

Figure 3. High voltage monitor with hysteresis.

$$V_{INTP\_PG} = R1\left(\frac{V_{REF}}{R2} + \frac{V_{REF}}{R3}\right) + V_{REF} \qquad \text{(Eq. 2)}$$

$$V_{INTP\_PF} = R1\left(\frac{V_{REF}}{R2} - \frac{V_{CC} - V_{REF}}{R3}\right) + V_{REF} \qquad \text{(Eq. 3)}$$

$$V_{HYST} = V_{INTP\_PG} - V_{INTP\_PF} = V_{CC}\left(\frac{R1}{R3}\right) \qquad \text{(Eq. 4)}$$
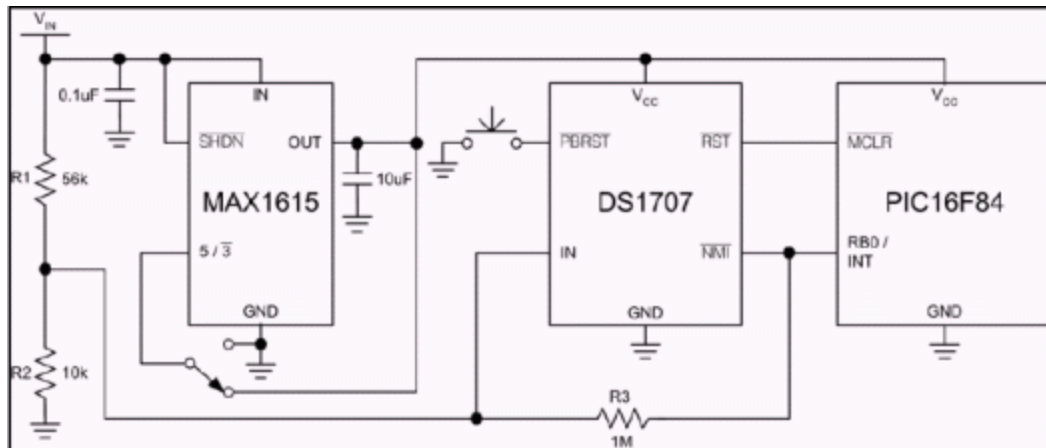

Figure 4. "NMI-bar" outpus hysteresis as a function of V_{IN}.

The example circuit shows a MAX1615 regulator that is configured to provide a 5.0V supply using its 5/"3-bar" input. The voltage input for the regulator, V_{IN}, is being monitored by the voltage sense input (DS1707's V_{REF} = 1.25V, typical) of the DS1707. The DS1707 is configured by the resistors shown in

Figure 3 to allow operation when $V_{IN} > V_{INTP\_PG} = 8.32V$. When $V_{IN} < V_{INTP\_PF} = 8.04V$, the "NMI-bar" output will be asserted to inform the processor that the V_{IN} supply is failing. This setup provides 280mV of hysteresis to prevent the "NMI-bar" output from chattering in the event that V_{IN}, which is likely to be moderately noisy, remains near the monitoring trip point for an extended period of time. In addition to monitoring V_{IN}, the DS1707 is monitoring the MAX1615's output (V_{CC}) to ensure that it remains above the DS1707's 5.0V 10% trip level.

Handling the "NMI-bar" Interrupt

The "NMI-bar" interrupt's purpose in this instance is to ensure that the processor gracefully shuts itself down when upstream power is failing, which will eventually cause the 3.3V/5V power supply to fail. One simple approach is to save all the application's data, get the application to a safe state, and halt execution until power is restored. **Figure 5** shows pseudocode to accomplish this task.

Figure 5. Pseudocode for the "NMI-bar" interrupt service routine
- **Save** the application's data
- **Shutdown Application** (put the system in to a safe state for shutdown, inform user, ...)
- **If** ("NMI-bar"> = 1)
  > **Then** Power has restored: Continue executing where you left off OR restart application
  > **Else** Upstream power is still below the trip level: Continue polling "NMI-bar" until 3.3V/5V power fails or the upstream power raises back above the trip level.

As shown in Figure 5, The "NMI-bar" pin can be polled to determine if power has been restored or is still below the trip level (V_{INTP_PG}). If it is below the trip level, it can signify either V_{IN} is still dropping but is at a high enough voltage level that the regulator can maintain V_{CC}, or that the power is in a "brown out" condition. If it drops far enough, the regulator will no longer be able to provide V_{CC} to the system within the tolerance of the DS1707, which will reset the processor. If the upstream power goes back above (V_{INTP_PG}), the application can be restarted either from the beginning or where it left off depending on the system's requirements. The critical item to keep in mind while programming this algorithm is the timing of the situation. When power is failing, the amount of time that the processor has to save data and reach a safe state will be system dependent. Thus, this algorithm should be as short as possible, and extensively tested to ensure that this routine will shutdown the application and be polling the "NMI-bar" pin before the DS1707 will shutdown the application because V_{CC} has failed.

Conclusion

Hysteresis can be added to any voltage sense input by utilizing a feedback resistor. The hysteresis prevents the CPU supervisor's "NMI-bar" output from chattering due to noise if the input voltage hovers near the trip point. This improves the quality of the "NMI-bar" output signal that is used as an early warning that power is failing. When processor receives the "NMI-bar" interrupt, it can save critical data and reach a defined state before it is eventually reset as the voltage continues to drop. By allowing the processor to reach the same safe state each time before power fails, the systems behavior during power fail conditions becomes predictable and reliable.

Related Parts		
DS1231	Power Monitor	Free Samples
DS1238	MicroManager	
DS1238A	MicroManager	
DS1239	MicroManager Chip	

DS1705	3.3V and 5.0V MicroMonitor	Free Samples
DS1706	3.3V and 5.0V MicroMonitor	Free Samples
DS1707	3.3 and 5.0 Volt MicroMonitor	Free Samples
DS1708	3.3 and 5.0 Volt MicroMonitor	Free Samples
DS1831A	Multisupply MicroMonitor™	Free Samples
DS1831B	Multisupply MicroMonitor™	Free Samples
DS1831C	3.3V/2.5V Multisupply Micromonitor	Free Samples
DS1831D	3.3V/2.5V Multisupply Micromonitor	Free Samples
DS1831E	3.3V/2.5V Multisupply Micromonitor	Free Samples

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