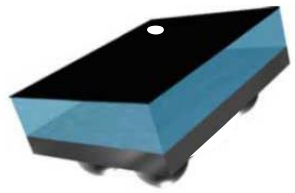
BAL-NRF01D3

50 Ω nominal input / conjugate match balun to nRF51422-QFAA, nRF24LE1, nRF51822-QFAA/AB, with integrated harmonic filter

Datasheet - production data



Lead-free Flip-Chip (5 bumps) package

Features

- 50 Ω nominal input / conjugate match to Nordic Semiconductor chips nRF24LE1 QFN32, nRF24AP2-1CH, nRF24AP2-8CH, nRF51422-QFAA (build code CA/C0), nRF51822-QFAA (build code CA/C0) and nRF51822-QFAB (build code AA/A0)
- Low insertion loss
- Low amplitude imbalance
- Low phase imbalance
- Small footprint < 1.5 mm^2

Benefits

- Very low profile < 595 µm after reflow
- High RF performance
- RF BOM and area reduction

Applications

- 2.45 GHz impedance matched balun filter
- Optimized for Nordic's chip set nRF24LE1/AP2, nRF51422-QFAA (build code CA/C0), nRF51822-QFAA (build code CA/C0) and nRF51822-QFAB (build code AA/A0)

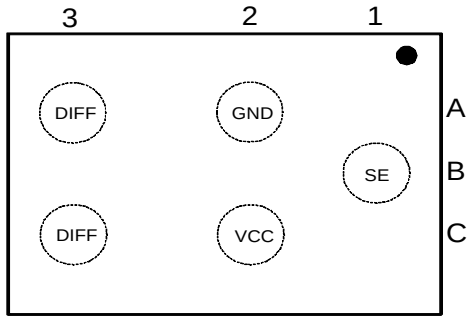
Description

STMicroelectronics BAL-NRF01D3 is an ultraminiature balun. The device integrates matching network and harmonics filter. Matching impedance has been customized for the following Nordic Semiconductor circuits: nRF24LE1 QFN-32 pins, nRF24AP2-1CH, nRF24AP2-8CH, nRF51422-QFAA (build code CA/C0), nRF51822-QFAA (build code CA/C0) and nRF51822-QFAB (build code AA/A0).

The device uses STMicroelectronics' IPD technology on a non-conductive glass substrate to optimize RF performance.

The BAL-NRF01D3 has been tested and approved by Nordic Semiconductor in their nRF2723 and nRF2752 nRFgo modules.

Figure 1: Application schematic



1 Characteristics

Table 1: Absolute maximum ratings (limiting values)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
P_{IN}	Input power RFIN		-	20	dBm
V_{ESD}	ESD ratings MIL STD883C (HBM: C = 100 pF, R = 1.5 Ω, air discharge)	2000	-		V
	ESD ratings charge device model (JESD22-C101-C)	500			
	ESD ratings machine model (MM: C = 200 pF, R = 25 W, L = 500 nH)	200	-		
T_{OP}	Operating temperature	-40	-	+105	°C

Table 2: Impedances (T_{amb} = 25 °C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Z_{OUT}	Nominal differential output impedance	-	Conjugate match to: nRF24LE1/AP2 nRF51422-QFAA (build code CA/C0) nRF51822-QFAA (build code CA/C0) nRF51822-QFAB (build code AA/A0)	-	Ω
Z_{IN}	Nominal input impedance	-	50	-	Ω

Table 3: RF performance (T_{amb} = 25 °C)

Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
F	Frequency range (bandwidth) 2400 2540		2400		2540	MHz
I_L	Insertion loss in bandwidth			2.25		dB
R_L	Return loss in bandwidth			10		dB
ϕ_{imb}	Phase imbalance			3		°
A_{imb}	Amplitude imbalance			0.1		dB
2f0	2nd harmonic filtering	4880 MHz		10		dB
3f0	3rd harmonic filtering	7320 MHz		20		dB

1.1 RF measurement

Figure 2: Transmission (T_{amb} = 25 °C)

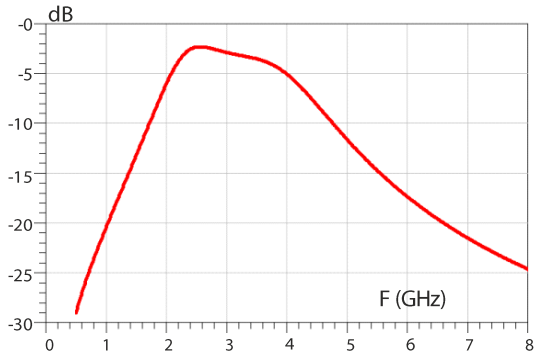


Figure 3: Return loss on SE port (T_{amb} = 25 °C)

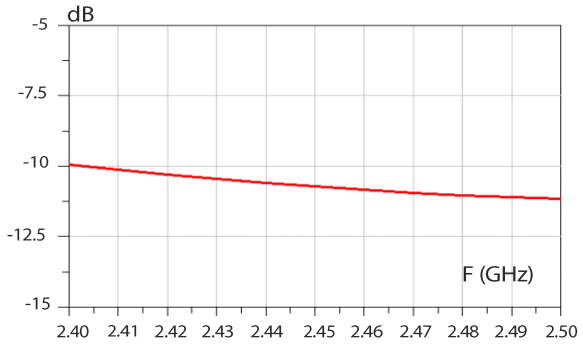


Figure 4: Return loss on DIFF port (T_{amb} = 25 °C)

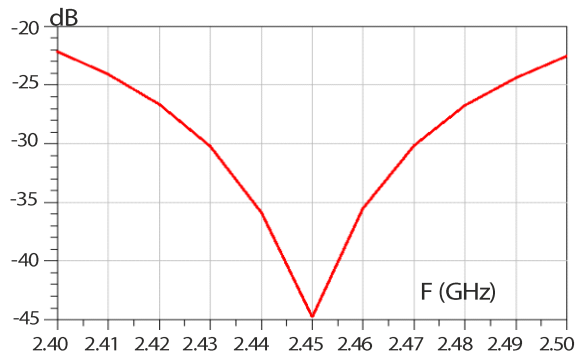


Figure 5: Amplitude imbalance (T_{amb} = 25 °C)

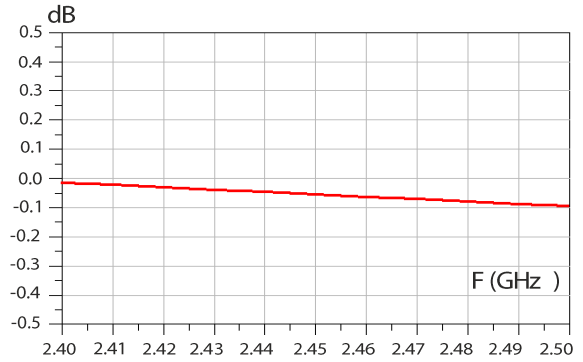
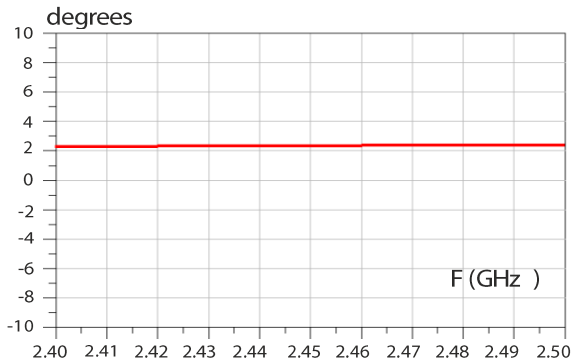


Figure 6: Phase imbalance (T_{amb} = 25 °C)



2 Application information

Figure 7: Application schematic (courtesy of Nordic Semiconductor)

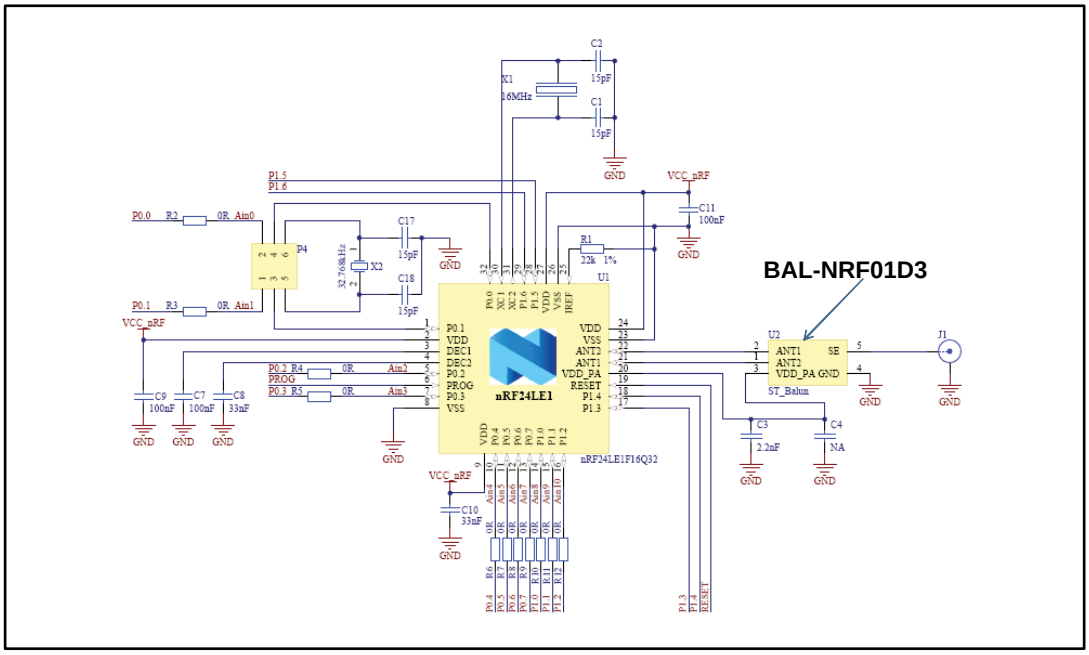


Figure 8: nRF2723 application board (courtesy of Nordic Semiconductor)

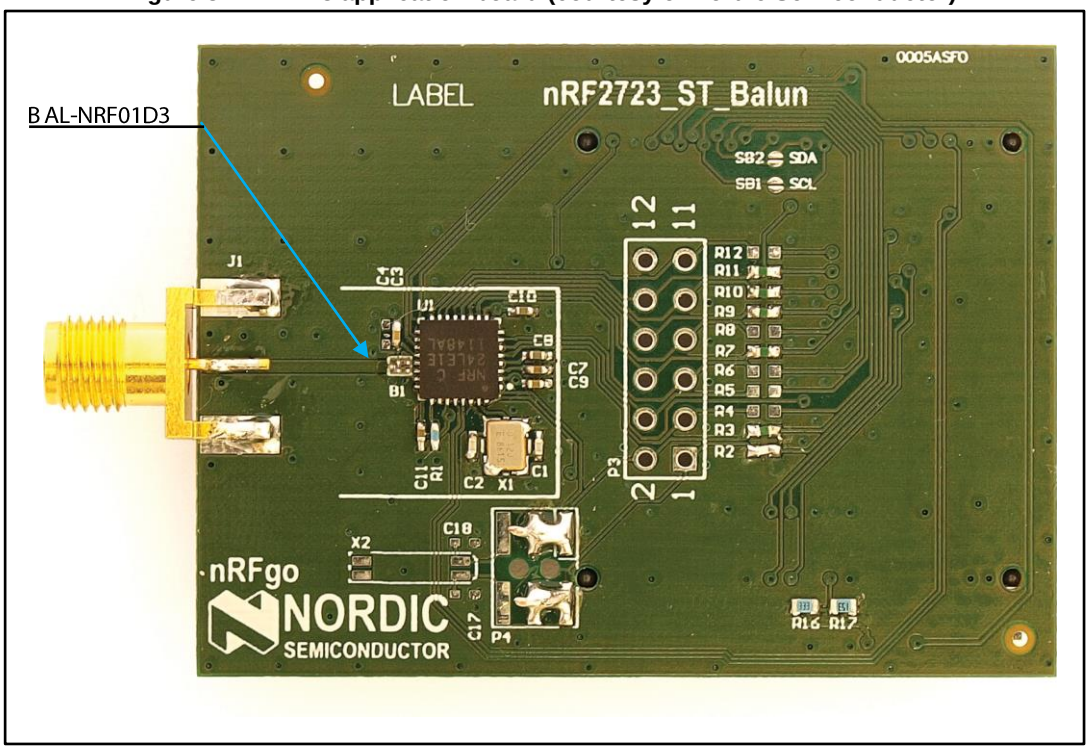
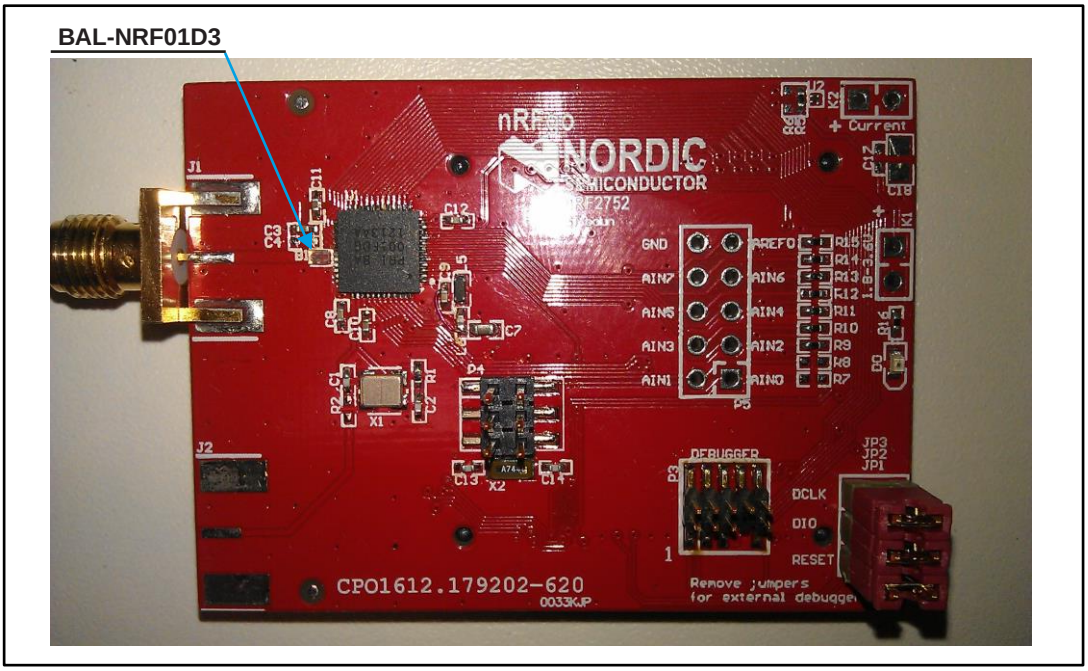


Figure 9: nRF2752 application board (courtesy of Nordic Semiconductor)



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

- Epoxy meets UL94, V0
- Lead-free package

3.1 Flip-Chip 5 bumps package information

Figure 10: Flip-Chip 5 bumps package outline

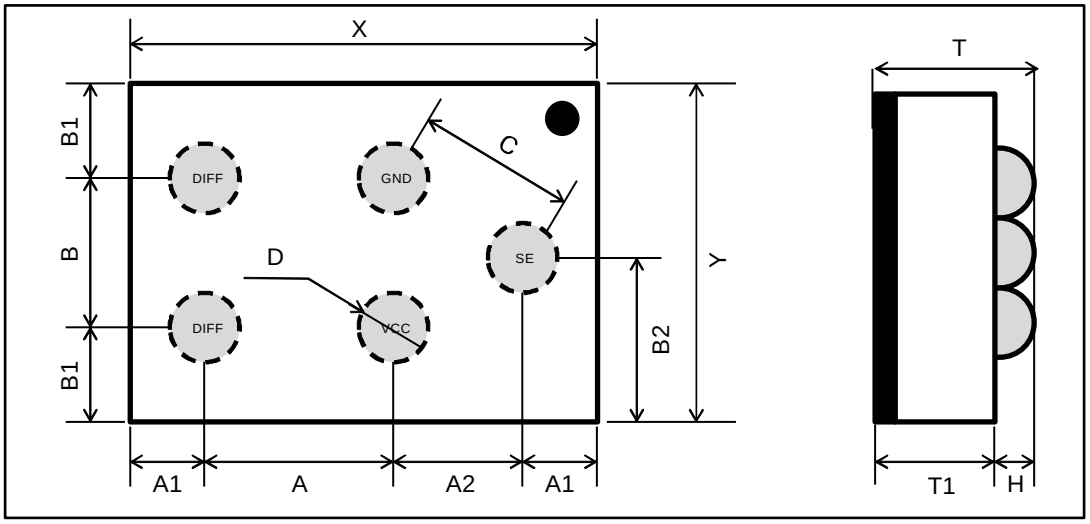


Table 4: Flip-Chip 5 bumps dimensions

Parameter	Description	Min.	Typ.	Max.	Unit
X	X dimension of the die	1445	1485	1525	mm
Y	Y dimension of the die	980	1020	1060	mm
A	X pitch		604		mm
B	Y pitch		500		mm
A1	Distance from bump to edge of die on X axis		224		mm
B1	Distance from bump to edge of die on Y axis		260		mm
A2	Distance from VCC bump to SE bump on X axis		433		mm
B2	Distance from bump to edge of die on Y axis		510		mm
C	GND, VCC bump to SE bump pitch		500		mm
D	Bump diameter	240	255	260	mm
T1	Substrate thickness		425		mm
H	Bump height		205		mm
T	Total die thickness	570	630	690	

Figure 11: Footprint - 3 mils stencil -non solder mask defined

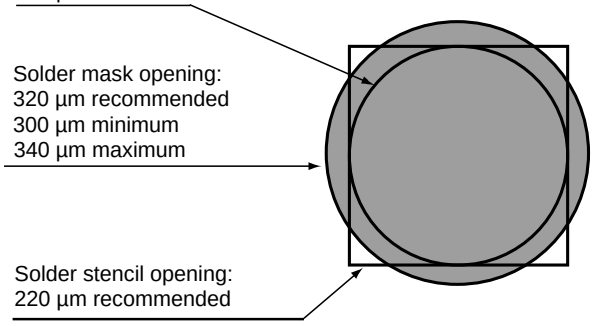


Figure 12: Footprint - 3 mils stencil - solder mask defined

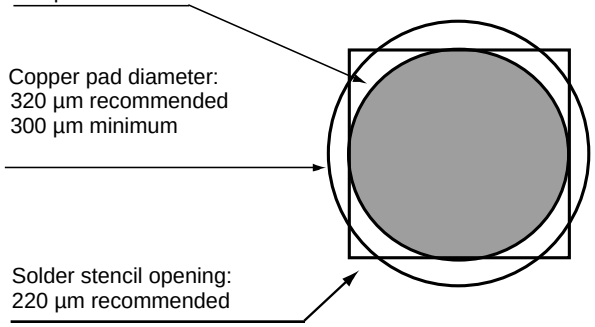
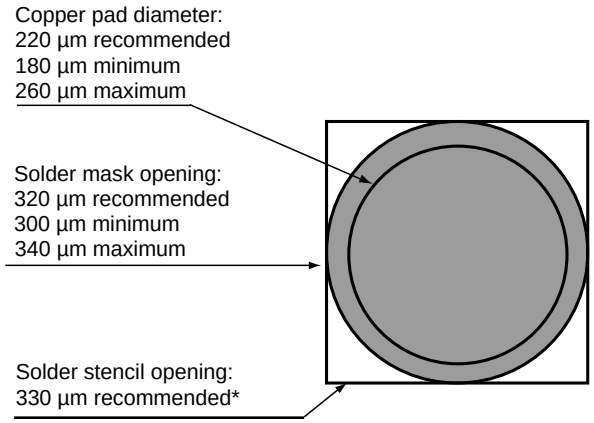
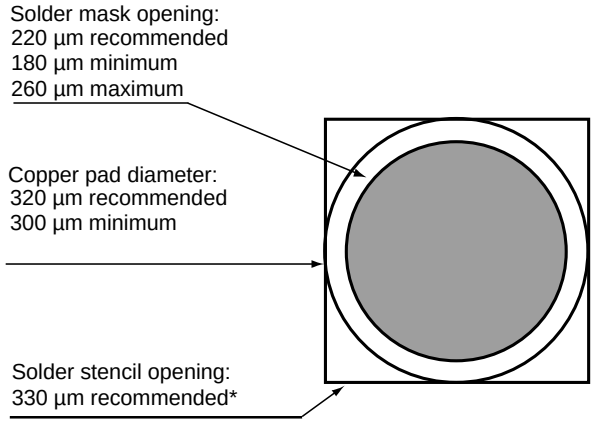


Figure 13: Footprint - 5 mils stencil -non solder mask defined



*depending on paste, it can go down to 270 µm

Figure 14: Footprint - 5 mils stencil - solder mask defined



*depending on paste, it can go down to 270 µm

3.2 Flip-chip 5 bumps packing information

Figure 15: Marking

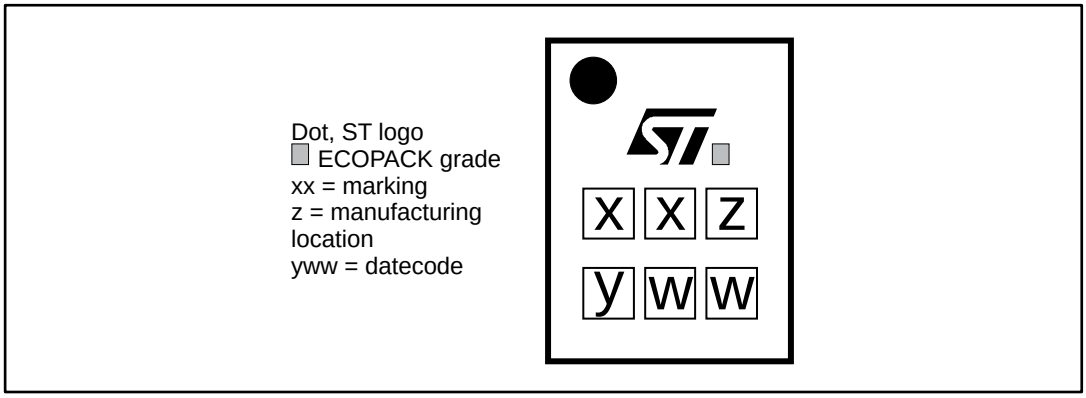
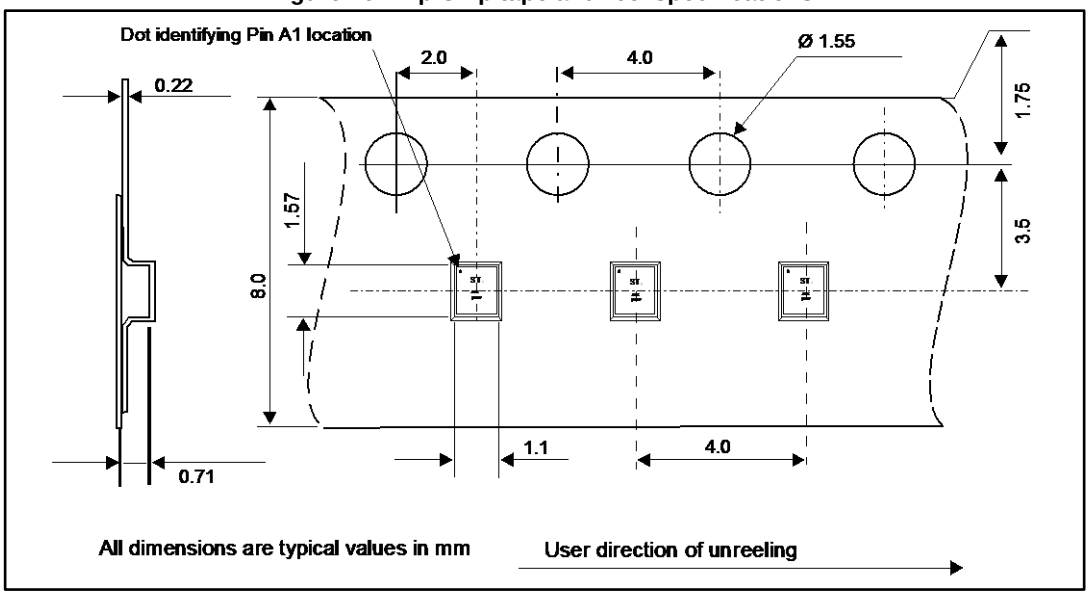


Figure 16: Flip Chip tape and reel specifications



More packing information is available in the application note:

- AN2348 Flip-Chip: “Package description and recommendations for use”
- AN4111: “BAL-NRF01D3 matched balun with integrated harmonics filter for Nordic Semiconductor chips with ultralow power transceivers”

4 Ordering information

Table 5: Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
BAL-NRF01D3	SC	Flip-Chip package (5 bumps)	1.82 mg	5000	Tape and reel

5 Revision history

Table 6: Document revision history

Date	Revision	Changes
15-Oct-2012	1	First issue.
13-Nov-2012	2	Added references to nRF51 series. Added Figure 9. Updated y-axis labels in Figure 2.
04-Mar-2013	3	Updated footprint illustrations in Figure 13, and Figure 14.
06-Aug-2013	4	Added dimensions in Figure 10. Updated marking orientation in Figure 11 and Figure 12.
13-Jan-2014	5	Updated document title and product references.
07-Jul-2015	6	Updated Table 1.
21-Jun-2017	7	Updated *Figure 10: "Flip-Chip 5 bumps package outline"* and *Table 4: "Flip-Chip 5 bumps dimensions"*.

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