

PCN Number:	20181127000.0	PCN Date:	Dec. 11, 2018
Title:	Datasheet for TUSB564,TUSB1064		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product datasheet(s) is being updated as summarized below. The following change history provides further details.



TUSB564

SLLSF29D –OCTOBER 2017–REVISED NOVEMBER 2018

Changes from Revision C (February 2018) to Revision D	Page
• Changed the RNQ pin image appearance	3
• Changed the EN pin Description in the <i>Pin Functions</i> table	4
• Changed the HPDIN pin From: I/O To: 2 Level I	4
• Added pull-down indicator (PD) in the I/O column on FLIP/SCL and CTL0/SDA pins	4
• Added Junction temperature to absolute maximum ratings table	5
• From: Internal pull-down resistance for CTL1. To: Internal pull-down resistance for CTL1, CTL0, FLIP, and EN	6
• Deleted EN from Note 1 of Table 8	23



TUSB1064

SLLSF48A –MARCH 2018–REVISED NOVEMBER 2018

Changes from Original (March 2018) to Revision A	Page
• Changed the RNQ pin image appearance	3
• Changed the column on EN From: I To: 2 Level I (PD)	4
• Changed the EN pin Description in the <i>Pin Functions</i> table	4
• Changed the HPDIN pin From: I/O To: 2 Level I	4
• Added pull-down indicator (PD) in the I/O column on FLIP/SCL and CTL0/SDA pins	4
• Added Junction temperature to absolute maximum ratings table.	5
• From: Internal pull-down resistance for CTL1. To: Internal pull-down resistance for CTL1, CTL0, FLIP, and EN.	6
• Deleted EN from Note 1 of Table 8	23

The datasheet number will be changing.

Device Family	Change From:	Change To:
TUSB564	SLLSF29C	SLLSF29D
TUSB1064	SLLSF48	SLLSF48A

These changes may be reviewed at the datasheet links provided.

<http://www.ti.com/product/TUSB564>

<http://www.ti.com/product/TUSB1064>

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:			
None.			
Product Affected:			
TUSB564IRNQR	TUSB564IRNQT	TUSB564RNQR	TUSB564RNQT
TUSB1064IRNQR	TUSB1064IRNQT	TUSB1064RNQR	TUSB1064RNQT

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com