

<b>PCN Number:</b>	20221215004.0	<b>PCN Date:</b>	December 16, 2022
<b>Title:</b>	DP83869H Firmware and Datasheet Updates		
<b>Customer Contact:</b>	<a href="#">PCN Manager</a>	<b>Dept:</b>	Quality Services
<b>Change Type:</b>			
<input type="checkbox"/> Assembly Site	<input type="checkbox"/> Assembly Process	<input type="checkbox"/> Assembly Materials	
<input checked="" type="checkbox"/> Design	<input checked="" type="checkbox"/> Electrical Specification	<input type="checkbox"/> Mechanical Specification	
<input type="checkbox"/> Test Site	<input type="checkbox"/> Packing/Shipping/Labeling	<input type="checkbox"/> Test Process	
<input type="checkbox"/> Wafer Bump Site	<input type="checkbox"/> Wafer Bump Material	<input type="checkbox"/> Wafer Bump Process	
<input type="checkbox"/> Wafer Fab Site	<input type="checkbox"/> Wafer Fab Materials	<input type="checkbox"/> Wafer Fab Process	
	<input type="checkbox"/> Part number change		

### PCN Details

#### Description of Change:

This notification is to communicate an update for the DP83869H devices to correct an occasional anomaly in fiber auto-negotiation. As a result, the PHYIDR2 Register (address = 0x3) value is changing from 0xA0F1 to 0xA0F3.

Customers may need to update their application firmware as the PHY driver may be checking for PHYIDR2 register 0x3 content.

It is recommended to use an OR function for PHYIDR2 register contact check in the firmware so it can be used seamlessly.

The product datasheet(s) is being updated as summarized below.



**DP83869HM**  
SNLS614B – SEPTEMBER 2018 – REVISED DECEMBER 2022

Changes from Revision A (September 2018) to Revision B (December 2022)	Page
• Changed fiber compliance to current Specification .....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Deleted leading 0 from all register, read, and write statements .....	25
• Deleted 1000Base-X fiber application clarification, bug has been fixed .....	33
• Changed bridge mode image and description to clarify TX and RX pin behavior.....	38
• Changed description of Media Converter mode to support Unmanaged Media Converter mode in response to bug fix .....	38
• Changed register read and writes to correct values with comments .....	39
• Changed number of PHYs and size of PHY address to correct values.....	40
• Added clarification for Auto-Negotiation setting.....	48
• Changed strapping modes in the figure and description to correct values.....	48
• Changed <a href="#">Table 10-1</a> to clarify Frequency Tolerance .....	91
• Changed <a href="#">Table 10-2</a> to clarify Frequency Tolerance .....	92
• Changed the two-supply config figure to the correct number of pins for VDDIO and VDD1P1, also changed the pin name from VDDA1P1 to VDD1P1.....	95
• Changed the three-supply config figure to the correct number of pins for VDDIO and VDD1P1, also changed the pin name from VDDA1P1 to VDD1P1.....	97

The datasheet number will be changing.

	Current	New
Product Family	Datasheet Number	Datasheet Number
DP83869HM	SNLS614A	<b>SNLS614B</b>

These changes may be reviewed at the datasheet links provided:

<http://www.ti.com/product/DP83869HM>

Affected devices are listed in the Product Affected section of this document.

**Reason for Change:**

Improved device functionality

**Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):**

None.

**Product Affected:**

DP83869HMRGZR	DP83869HMRGZT
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## Qualification Report

**Approve Date 07-Nov-2019**

### Qualification Results

**Data Displayed as: Number of lots / Total sample size / Total failed**

Type	Test Name / Condition	Duration	Qual Device: <u>DP83869-A2</u>	Qual Device: <u>DP83869A0</u>	Qual Device: <u>PDP83869A1</u>	QBS: Process References DS90UH947TRGCR Q1
HTOL	High Temp Operating Life, 125C	1000 Hours	-	1/77/0	1/77/0	3/231/0
ELFR	Early Life Failure Rate, 125C	48 Hours	-			3/2400/0
TC	**T/C -65C/150C	500 Cycles	-	3/231/0	-	3/231/0
AC	**Autoclave 121C	96 Hours	-	3/231/0	-	3/231/0
HAST	**Biased HAST, 110C/85% RH	264 Hours	-	3/231/0	-	3/231/0
HTSL	**High Temp. Storage Bake	170C (168, 420 Hours)	-	3/231/0	-	
ED	Electrical Characterization	Limit Verification	Pass	-	Pass	Pass
CDM	ESD CDM	1500V	1/3/0	1/3/0	1/3/0	1/3/0
HBM	ESD HBM	4000V	1/3/0	1/3/0	1/3/0	1/3/0
LU	Latch-up, 25C	(per JESD78)	1/6/0	1/6/0	1/6/0	1/6/0
LU	Latch-up, 125C	(per JESD78)	1/6/0	1/6/0	1/6/0	1/6/0
BPC	Bond Pad Cratering Check	Post 500 Temp Cycle	-	3/5/0	-	
BPC	Bond Pad Cratering Check	Post assembly	-	3/6/0	-	
MQ	Manufacturability (Assembly)	(per mfg. Site specification)	-	Pass	-	
TC-BP	Post T/C bond-pull strength	Wires	-	3/30/0	-	
TC-SAM	Post Temp Cycle SAM	Pre and Post MSL	-	3/30/0	-	
VM	Visual Quality Reliability Inspection	Post 500 Cycle Temp Cycle	-	3/2/0	-	
VM	Visual Quality Reliability Inspection	Post HTSL	-	3/2/0	-	
WBP	Bond Pull	Wires	-	3/228/0	-	
BLR	BLR - Temp Cycle (QFN), -40/125C	1000 Cycles	-	1/32/0	-	

Type	Test Name / Condition	Duration	Qual Device: <u>DP83869-A2</u>	Qual Device: <u>DP83869A0</u>	Qual Device: <u>PDP83869A1</u>	QBS: Process References DS90UH947TRGCR Q1
SD	Solderability w. Bake precon	4 Hours/@ 155C, Pb Free	-	3/66/0	-	
SD	Solderability w. Bake precon	4 Hours/@ 155C, Pb	-	3/66/0	-	

QBS: Qual By Similarity

- Qual Device DP83869 is qualified at LEVEL2-260C

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

- The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

- The following are equivalent HTSL options based on an activation energy of 0.7eV: 150C/1k Hours, and 170C/420 Hours

- The following are equivalent Temp Cycle options per JESD47: -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

**Green/Pb-free Status:**

Qualified Pb-Free(SMT) and Green

For questions regarding this notice, e-mails can be sent to the contact shown below or your local Field Sales Representative.

Location	E-Mail
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