

# TCA9548A-Q1 Automotive 8-Channel I<sup>2</sup>C Switch with Reset

## 1 Features

- AEC-Q100 (grade 1): Qualified for automotive applications
- [Functional Safety-Capable](#)
  - [Documentation available to aid in functional safety system design](#)
- 1-to-8 Bidirectional translating switches
- I<sup>2</sup>C Bus and SMBus compatible
- Active-low reset input
- Three address pins, allowing up to eight TCA9548A-Q1 devices on the I<sup>2</sup>C bus
- Channel selection through an I<sup>2</sup>C Bus, in any combination
- Power up with all switch channels deselected
- Low R<sub>ON</sub> switches
- Allows voltage-level translation between 1.8 V, 2.5 V, 3.3 V, and 5 V buses
- No glitch on power up
- Supports hot insertion
- Low quiescent current
- Operating power-supply voltage range of 1.65 V to 5.25 V
- 5 V tolerant Inputs
- 0 to 400 kHz clock frequency
- Latch-up performance exceeds 100 mA per JESD 78, class II

## 2 Applications

- [Infotainment](#)
- [Body and control](#)
- Routers (telecom switching equipment)
- [Factory automation](#)
- Products with I<sup>2</sup>C target address conflicts (such as multiple, identical temperature sensors)

## 3 Description

The TCA9548A-Q1 device has eight bidirectional translating switches that can be controlled through the I<sup>2</sup>C bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Any individual SC<sub>n</sub>/SD<sub>n</sub> channel or combination of channels can be selected, determined by the contents of the programmable control register. These downstream channels can be used to resolve I<sup>2</sup>C target address conflicts. For example, if eight identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0-7.

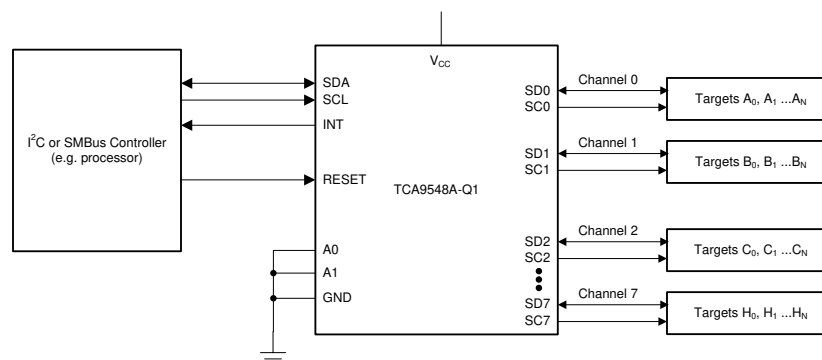
The system controller can reset the TCA9548A-Q1 in the event of a time-out or other improper operation by asserting a low in the  $\overline{\text{RESET}}$  input. Similarly, the power-on reset deselects all channels and initializes the I<sup>2</sup>C/SMBus state machine. Asserting  $\overline{\text{RESET}}$  causes the same reset and initialization to occur without powering down the part. This allows recovery should one of the downstream I<sup>2</sup>C buses get stuck in a low state.

The pass gates of the switches are constructed so that the VCC pin can be used to limit the maximum high voltage, which is passed by the TCA9548A-Q1. Limiting the maximum high voltage allows the use of different bus voltages on each pair, so that 1.8 V, 2.5 V or 3.3 V parts can communicate with 5 V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

### Device information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
TCA9548A-Q1	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified application diagram



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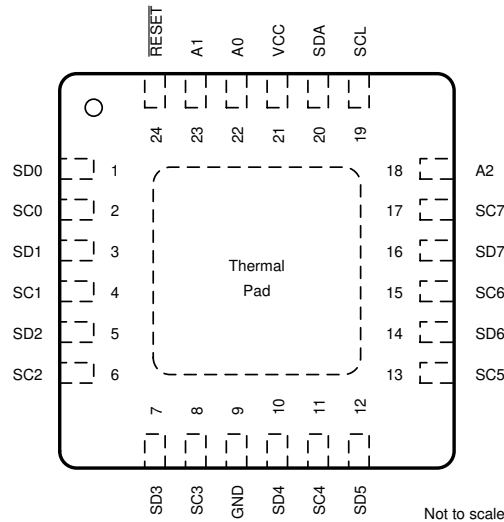
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (November 2019) to Revision B (October 2021)</b>	<b>Page</b>
• Added feature: <i>Functional Safety-Capable</i> .....	1
• Added grade 1 to the automotive feature, and deleted <i>Temperature grade 3: -40°C to +85°C, T<sub>A</sub></i> .....	1
• Globally changed instances of legacy terminology to controller and target where mentioned.....	1

<b>Changes from Revision * (May 2019) to Revision A (November 2019)</b>	<b>Page</b>
• V <sub>CC</sub> value missing, added V <sub>CC</sub> = 2.5 V in <a href="#">Figure 9-1</a> .....	19

## 5 Pin Configuration and Functions



**Figure 5-1. RGE Package, 24-Pin VQFN, Top View**

**Table 5-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NAME	QFN (RGE)		
A0	22	I	Address input 0. Connect directly to V <sub>CC</sub> or ground
A1	23	I	Address input 1. Connect directly to V <sub>CC</sub> or ground
A2	18	I	Address input 2. Connect directly to V <sub>CC</sub> or ground
GND	9	—	Ground
RESET	24	I	Active-low reset input. Connect to V <sub>CC</sub> or V <sub>DPUM</sub> <sup>(1)</sup> through a pull-up resistor, if not used
SD0	1	I/O	Serial data 0. Connect to V <sub>DPU0</sub> <sup>(1)</sup> through a pull-up resistor
SC0	2	I/O	Serial clock 0. Connect to V <sub>DPU0</sub> <sup>(1)</sup> through a pull-up resistor
SD1	3	I/O	Serial data 1. Connect to V <sub>DPU1</sub> <sup>(1)</sup> through a pull-up resistor
SC1	4	I/O	Serial clock 1. Connect to V <sub>DPU1</sub> <sup>(1)</sup> through a pull-up resistor
SD2	5	I/O	Serial data 2. Connect to V <sub>DPU2</sub> <sup>(1)</sup> through a pull-up resistor
SC2	6	I/O	Serial clock 2. Connect to V <sub>DPU2</sub> <sup>(1)</sup> through a pull-up resistor
SD3	7	I/O	Serial data 3. Connect to V <sub>DPU3</sub> <sup>(1)</sup> through a pull-up resistor
SC3	8	I/O	Serial clock 3. Connect to V <sub>DPU3</sub> <sup>(1)</sup> through a pull-up resistor
SD4	10	I/O	Serial data 4. Connect to V <sub>DPU4</sub> <sup>(1)</sup> through a pull-up resistor
SC4	11	I/O	Serial clock 4. Connect to V <sub>DPU4</sub> <sup>(1)</sup> through a pull-up resistor
SD5	12	I/O	Serial data 5. Connect to V <sub>DPU5</sub> <sup>(1)</sup> through a pull-up resistor
SC5	13	I/O	Serial clock 5. Connect to V <sub>DPU5</sub> <sup>(1)</sup> through a pull-up resistor
SD6	14	I/O	Serial data 6. Connect to V <sub>DPU6</sub> <sup>(1)</sup> through a pull-up resistor
SC6	15	I/O	Serial clock 6. Connect to V <sub>DPU6</sub> <sup>(1)</sup> through a pull-up resistor
SD7	16	I/O	Serial data 7. Connect to V <sub>DPU7</sub> <sup>(1)</sup> through a pull-up resistor
SC7	17	I/O	Serial clock 7. Connect to V <sub>DPU7</sub> <sup>(1)</sup> through a pull-up resistor
SCL	19	I/O	Serial clock bus. Connect to V <sub>DPUM</sub> <sup>(1)</sup> through a pull-up resistor
SDA	20	I/O	Serial data bus. Connect to V <sub>DPUM</sub> <sup>(1)</sup> through a pull-up resistor
VCC	21	Power	Supply voltage

(1) V<sub>DPUX</sub> is the pull-up reference voltage for the associated data line. V<sub>DPUM</sub> is the controller I<sup>2</sup>C reference voltage and V<sub>DPU0</sub>-V<sub>DPU7</sub> are the target channel reference voltages.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	7	V
I <sub>I</sub>	Input current	-20	20	mA
I <sub>O</sub>	Output current	-25		mA
I <sub>CC</sub>	Supply current	-100	100	mA
T <sub>stg</sub>	Storage temperature	-65	150	°C
T <sub>J</sub>	Max Junction Temperature	V <sub>CC</sub> ≤ 5.25 V		90 °C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-40 °C ≤ T <sub>A</sub> ≤ 85 °C		1.65 5.25 V
V <sub>IH</sub>	High-level input voltage	SCL, SDA	0.7 × V <sub>CC</sub>	6 V
		A2–A0, RESET	0.7 × V <sub>CC</sub>	V <sub>CC</sub> + 0.5
V <sub>IL</sub>	Low-level input voltage	SCL, SDA	-0.5	0.3 × V <sub>CC</sub> V
		A2–A0, RESET	-0.5	0.3 × V <sub>CC</sub>
T <sub>A</sub>	Operating free-air temperature	1.65 V ≤ V <sub>CC</sub> ≤ 5.25 V		-40 85 °C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TCA9548A	
		RGE (VQFN)	
		24 PINS	
			UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	57.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	62.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	34.4	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.8	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	34.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	15.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics<sup>(1)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT	
V <sub>PORR</sub>	Power-on reset voltage, V <sub>CC</sub> rising	No load, V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(4)</sup>			1.2	1.5	V	
V <sub>PORF</sub>	Power-on reset voltage, V <sub>CC</sub> falling <sup>(2)</sup>	No load, V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(4)</sup>		0.8	1		V	
V <sub>O(sw)</sub>	Switch output voltage	V <sub>I(sw)</sub> = V <sub>CC</sub> , I <sub>SWout</sub> = –100 μA	5 V		3.6		V	
			4.5 V to 5.25 V	2.6		4.5		
			3.3 V		1.9			
			3 V to 3.6 V	1.6		2.8		
			2.5 V		1.5			
			2.3 V to 2.7 V	1.1		2		
			1.8 V		1.1			
I <sub>OL</sub>	SDA	V <sub>OL</sub> = 0.4 V	1.65 V to 5.25 V	3	6		mA	
		V <sub>OL</sub> = 0.6 V		5	9			
I <sub>I</sub>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(4)</sup>	1.65 V to 5.25 V	–1		1	μA	
	SC7–SC0, SD7–SD0			–1		1		
	A2–A0			–1		1		
	RESET			–1		1		
I <sub>CC</sub>	Operating mode	f <sub>SCL</sub> = 400 kHz	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(4)</sup> , I <sub>O</sub> = 0	5.25 V	50	80	μA	
				3.6 V	20	35		
				2.7 V	11	20		
		1.65 V		6	10			
		f <sub>SCL</sub> = 100 kHz		5.25 V	9	30		
				3.6 V	6	15		
	2.7 V		4	8				
	Standby mode	Low inputs	V <sub>I</sub> = GND <sup>(4)</sup> , I <sub>O</sub> = 0	5.25 V	0.2	4		
				3.6 V	0.1	2		
				2.7 V	0.1	2		
		1.65 V		0.1	1			
		High inputs		V <sub>I</sub> = V <sub>CC</sub> , I <sub>O</sub> = 0	5.25 V	0.2		4
3.6 V					0.1	2		
2.7 V	0.1		2					
1.65 V	0.1	1						
ΔI <sub>CC</sub>	Supply-current change	SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V <sub>CC</sub> or GND <sup>(4)</sup>		1.65 V to 5.25 V	3	20	μA
						SCL or SDA input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND <sup>(4)</sup>	3	
C <sub>i</sub>	A2–A0	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(4)</sup>	1.65 V to 5.25 V	4	5	pF		
	RESET			4	5			
	SCL			20	28			
C <sub>io(off)</sub> <sup>(3)</sup>	SDA	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(4)</sup> , Switch OFF	1.65 V to 5.25 V	20	28	pF		
	SC7–SC0, SD7–SD0			5.5	7.5			
R <sub>ON</sub>	Switch-on resistance	V <sub>O</sub> = 0.4 V, I <sub>O</sub> = 15 mA	4.5 V to 5.25 V	4	10	25	Ω	
			3 V to 3.6 V	5	12	35		
		V <sub>O</sub> = 0.4 V, I <sub>O</sub> = 10 mA	2.3 V to 2.7 V	7	15	45		
			1.65 V to 1.95 V	10	25	70		

(1) For operation between specified voltage ranges, refer to the worst-case parameter in both applicable ranges.

(2) The power-on reset circuit resets the I<sup>2</sup>C bus logic with V<sub>CC</sub> < V<sub>PORF</sub>.

(3) C<sub>io(ON)</sub> depends on internal capacitance and external capacitance added to the SCn lines when channel(s) are ON.

(4) RESET = V<sub>CC</sub> (held high) when all other input voltages, V<sub>I</sub> = GND.

## 6.6 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

		MIN	MAX	UNIT
<b>STANDARD MODE</b>				
$f_{scl}$	I <sup>2</sup> C clock frequency	0	100	kHz
$t_{sch}$	I <sup>2</sup> C clock high time	4		μs
$t_{scl}$	I <sup>2</sup> C clock low time	4.7		μs
$t_{sp}$	I <sup>2</sup> C spike time		50	ns
$t_{sds}$	I <sup>2</sup> C serial-data setup time	250		ns
$t_{sdh}$	I <sup>2</sup> C serial-data hold time	0 <sup>(1)</sup>		μs
$t_{icr}$	I <sup>2</sup> C input rise time		1000	ns
$t_{icf}$	I <sup>2</sup> C input fall time		300	ns
$t_{ocf}$	I <sup>2</sup> C output (SDn) fall time (10 pF to 400 pF bus)		300	ns
$t_{buf}$	I <sup>2</sup> C bus free time between stop and start	4.7		μs
$t_{sts}$	I <sup>2</sup> C start or repeated start condition setup	4.7		μs
$t_{sth}$	I <sup>2</sup> C start or repeated start condition hold	4		μs
$t_{sps}$	I <sup>2</sup> C stop condition setup	4		μs
$t_{vdL(Data)}$	Valid-data time (high to low) <sup>(2)</sup>	SCL low to SDA output low valid	1	μs
$t_{vdH(Data)}$	Valid-data time (low to high) <sup>(2)</sup>	SCL low to SDA output high valid	0.6	μs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low	1	μs
$C_b$	I <sup>2</sup> C bus capacitive load		400	pF
<b>FAST MODE</b>				
$f_{scl}$	I <sup>2</sup> C clock frequency	0	400	kHz
$t_{sch}$	I <sup>2</sup> C clock high time	0.6		μs
$t_{scl}$	I <sup>2</sup> C clock low time	1.3		μs
$t_{sp}$	I <sup>2</sup> C spike time		50	ns
$t_{sds}$	I <sup>2</sup> C serial-data setup time	100		ns
$t_{sdh}$	I <sup>2</sup> C serial-data hold time	0 <sup>(1)</sup>		μs
$t_{icr}$	I <sup>2</sup> C input rise time	20	300	ns
$t_{icf}$	I <sup>2</sup> C input fall time	$20 \times (V_{CC} / 5.5 \text{ V})$	300	ns
$t_{ocf}$	I <sup>2</sup> C output (SDn) fall time (10 pF to 400 pF bus)	$20 \times (V_{CC} / 5.5 \text{ V})$	300	ns
$t_{buf}$	I <sup>2</sup> C bus free time between stop and start	1.3		μs
$t_{sts}$	I <sup>2</sup> C start or repeated start condition setup	0.6		μs
$t_{sth}$	I <sup>2</sup> C start or repeated start condition hold	0.6		μs
$t_{sps}$	I <sup>2</sup> C stop condition setup	0.6		μs
$t_{vdL(Data)}$	Valid-data time (high to low) <sup>(2)</sup>	SCL low to SDA output low valid	1	μs
$t_{vdH(Data)}$	Valid-data time (low to high) <sup>(2)</sup>	SCL low to SDA output high valid	0.6	μs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low	1	μs
$C_b$	I <sup>2</sup> C bus capacitive load		400	pF

(1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to the  $V_{IH}$  min of the SCL signal), to bridge the undefined region of the falling edge of SCL.

(2) Data taken using a 1 kΩ pull-up resistor and 50 pF load (see [Figure 7-2](#))

## 6.7 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{W(L)}$	Pulse duration, $\overline{\text{RESET}}$ low	6		ns
$t_{\text{REC(STA)}}$	Recovery time from $\overline{\text{RESET}}$ to start	0		ns

## 6.8 Switching Characteristics

over recommended operating free-air temperature range,  $C_L \leq 100$  pF (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER			FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}^{(1)}$	Propagation delay time	$R_{ON} = 20 \Omega, C_L = 15$ pF	SDA or SCL	SDn or SCn		0.3	ns
		$R_{ON} = 20 \Omega, C_L = 50$ pF				1	
$t_{rst}^{(2)}$	RESET time (SDA clear)		RESET	SDA		500	ns

- (1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- (2)  $t_{rst}$  is the propagation delay measured from the time the  $\overline{\text{RESET}}$  pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of  $t_{W(L)}$ .

### 6.9 Typical Characteristics

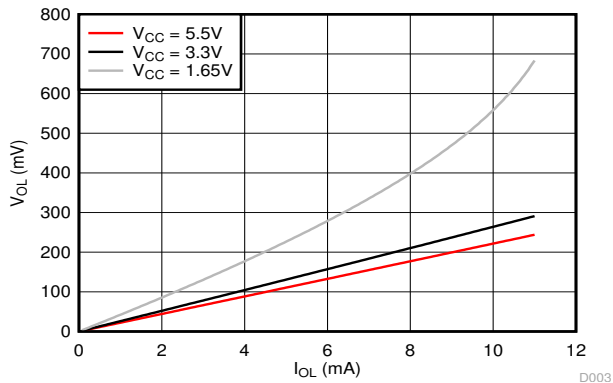


Figure 6-1. SDA Output Low Voltage ( $V_{OL}$ ) vs Load Current ( $I_{OL}$ ) at Three  $V_{CC}$  Levels

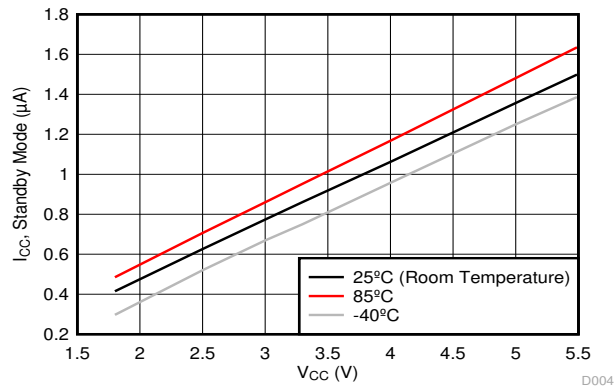


Figure 6-2. Standby Current ( $I_{CC}$ ) vs Supply Voltage ( $V_{CC}$ ) at three temperatures

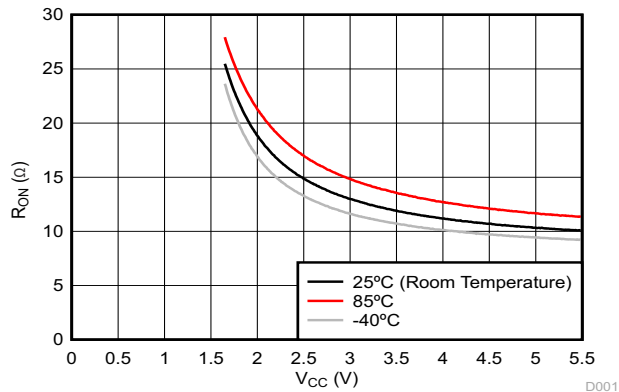
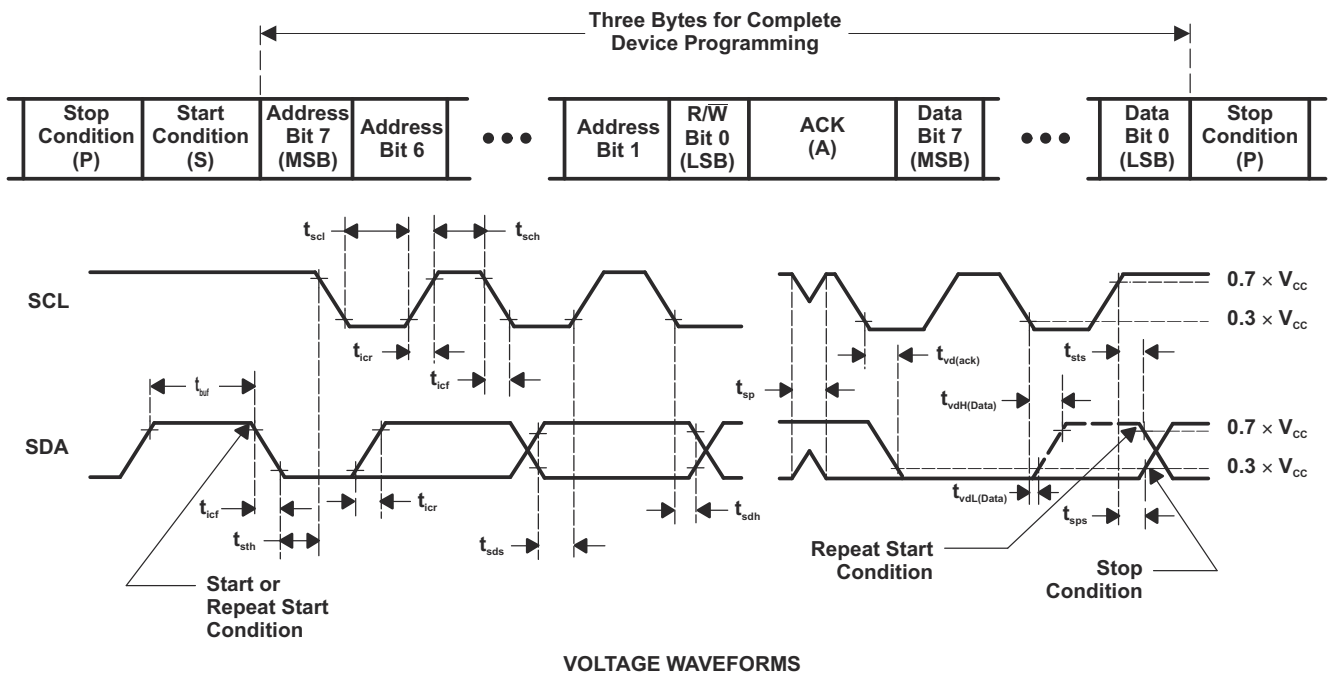
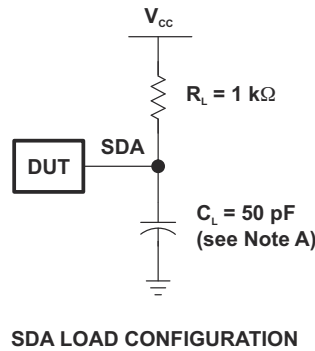


Figure 6-3. On-Resistance ( $R_{ON}$ ) vs Supply Voltage ( $V_{CC}$ ) at three temperatures



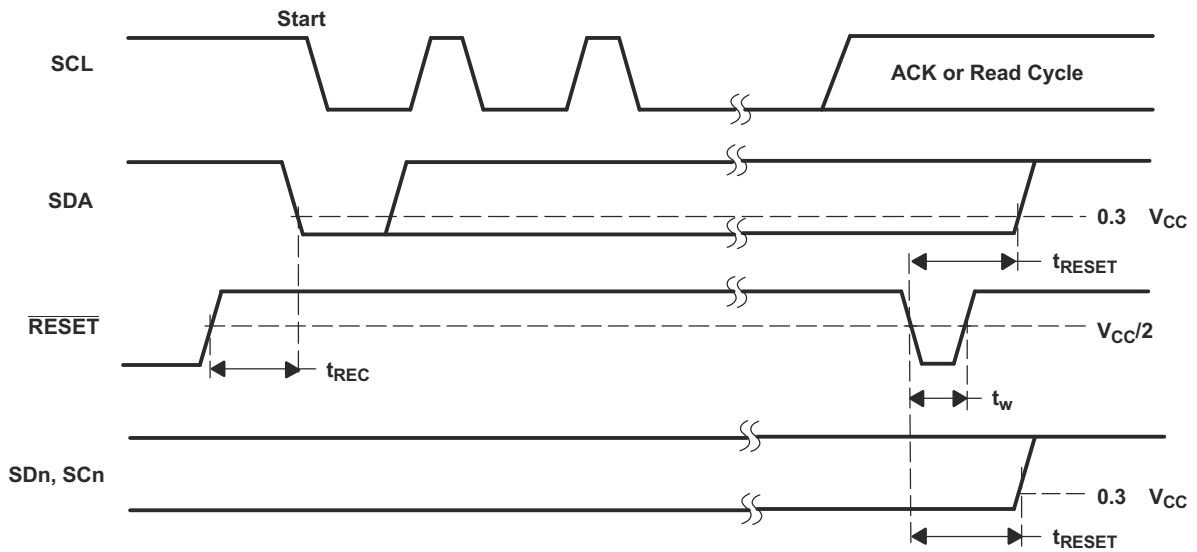
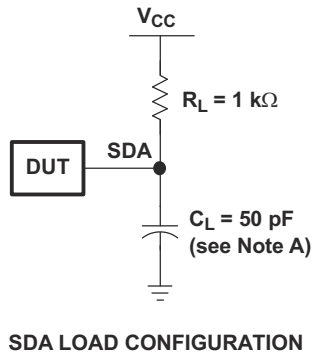
## 7 Parameter Measurement Information



BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2, 3	P-port data

- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_0 = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. Not all parameters and waveforms are applicable to all devices.

**Figure 7-1. I<sup>2</sup>C Load Circuit and Voltage Waveforms**



- A. C<sub>L</sub> includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub>/t<sub>f</sub> ≤ 30 ns.
- C. I/Os are configured as inputs.
- D. Not all parameters and waveforms are applicable to all devices.

**Figure 7-2. Reset Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

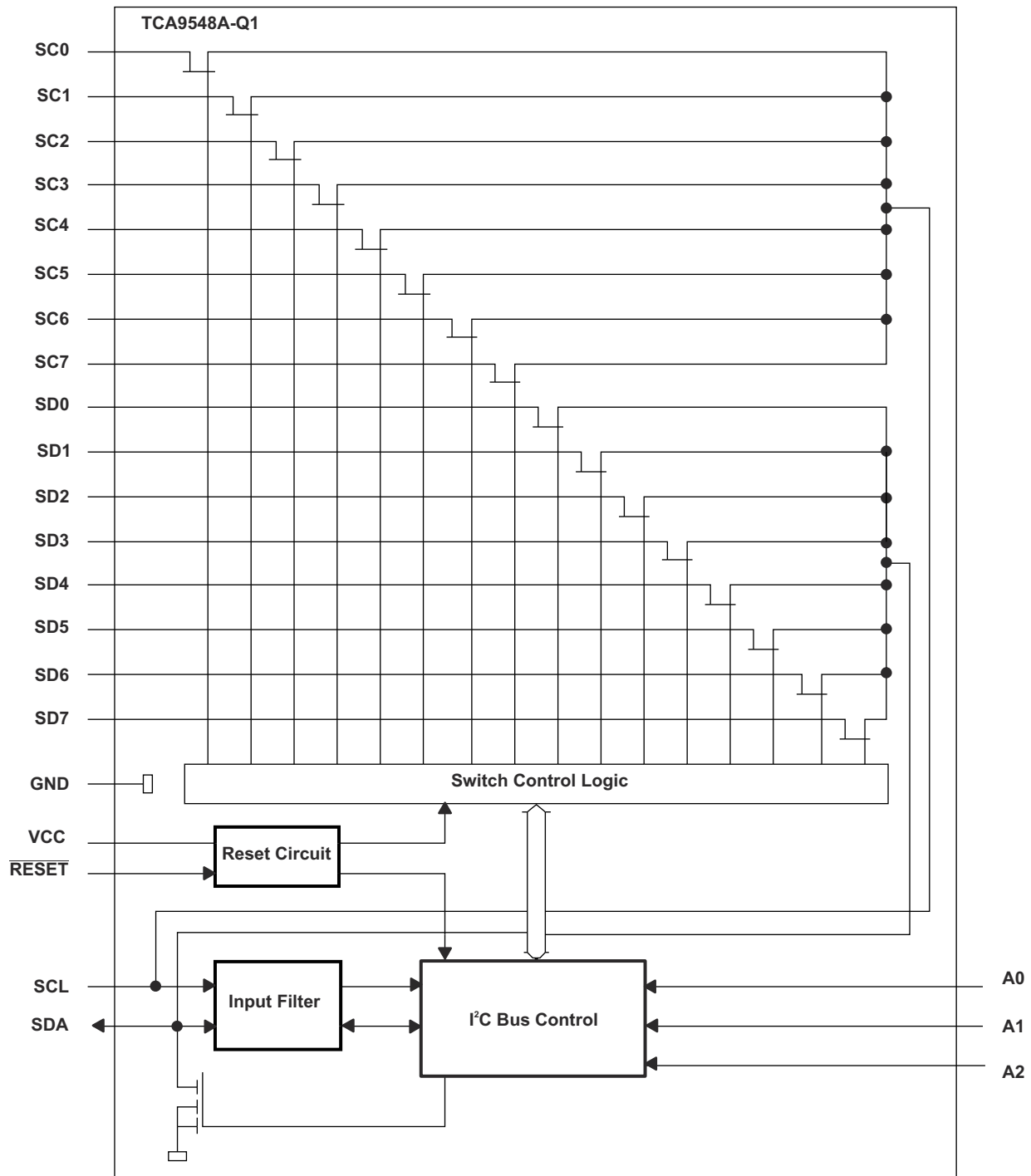
The TCA9548A-Q1 is an 8-channel, bidirectional translating I<sup>2</sup>C switch. The controller SCL/SDA signal pair is directed to eight channels of target devices, SC0/SD0-SC7/SD7. Any individual downstream channel can be selected as well as any combination of the eight channels.

The device offers an active-low  $\overline{\text{RESET}}$  input which resets the state machine and allows the TCA9548A-Q1 to recover if one of the downstream I<sup>2</sup>C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V<sub>CC</sub>, also known as a power-on reset (POR). Both the  $\overline{\text{RESET}}$  function and a POR cause all channels to be deselected.

The connections of the I<sup>2</sup>C data path are controlled by the same I<sup>2</sup>C controller device that is switched to communicate with multiple I<sup>2</sup>C targets. After the successful acknowledgment of the target address (hardware selectable by A0, A1, and A2 pins), a single 8-bit control register is written to or read from to determine the selected channels.

The TCA9548A-Q1 may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8 V, 2.5 V, or 3.3 V parts can communicate with 5 V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the controller and each target channel.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

The TCA9548A-Q1 is an 8-channel, bidirectional translating switch for I<sup>2</sup>C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The TCA9548A-Q1 features I<sup>2</sup>C control using a single 8-bit control register in which each bit controls the enabling and disabling of one of the corresponding 8 switch channels for I<sup>2</sup>C data flow. Depending on the application, voltage translation of the I<sup>2</sup>C bus can also be achieved using the TCA9548A-Q1 to allow 1.8 V, 2.5 V, or 3.3 V parts to communicate with 5 V parts. Additionally, in the event that communication on the I<sup>2</sup>C bus enters a fault state, the TCA9548A-Q1 can be reset to resume normal operation using the  $\overline{\text{RESET}}$  pin feature or by a power-on reset which results from cycling power to the device.

## 8.4 Device Functional Modes

### 8.4.1 RESE $\bar{T}$ Input

The RESE $\bar{T}$  input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of  $t_{WL}$ , the TCA9548A-Q1 resets its registers and I<sup>2</sup>C state machine and deselects all channels. The RESE $\bar{T}$  input must be connected to V<sub>CC</sub> through a pull-up resistor.

### 8.4.2 Power-On Reset

When power is applied to the VCC pin, an internal power-on reset holds the TCA9548A-Q1 in a reset condition until V<sub>CC</sub> has reached V<sub>PORR</sub>. At this point, the reset condition is released, and the TCA9548A-Q1 registers and I<sup>2</sup>C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V<sub>CC</sub> must be lowered below V<sub>PORF</sub> to reset the device.

## 8.5 Programming

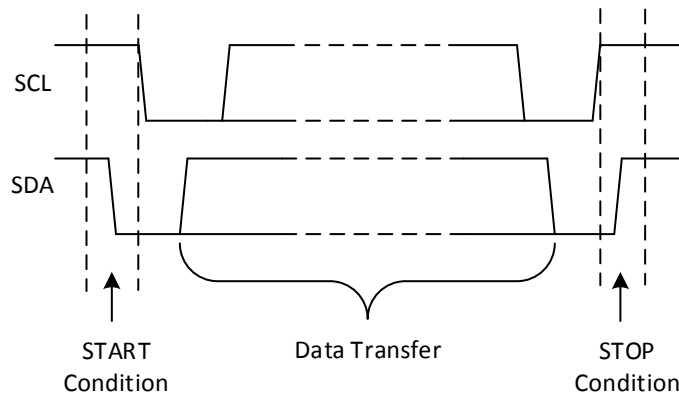
### 8.5.1 I<sup>2</sup>C Interface

The TCA9548A-Q1 has a standard bidirectional I<sup>2</sup>C interface that is controlled by a controller device in order to be configured or read the status of this device. Each target on the I<sup>2</sup>C bus has a specific device address to differentiate between other target devices that are on the same I<sup>2</sup>C bus. Many target devices require configuration upon startup to set the behavior of the device. This is typically done when the controller accesses internal register maps of the target, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read.

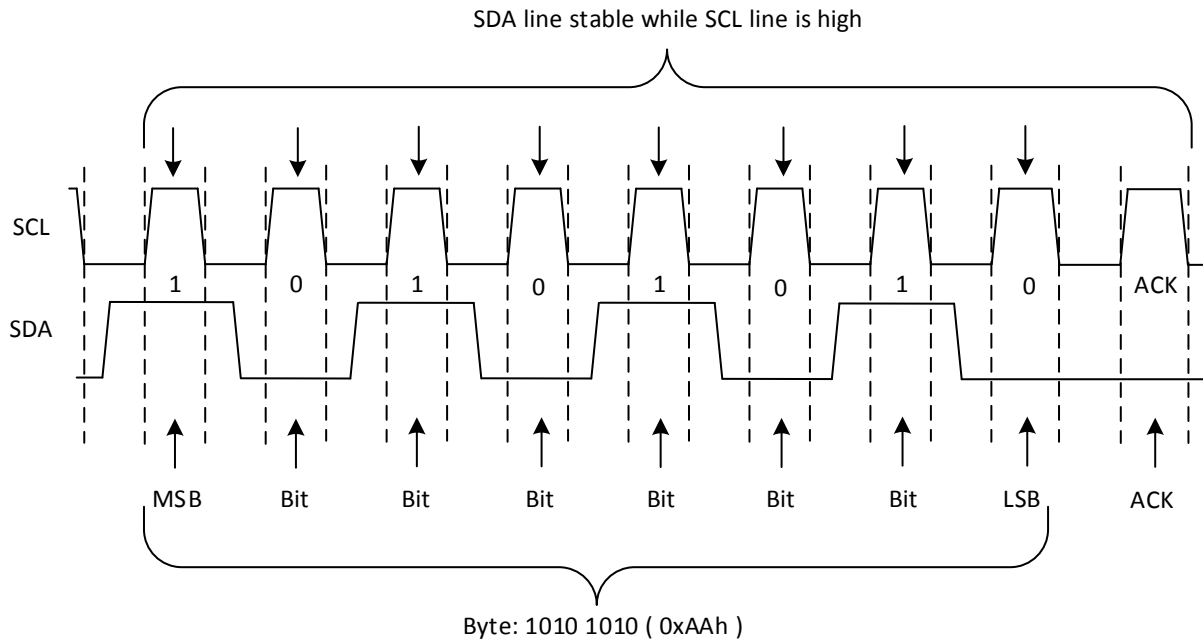
The physical I<sup>2</sup>C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V<sub>CC</sub> through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I<sup>2</sup>C lines. (For further details, see the [I<sup>2</sup>C Pull-up Resistor Calculation](#) application report. Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition (See [Figure 8-1](#) and [Figure 8-2](#)).

The following is the general procedure for a controller to access a target device:

1. If a controller wants to send data to a target:
  - Controller-transmitter sends a START condition and addresses the target-receiver.
  - Controller-transmitter sends data to target-receiver.
  - Controller-transmitter terminates the transfer with a STOP condition.
2. If a controller wants to receive or read data from a target:
  - Controller-receiver sends a START condition and addresses the target-transmitter.
  - Controller-receiver sends the requested register to read to target-transmitter.
  - Controller-receiver receives data from the target-transmitter.
  - Controller-receiver terminates the transfer with a STOP condition.



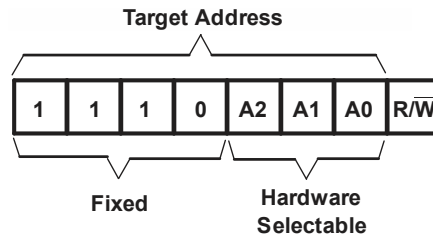
**Figure 8-1. Definition of Start and Stop Conditions**



**Figure 8-2. Bit Transfer**

### 8.5.2 Device Address

Figure 8-3 shows the address byte of the TCA9548A-Q1.



**Figure 8-3. TCA9548A-Q1 Address**

The last bit of the target address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

Table 8-1 shows the TCA9548A-Q1 address reference.

**Table 8-1. Address Reference**

INPUTS			I <sup>2</sup> C BUS TARGET ADDRESS
A2	A1	A0	
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

### 8.5.3 Bus Transactions

Data must be sent to and received from the target devices, and this is accomplished by reading from or writing to registers in the target device.

Registers are locations in the memory of the target which contain information, whether it be the configuration information or some sampled data to send back to the controller. The controller must write information to these registers in order to instruct the target device to perform a task.

While it is common to have registers in I<sup>2</sup>C targets, note that not all target devices have registers. Some devices are simple and contain only 1 register, which may be written to directly by sending the register data immediately after the target address, instead of addressing a register. The TCA9548A-Q1 is example of a single-register device, which is controlled via I<sup>2</sup>C commands. Since it has 1 bit to enable or disable a channel, there is only 1 register needed, and the controller merely writes the register data after the target address, skipping the register number.

#### 8.5.3.1 Writes

To write on the I<sup>2</sup>C bus, the controller sends a START condition on the bus with the address of the target, as well as the last bit (the R/  $\bar{W}$  bit) set to 0, which signifies a write. The target acknowledges, letting the controller know it is ready. After this, the controller starts sending the control register data to the target until the controller has sent all the data necessary (which is sometimes only a single byte), and the controller terminates the transmission with a STOP condition.

There is no limit to the number of bytes sent, but the last byte sent is what is in the register.

Figure 8-4 shows an example of writing a single byte to a target register.

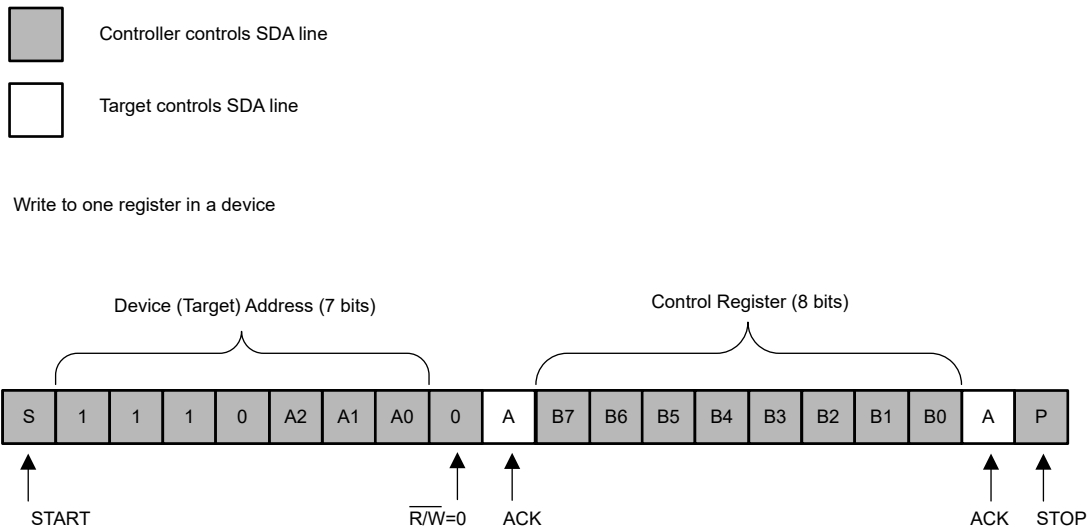


Figure 8-4. Write to Register

#### 8.5.3.2 Reads

Reading from a target is very similar to writing, but the controller sends a START condition, followed by the target address with the R/  $\bar{W}$  bit set to 1 (signifying a read). The target acknowledges the read request, and the controller releases the SDA bus but continues supplying the clock to the target. During this part of the transaction, the controller becomes the controller-receiver, and the target becomes the target-transmitter.

The controller continues to send out the clock pulses, but releases the SDA line so that the target can transmit data. At the end of every byte of data, the controller sends an ACK to the target, letting the target know that it is ready for more data. Once the controller has received the number of bytes it is expecting, it sends a NACK, signaling to the target to halt communications and release the bus. The controller follows this up with a STOP condition.

Figure 8-5 shows an example of reading a single byte from a target register.

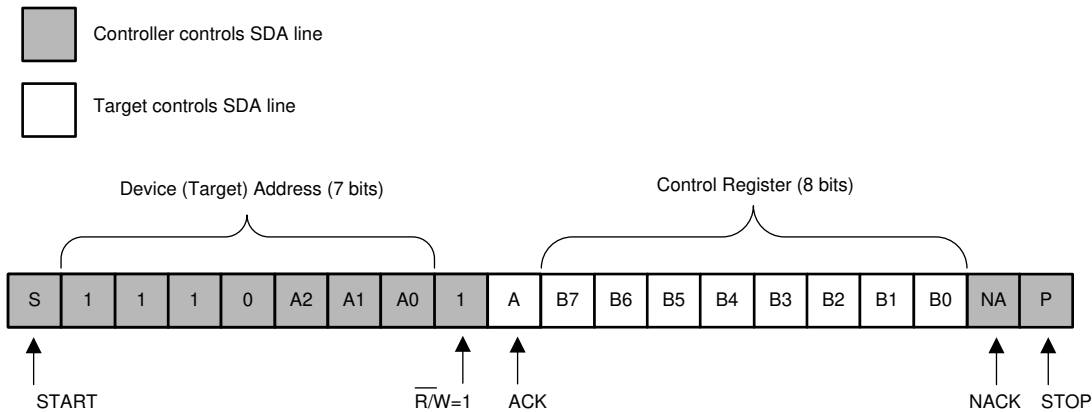


Figure 8-5. Read from Control Register

### 8.5.4 Control Register

Following the successful acknowledgment of the address byte, the bus controller sends a command byte that is stored in the control register in the TCA9548A-Q1 (see Figure 8-6). This register can be written and read via the I<sup>2</sup>C bus. Each bit in the command byte corresponds to a SCn/SDn channel and a high (or 1) selects this channel. Multiple SCn/SDn channels may be selected at the same time. When a channel is selected, the channel becomes active after a stop condition has been placed on the I<sup>2</sup>C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur immediately after the acknowledge cycle. If multiple bytes are received by the TCA9548A-Q1, it saves the last byte received.

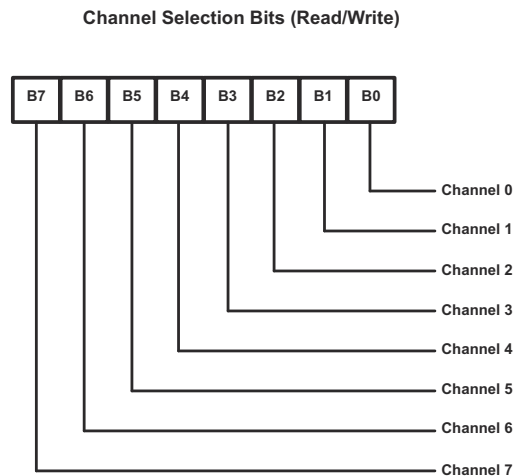


Figure 8-6. Control Register



Table 8-2 shows the TCA9548A-Q1 Command Byte Definition.

**Table 8-2. Command Byte Definition**

CONTROL REGISTER BITS								COMMAND
B7	B6	B5	B4	B3	B2	B1	B0	
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	X	0	Channel 1 disabled
							1	Channel 1 enabled
X	X	X	X	X	X	X	0	Channel 2 disabled
							1	Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
				1				Channel 3 enabled
X	X	X	0	X	X	X	X	Channel 4 disabled
			1					Channel 4 enabled
X	X	0	X	X	X	X	X	Channel 5 disabled
		1						Channel 5 enabled
X	0	X	X	X	X	X	X	Channel 6 disabled
	1							Channel 6 enabled
0	X	X	X	X	X	X	X	Channel 7 disabled
1								Channel 7 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up/reset default state

### 8.5.5 $\overline{\text{RESET}}$ Input

The  $\overline{\text{RESET}}$  input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of  $t_{\text{WL}}$ , the TCA9548A-Q1 resets its registers and I<sup>2</sup>C state machine and deselects all channels. The  $\overline{\text{RESET}}$  input must be connected to  $V_{\text{CC}}$  through a pull-up resistor.

### 8.5.6 Power-On Reset

When power (from 0 V) is applied to  $V_{\text{CC}}$ , an internal power-on reset holds the TCA9548A-Q1 in a reset condition until  $V_{\text{CC}}$  has reached  $V_{\text{POR}}$ . At that point, the reset condition is released and the TCA9548A-Q1 registers and I<sup>2</sup>C state machine initialize to their default states. After that,  $V_{\text{CC}}$  must be lowered to below  $V_{\text{POR}}$  and then back up to the operating voltage for a power-reset cycle.

## Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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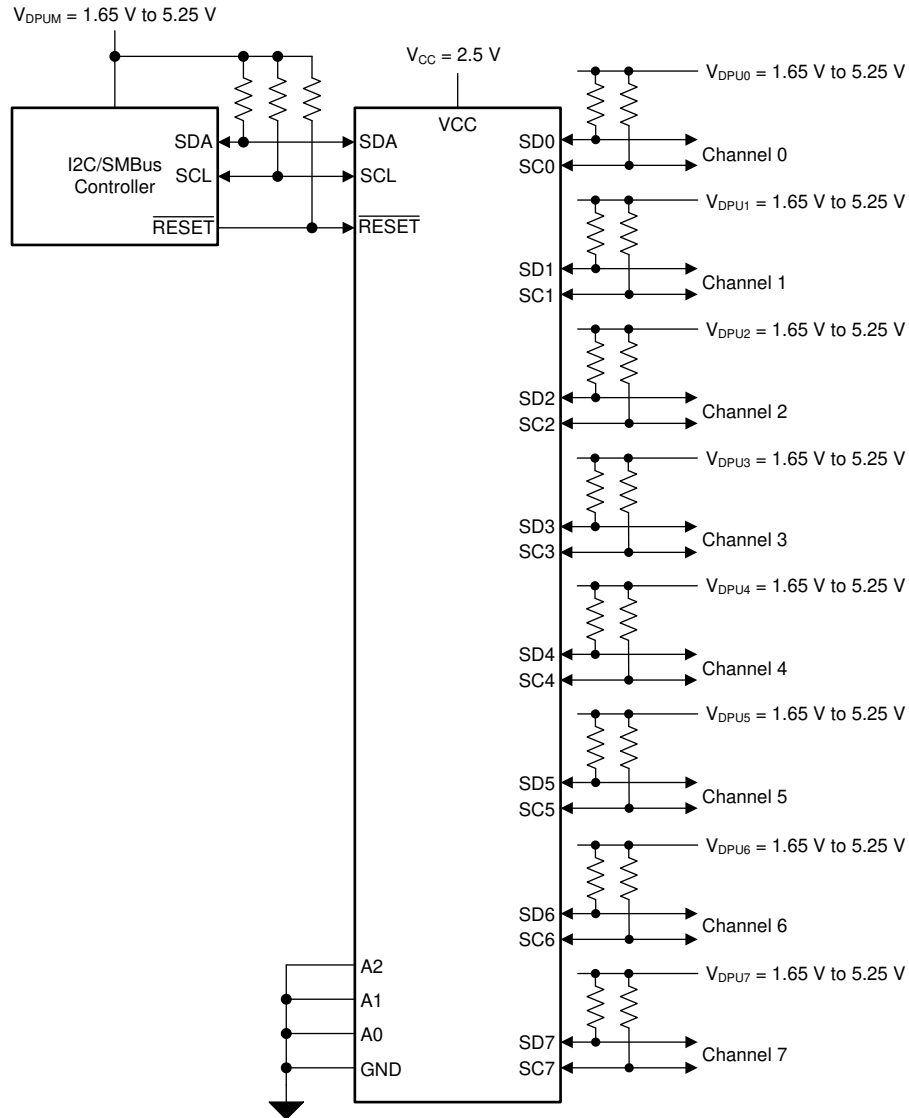
### 9.1 Application Information

Applications of the TCA9548A-Q1 contain an I<sup>2</sup>C (or SMBus) controller device and up to eight I<sup>2</sup>C target devices. The downstream channels are ideally used to resolve I<sup>2</sup>C target address conflicts. For example, if eight identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0-7. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I<sup>2</sup>C controller can move on and read the next channel.

In an application where the I<sup>2</sup>C bus contains many additional target devices that do not result in I<sup>2</sup>C target address conflicts, these target devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches are enabled simultaneously, additional design requirements must be considered (see the [Design Requirements](#) section and [Detailed Design Procedure](#) section).

## 9.2 Typical Application

Figure 9-1 shows an application in which the TCA9548A-Q1 can be used.



**Figure 9-1. Typical Application Schematic**

### 9.2.1 Design Requirements

A typical application of the TCA9548A-Q1 contains one or more data pull-up voltages,  $V_{DPUX}$ , one for the controller device ( $V_{DPUM}$ ) and one for each of the selectable target channels ( $V_{DPU0} - V_{DPU7}$ ). In the event where the controller device and all target devices operate at the same voltage, then  $V_{DPUM} = V_{DPUX} = V_{CC}$ . In an application where voltage translation is necessary, additional design requirements must be considered to determine an appropriate  $V_{CC}$  voltage.

The A0, A1, and A2 pins are hardware selectable to control the target address of the TCA9548A-Q1. These pins may be tied directly to GND or  $V_{CC}$  in the application.

If multiple target channels are activated simultaneously in the application, then the total  $I_{OL}$  from SCL/SDA to GND on the controller side is the sum of the currents through all pull-up resistors,  $R_p$ .

The pass-gate transistors of the TCA9548A-Q1 are constructed such that the  $V_{CC}$  voltage can be used to limit the maximum voltage that is passed from one I<sup>2</sup>C bus to another.

Figure 9-2 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the [Electrical Characteristics](#) table). In order for the TCA9548A-Q1 to act as a voltage translator, the  $V_{pass}$  voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V,  $V_{pass}$  must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 9-2,  $V_{pass(max)}$  is 2.7 V when the TCA9548A-Q1 supply voltage is 4 V or lower, so the TCA9548A-Q1 supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 9-1).

### 9.2.2 Detailed Design Procedure

Once all the targets are assigned to the appropriate target channels and bus voltages are identified, the pull-up resistors,  $R_p$ , for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of  $V_{DPUX}$ ,  $V_{OL(max)}$ , and  $I_{OL}$  as shown in Equation 1:

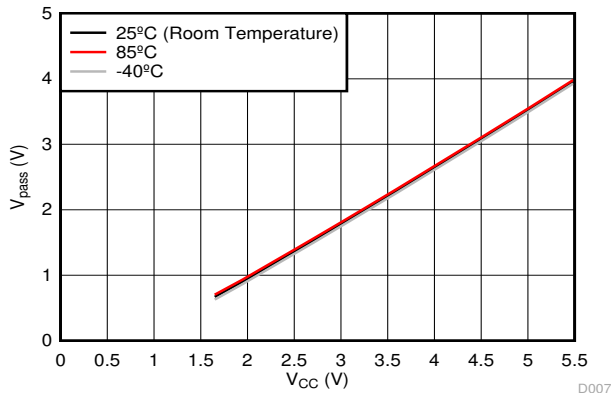
$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$  as shown in Equation 2:

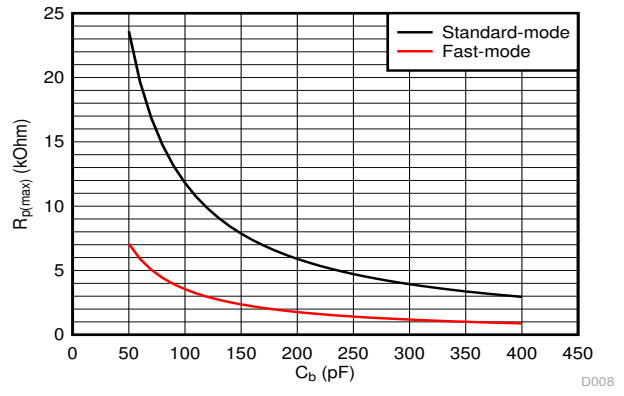
$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9548A-Q1,  $C_{io(OFF)}$ , the capacitance of wires, connections and traces, and the capacitance of each individual target on a given channel. If multiple channels are activated simultaneously, each of the targets on all channels contribute to total bus capacitance.

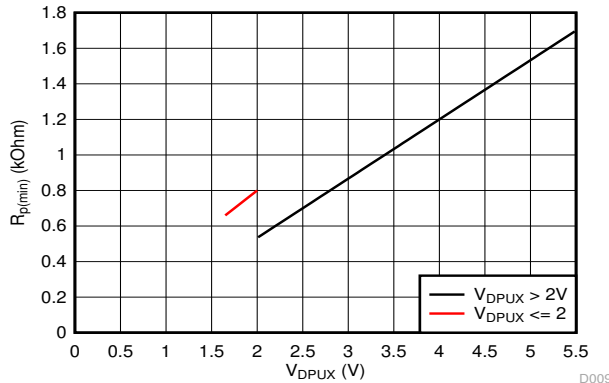
### 9.2.3 Application Curves



**Figure 9-2. Pass-Gate Voltage ( $V_{pass}$ ) vs Supply Voltage ( $V_{CC}$ ) at Three Temperature Points**



**Figure 9-3. Maximum Pull-up Resistance ( $R_{p(max)}$ ) vs Bus Capacitance ( $C_b$ )**



$V_{OL} = 0.2 \times V_{DPUX}$ ,  $I_{OL} = 2 \text{ mA}$  when  $V_{DPUX} \leq 2 \text{ V}$   
 $V_{OL} = 0.4 \text{ V}$ ,  $I_{OL} = 3 \text{ mA}$  when  $V_{DPUX} > 2 \text{ V}$

**Figure 9-4. Minimum Pull-up Resistance ( $R_{p(min)}$ ) vs Pull-up Reference Voltage ( $V_{DPUX}$ )**

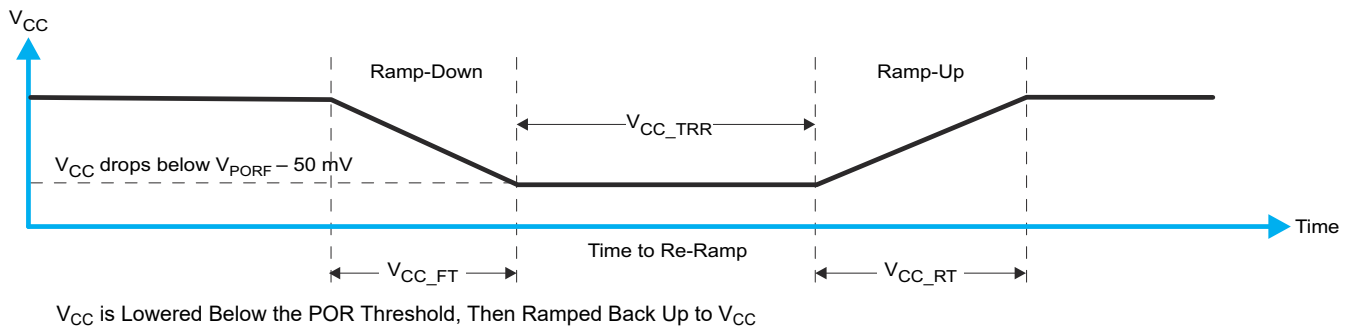
## Power Supply Recommendations

The operating power-supply voltage range of the TCA9548A-Q1 is 1.65 V to 5.25 V applied at the VCC pin. When the TCA9548A-Q1 is powered on for the first time or anytime the device must be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I<sup>2</sup>C bus logic is initialized properly.

### 9.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9548A-Q1 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

A power-on reset is shown in [Figure 9-1](#).



**Figure 9-1. Power-On Reset Waveform**

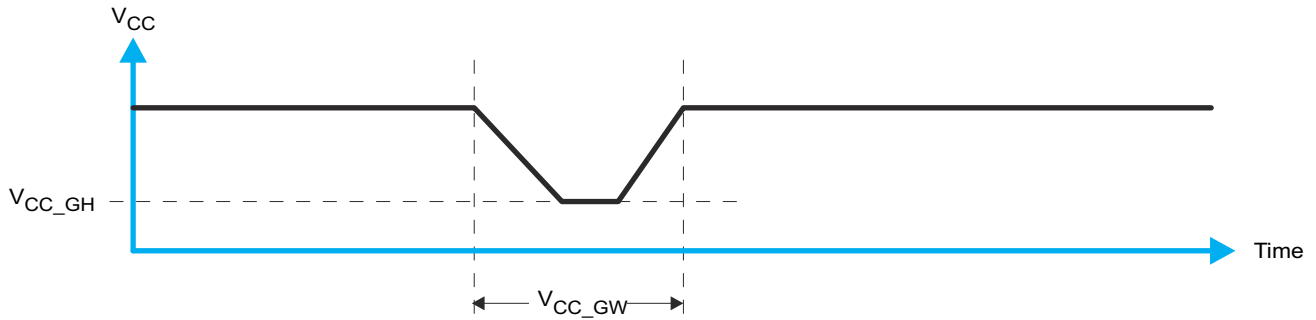
[Table 9-1](#) specifies the performance of the power-on reset feature for TCA9548A-Q1 for both types of power-on reset.

**Table 9-1. Recommended Supply Sequencing and Ramp Rates<sup>(1)</sup>**

PARAMETER			MIN	MAX	UNIT
V <sub>CC_FT</sub>	Fall time	See <a href="#">Figure 9-1</a>	1	100	ms
V <sub>CC_RT</sub>	Rise time	See <a href="#">Figure 9-1</a>	0.1	100	ms
V <sub>CC_TRR</sub>	Time to re-ramp (when V <sub>CC</sub> drops below V <sub>PORF(min)</sub> – 50 mV or when V <sub>CC</sub> drops to GND)	See <a href="#">Figure 9-1</a>	40		μs
V <sub>CC_GH</sub>	Level that V <sub>CC</sub> can glitch down to, but not cause a functional disruption when V <sub>CC_GW</sub> = 1 μs	See <a href="#">Figure 9-2</a>		1.2	V
V <sub>CC_GW</sub>	Glitch width that does not cause a functional disruption when V <sub>CC_GH</sub> = 0.5 × V <sub>CC</sub>	See <a href="#">Figure 9-2</a>		10	μs

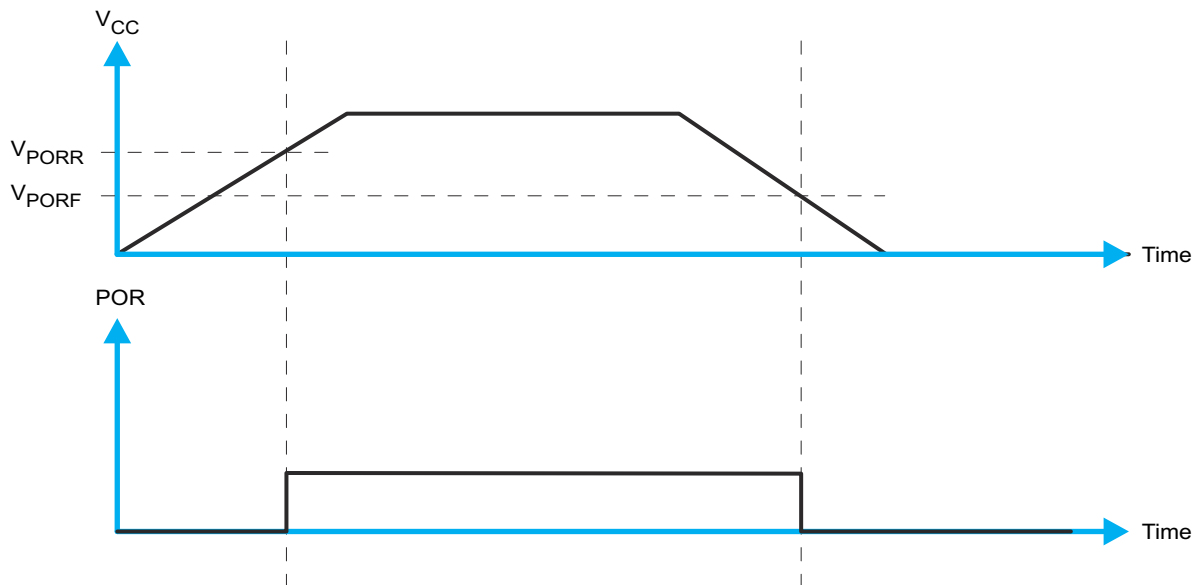
(1) All supply sequencing and ramp rate values are measured at T<sub>A</sub> = 25°C

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V<sub>CC\_GW</sub>) and height (V<sub>CC\_GH</sub>) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Figure 9-2](#) and [Table 9-1](#) provide more information on how to measure these specifications.



**Figure 9-2. Glitch Width and Glitch Height**

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. Figure 9-3 and Table 9-1 provide more details on this specification.



**Figure 9-3.  $V_{POR}$  Example**

## 9 Layout

### 9.1 Layout Guidelines

For PCB layout of the TCA9548A-Q1, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and pins that are connected to ground must have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. Bypass and decoupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V<sub>DPUX</sub> voltages and V<sub>CC</sub> could be at the same potential and a single copper plane could connect all of the pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V<sub>DPU0</sub> and V<sub>DPU0</sub> – V<sub>DPU7</sub>, may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I<sup>2</sup>C bus capacitance added by PCB parasitics, data lines (SC<sub>n</sub> and SD<sub>n</sub>) must be as short as possible and the widths of the traces must also be minimized (for example, 5-10 mils depending on copper weight).

### 9.2 Layout Example

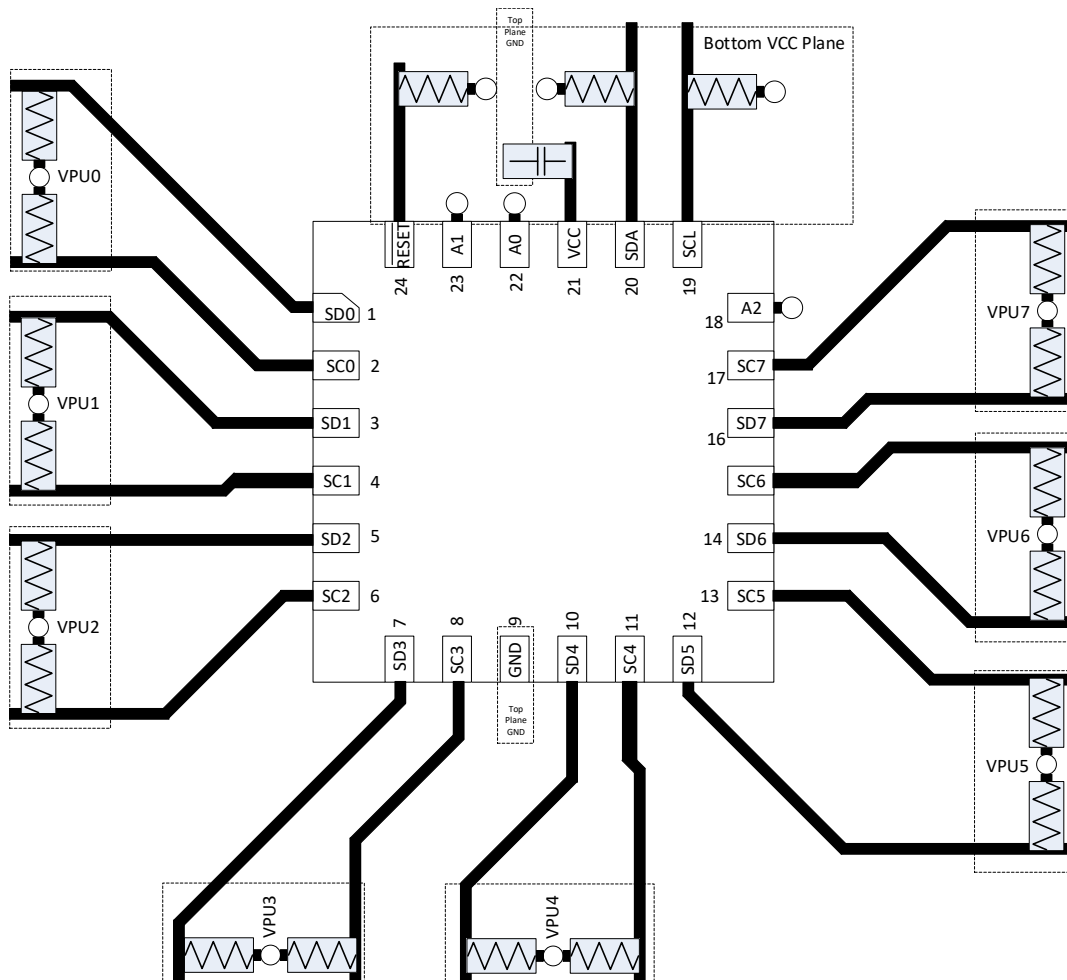


Figure 9-1. Layout Schematic



## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation see the following:

- [I2C Bus Pull-Up Resistor Calculation](#)
- [Maximum Clock Frequency of I2C Bus Using Repeaters](#)
- [Introduction to Logic](#)
- [Understanding the I2C Bus](#)
- [Choosing the Correct I2C Device for New Designs](#)
- [TCA9548AEVM User's Guide](#)

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9548ARGERQ1	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	T9548A	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TCA9548A-Q1 :**

- Catalog : [TCA9548A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9548ARGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9548ARGERQ1	VQFN	RGE	24	3000	367.0	367.0	35.0

## GENERIC PACKAGE VIEW

RGE 24

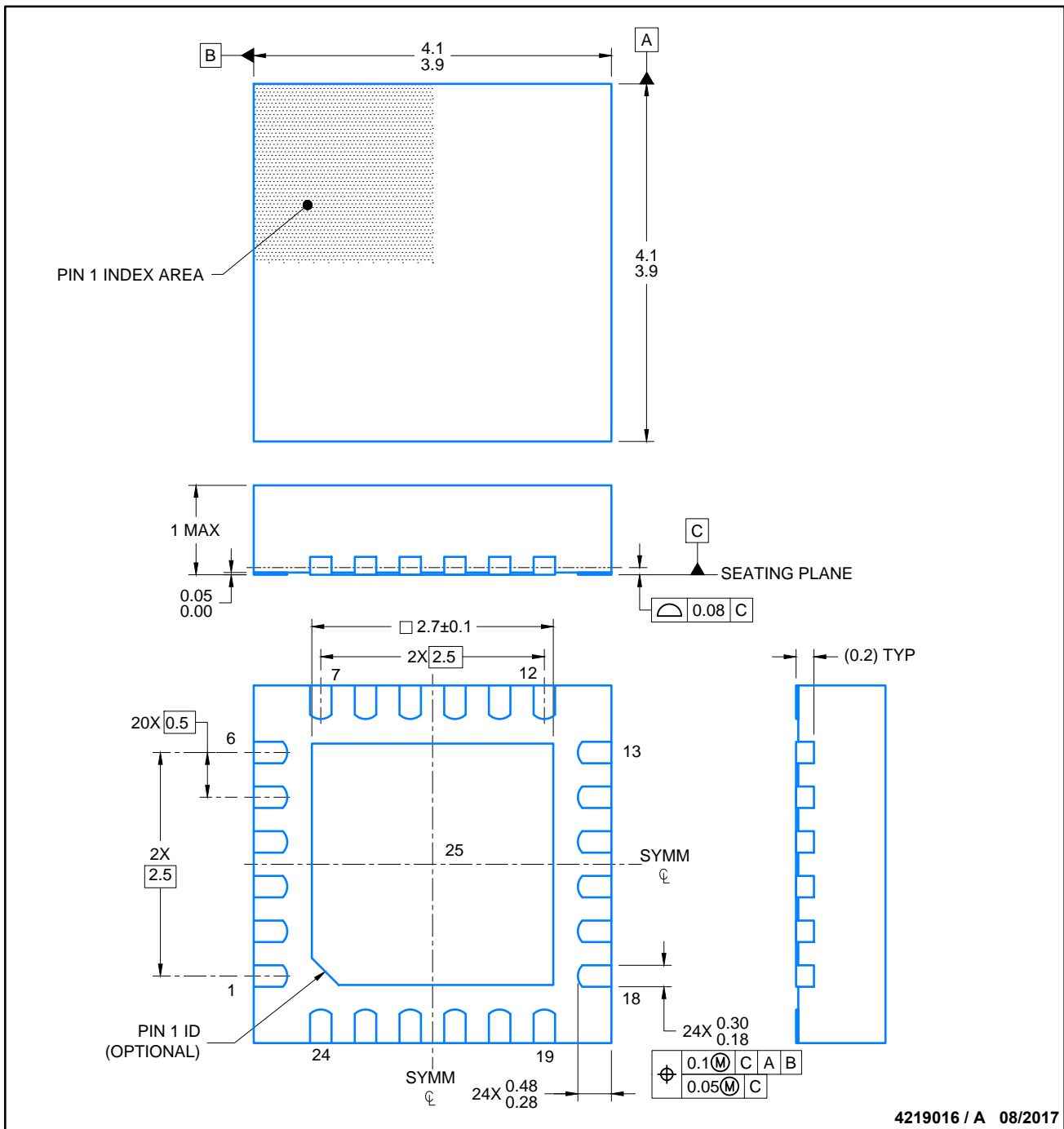
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

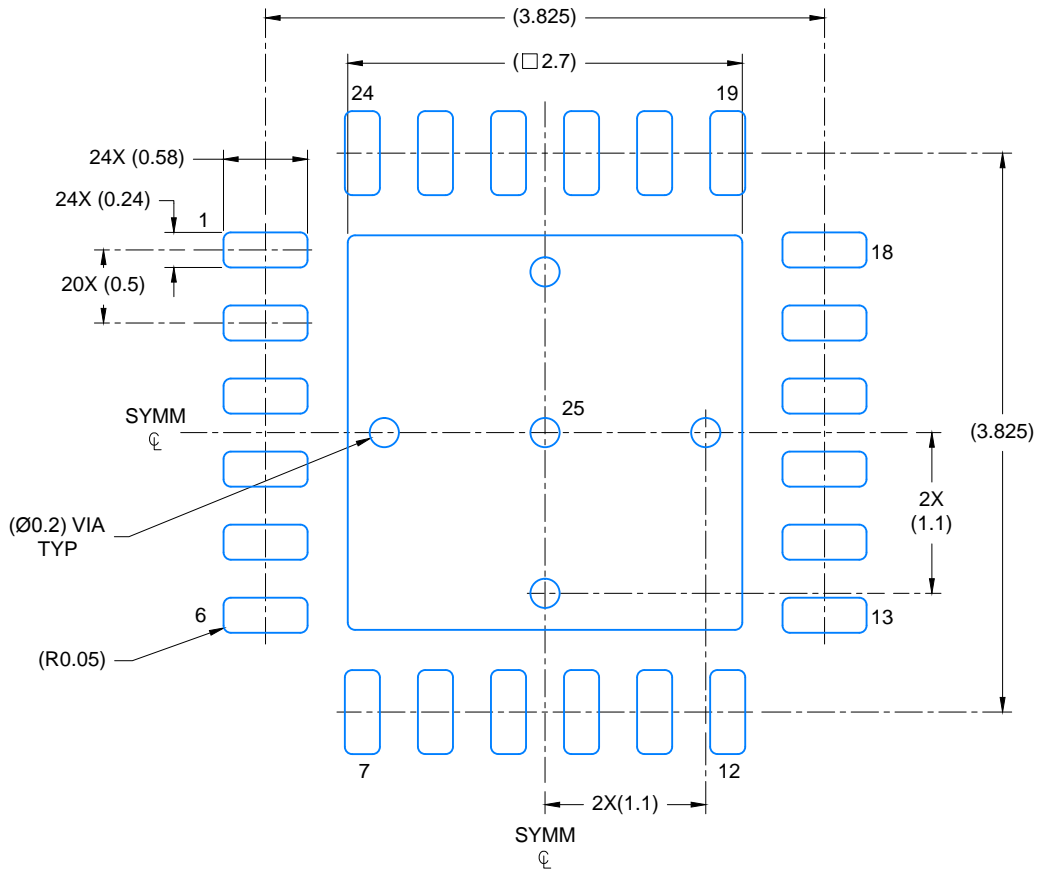
4204104/H



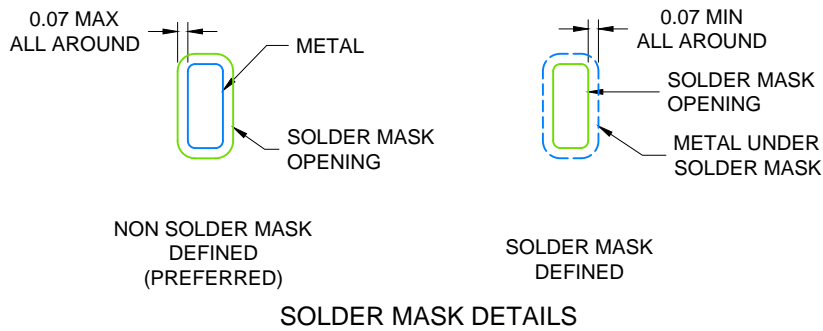
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE  
SCALE: 20X

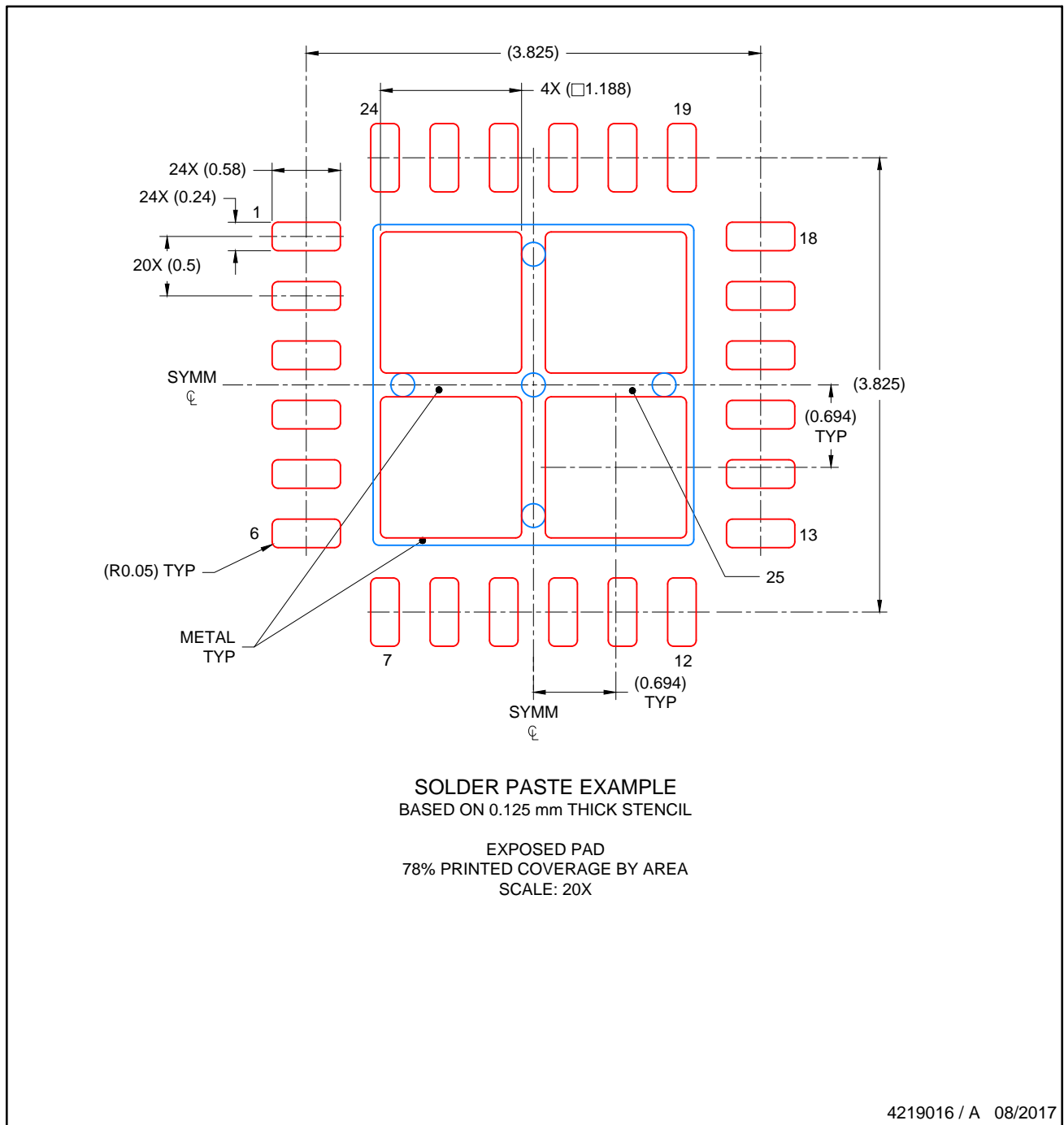


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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





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NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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