Kintex UltraScale & Virtex UltraScale FPGA Speed Specification Changes

XCN16031 (v1.0) December 20, 2016 Product Change Notice – For Your Information

Overview

Thank you for designing with the Xilinx Kintex® UltraScale™ and Virtex® UltraScale™ FPGA device families. The purpose of this notification is to inform Xilinx customers of changes to the Kintex UltraScale and Virtex UltraScale FPGA timing specifications with an updated Vivado® speed file version requirement.

Description

Xilinx is updating Kintex UltraScale FPGA and Virtex UltraScale FPGA timing specifications for certain SelectIO™ primitive pin timing and inclusion of clock-to-clock skew checks. Designs using memory interfaces and/or SelectIO applications in Native and Component mode are required to be re-timed and any timing violations to be corrected.

Earlier Production UltraScale speed files have a small number of pin timing inaccuracies and missing clock-to-clock skew requirements that impact some SelectIO primitives. These discrepancies can result in calibration failures or data errors on certain interfaces. New designs must be generated using Vivado 2016.4 or later. Existing designs must be re-timed using the new speed files and updates made, if timing violations occur or as necessary (Refer to Design Advisory **AR# 68169** for additional information).

The following timing parameters have been updated in the Speed File:

- OSERDESE3 skew check between CLK and CLKDIV inputs
- ISERDESE3 skew check between CLK and CLK_B inputs
- IDDRE1 skew check between C and CB inputs
- BITSLICE_CONTROL skew check between RIU_CLK and PLL_CLK inputs for when used for DDR3, DDR4, and RLDRAM3 interfaces
- BITSLICE_CONTROL, RXTX_BITSLICE, RX_BITSLICE, TX_BITSLICE, ISERDESE3, IDELAYE3, and ODELAYE3 pin timing parameters

Table 1: **Speed Specification Version for Kintex UltraScale Devices**

Vivado Release Version	Speed Specification	Device
2016.4	1.23	XCKU025
		XCKU035
		XCKU040
		XCKU060
	1.24	XCKU085
		XCKU095
		XCKU115

Table 2: **Speed Specification Version for Virtex UltraScale Devices**

Vivado Release Version	Speed Specification	Device
2016.4	1.24	XCVU080
		XCVU095
		XCVU440
	1.25	XCVU065
		XCVU125
		XCVU160
		XCVU190

Note: Refer to Design Advisory **AR# 68169**

Products Affected

This notice applies to all Kintex UltraScale and Virtex UltraScale FPGA device families. The products affected include all standard part numbers and specification control document (SCD) versions of these standard part numbers. There are no changes to the silicon related to this change.

Key Dates

These changes are effective upon this PCN release.

Response

No response is required. For additional information or questions, please contact Xilinx Technical Support

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Additional Documentation

Kintex UltraScale FPGA Data Sheet: DC and Switching Characteristics:
https://www.xilinx.com/support/documentation/data_sheets/ds892-kintex-ultrascale-data-sheet.pdf .
Virtex UltraScale FPGA Data Sheet: DC and Switching Characteristics:
https://www.xilinx.com/support/documentation/data_sheets/ds893-virtex-ultrascale-data-sheet.pdf
Design Advisory **AR# 68169**

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/20/2016	1.0	Initial release.

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