TMUX6119 ±16.5-V, Low Capacitance, Low-Leakage-Current, Precision, SPDT Switch

1 Features

- Wide Supply Range: ±5 V to ±16.5 V (Dual) or 10 V to 16.5 V (Single)
- Latch-Up Performance Meets 100 mA per JESD78 Class II Level A on all Pins
- Low On-Capacitance: 6.4 pF
- Low Input Leakage: 0.5 pA
- Low Charge Injection: 0.19 pC
- Rail-to-Rail Operation
- Low On-Resistance: 120 Ω
- Transition Time: 68 ns
- Break-Before-Make Switching Action
- EN Pin and SEL Pin Connectable to V_{DD} with Integrated Pull-down
- Logic Levels: 2 V to V_{DD}
- Low Supply Current: 17 µA
- Human Body Model (HBM) ESD Protection: ±2 kV on All Pins
- Industry-Standard SOT-23 Package

2 Applications

- Factory Automation and Industrial Process Controls
- Programmable Logic Controllers (PLC)
- Analog Input Modules
- ATE Test Equipment
- Digital Multimeters
- Battery Monitoring Systems

3 Description

The TMUX6119 is a modern complementary metal-oxide semiconductor (CMOS) single-pole, double throw (SPDT) switch. The device works well with dual supplies (±5 V to ±16.5 V), a single supply (10 V to 16.5 V), or asymmetric supplies. Both digital input pins (EN and SEL) have transistor-transistor logic (TTL) compatible thresholds, ensuring both TTL/CMOS logic compatibility.

The TMUX6119 can be enabled or disabled by controlling the EN pin. When disabled, both channel switches are off. When enabled, the SEL pin can be used to turn on channel A (SA to D) or channel B (SB to D). Each channel conducts equally well in both directions and has an input signal range that extends to the supplies. The switches of TMUX6119 exhibit break-before-make (BBM) switching action.

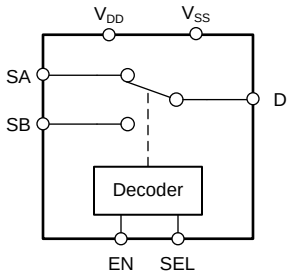
The TMUX6119 is part of Texas Instruments Precision Switches and Multiplexers family. The TMUX6119 has very low leakage currents and charge injection, allowing the device to be used in high precision measurement applications. The device also provides excellent isolation capability by blocking signal levels up to the supplies when the switches are in the OFF position. A low supply current of 17 µA enables usage in portable applications.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMUX6119	SOT-23 (8)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



TMUX6119

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2018) to Revision A	Page
• Changed the document status From: *Advanced Information* To: *Production* data	1

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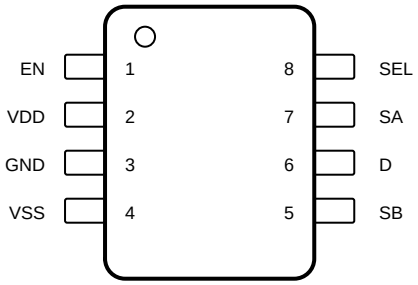
5 Pin Configuration and Functions

DCN Package
8-Pin SOT-23
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
EN	1	I	Active high digital input. When this pin is low, both switches are turned off. When this pin is high, the SEL logic input determine which switch is turned on.
V_{DD}	2	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
GND	3	P	Ground (0 V) reference
V_{SS}	4	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
SB	5	I/O	Source pin B. Can be an input or output.
D	6	I/O	Drain pin. Can be an input or output.
SA	7	I/O	Source pin A. Can be an input or output.
SEL	8	I	Logic control input.

(1) I = input, O = output, I/O = input and output, P = power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		36	V
V_{DD} to GND		–0.3	18	V
V_{SS} to GND		–18	0.3	V
V_{DIG}	Digital input pin (SEL, EN) voltage	GND –0.3	V_{DD}+0.3	V
I_{DIG}	Digital input pin (SEL, EN) current	–30	30	mA
V_{ANA_IN}	Analog input pin (Sx) voltage	V_{SS}–0.3	V_{DD}+0.3	V
I_{ANA_IN}	Analog input pin (Sx) current	–30	30	mA
V_{ANA_OUT}	Analog output pin (D) voltage	V_{SS}–0.3	V_{DD}+0.3	V
I_{ANA_OUT}	Analog output pin (D) current	–30	30	mA
T_A	Ambient temperature	–55	140	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		TMUX6119 DCN (SOT-23) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	138.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	73.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	90.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} to V_{SS} (1)	Power supply voltage differential	10		33	V
V_{DD} to GND	Positive power supply voltage (singlle supply, V_{SS} = 0 V)	10		16.5	V
V_{DD} to GND	Positive power supply voltage (dual supply)	5		16.5	V
V_{SS} to GND	Negative power supply voltage (dual supply)	–16.5		–5	V

(1) When V_{SS} = 0 V, V_{DD} can range from 10 V to 36 V.

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Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S (2)	Source pins voltage	V_{SS}		V_{DD}	V
V_D	Drain pin voltage	V_{SS}		V_{DD}	V
V_{DIG}	Digital input pin (SEL, EN) voltage	0		V_{DD}	V
I_{CH}	Channel current (T_A = 25°C)	–25		25	mA
T_A	Ambient temperature	–40		125	℃

(2) V_{DD} and V_{SS} can be any value as long as 10 V ≤ (V_{DD} – V_{SS}) ≤ 36 V.

6.5 Electrical Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range		T_A = –40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 0 V, I_S = 1 mA			120	135	Ω
		V_S = ±10 V, I_S = 1 mA			140	165	Ω
			T_A = –40°C to +85°C			210	Ω
			T_A = –40°C to +125°C			245	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = ±10 V, I_S = 1 mA			2.4	6	Ω
			T_A = –40°C to +85°C			9	Ω
			T_A = –40°C to +125°C			11	Ω
R_{ON_FLAT}	On-resistance flatness	V_S = –10 V, 0 V, +10 V, I_S = 1 mA			22	45	Ω
			T_A = –40°C to +85°C			47	Ω
			T_A = –40°C to +125°C			49	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.5		%/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ + 10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.12		0.05	nA
			T_A = –40°C to +125°C	–1		0.2	nA
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ +10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.12		0.05	nA
			T_A = –40°C to +125°C	–1		0.2	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = +10 V/ –10 V, V_D = –10 V/ +10 V		–0.04	0.01	0.04	nA
			T_A = –40°C to +85°C	–0.25		0.1	nA
			T_A = –40°C to +125°C	–1.8		0.4	nA
DIGITAL INPUT (EN, Ax pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(EN)}$	Pull-down resistance on EN pin				6		MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			16	21	µA
			T_A = –40°C to +85°C			22	µA
			T_A = –40°C to +125°C			23	µA
I_{SS}	V_{SS} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			7	10	µA
			T_A = –40°C to +85°C			11	µA
			T_A = –40°C to +125°C			12	µA

(1) When V_S is positive, V_D is negative, and vice versa.

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6.6 Switching Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Enable turn-on time	V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF		68	86	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			110	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			121	ns
t_{OFF}	Enable turn-off time	V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF		57	64	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			78	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			82	ns
t_{TRAN}	Transition time	V_S = 10 V, R_L = 300 Ω , C_L = 35 pF		68	88	ns
		V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			99	ns
		V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			106	ns
tBBM	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C	8	37		ns
Q_J	Charge injection	V_S = 0 V, R_S = 0 Ω , C_L = 1 nF		–0.19		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–85		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–93		dB
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		-7.7		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{DD}, f= 1 MHz		–55		dB
		R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{SS}, f= 1 MHz		–55		dB
BW	-3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF		700		MHz
THD	Total harmonic distortion + noise	R_L = 10k Ω , C_L = 5 pF, f= 20Hz to 20kHz		0.08		%
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		0.8		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 0 V, f = 1 MHz		1.9	2.8	pF
$C_{D(OFF)}$	Drain off-capacitance	V_S = 0 V, f = 1 MHz		4.3	4.7	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 0 V, f = 1 MHz		6.4	8.1	pF

(1) Specified by design; not subject to production testing.

6.7 Electrical Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range	T_A = –40°C to +125°C	T_A = –40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 10 V, I_S = 1 mA			230	265	Ω
			T_A = –40°C to +85°C			355	Ω
			T_A = –40°C to +125°C			405	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 10 V, I_S = 1 mA			1	9	Ω
			T_A = –40°C to +85°C			12	Ω
			T_A = –40°C to +125°C			14	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.48		%/°C

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Electrical Characteristics (Single Supply: 12 V) (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.08		0.04	nA
			T_A = –40°C to +125°C	–0.75		0.13	nA
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.08		0.04	nA
			T_A = –40°C to +125°C	–0.75		0.13	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = floating, V_D = 1 V/ 10 V		–0.04	0.01	0.04	nA
			T_A = –40°C to +85°C	–0.16		0.08	nA
			T_A = –40°C to +125°C	–1.5		0.25	nA
DIGITAL INPUT (EN, Ax pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(EN)}$	Pull-down resistance on EN pin				6		MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			11	14	µA
			T_A = –40°C to +85°C			16	µA
			T_A = –40°C to +125°C			17	µA

(1) When V_S is positive, V_D is negative, and vice versa.

6.8 Switching Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Enable turn-on time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		73	91	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			119	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			130	ns
t_{OFF}	Enable turn-off time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		60	69	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			82	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			88	ns
t_{TRAN}	Transition time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		73	93	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			104	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			112	ns
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C	10	45		ns
Q_J	Charge injection	V_S = 6 V, R_S = 0 Ω , C_L = 1 nF		0.1		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		-85		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–100		dB
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		-15		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V, f= 1 MHz		–55		dB
BW	-3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF		440		MHz
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		1		pF

(1) Specified by design; not subject to production testing.

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Switching Characteristics (Single Supply: 12 V) (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{S(OFF)}$	Source off-capacitance	V_S = 6 V, f = 1 MHz		2	2.9	pF
$C_{D(OFF)}$	Drain off-capacitance	V_S = 6 V, f = 1 MHz		4.9	5.3	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 6 V, f = 1 MHz		7.4	8.9	pF

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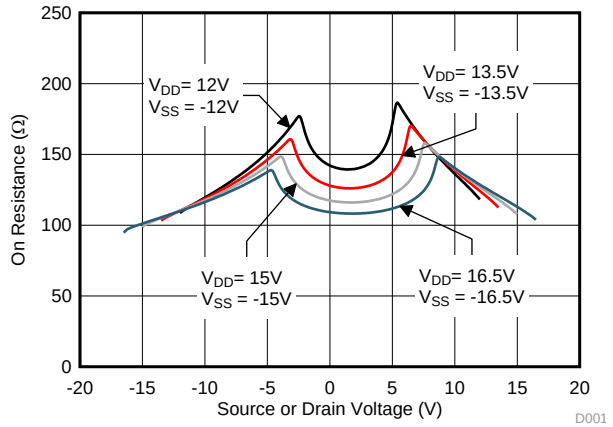
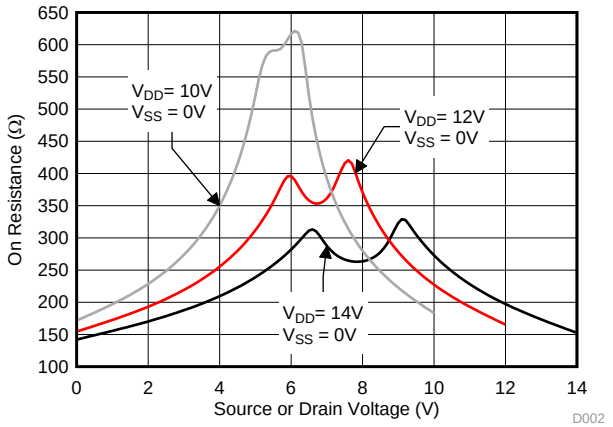
6.9 Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



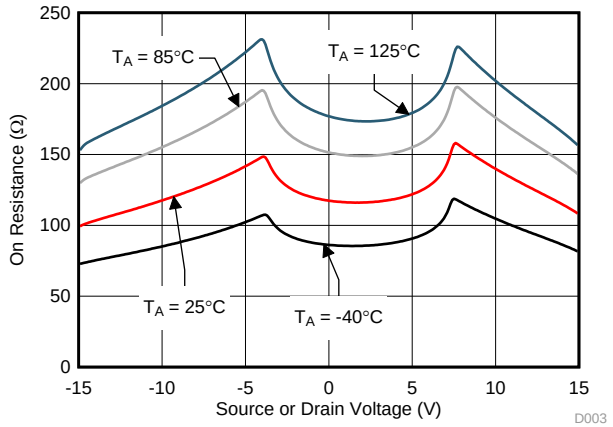
Dual Supply Operation (T_A = 25°C)

Figure 1. On-Resistance vs Source or Drain Voltage



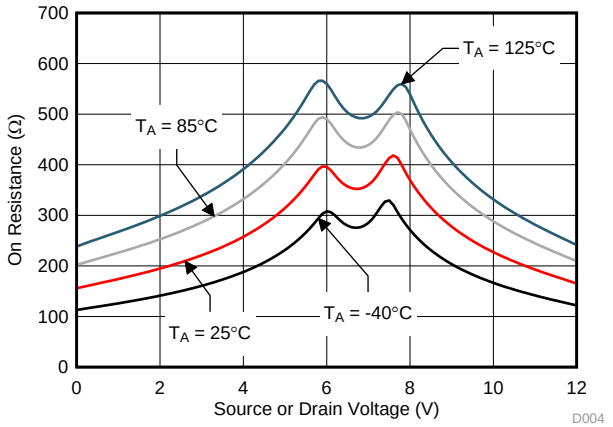
Single Supply Operation (T_A = 25°C)

Figure 2. On-Resistance vs Source or Drain Voltage



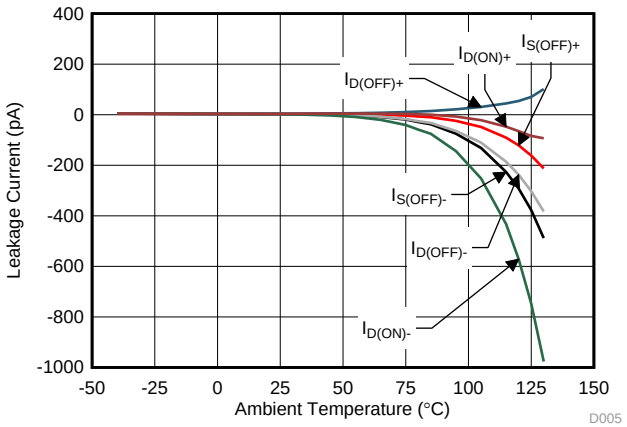
V_{DD} = 15 V, V_{SS} = –15 V

Figure 3. On-Resistance vs Source or Drain Voltage



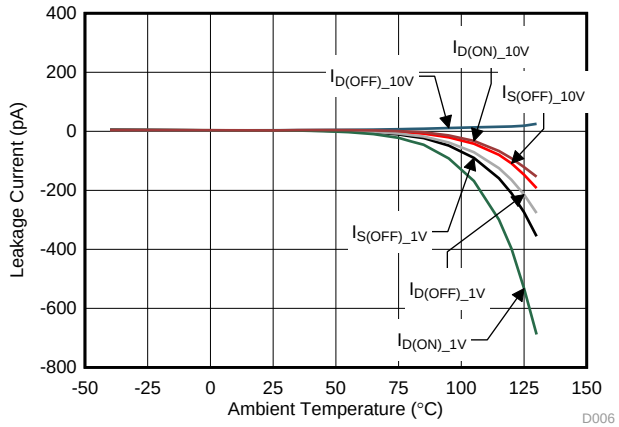
V_{DD} = 12 V, V_{SS} = 0 V

Figure 4. On-Resistance vs Source or Drain Voltage



V_{DD} = 15 V, V_{SS} = –15 V

Figure 5. . Leakage Current vs Temperature

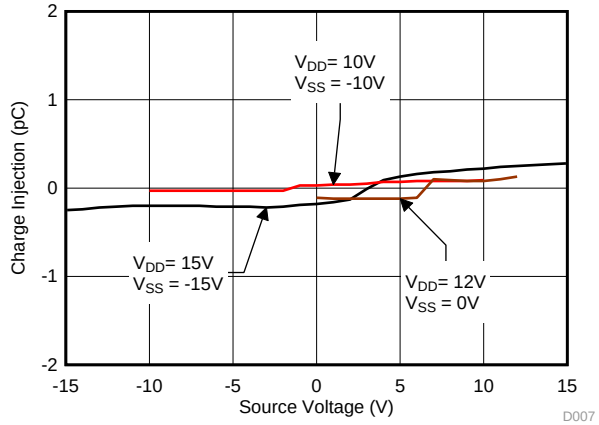


V_{DD} = 12 V, V_{SS} = 0 V

Figure 6. Leakage Current vs Temperature

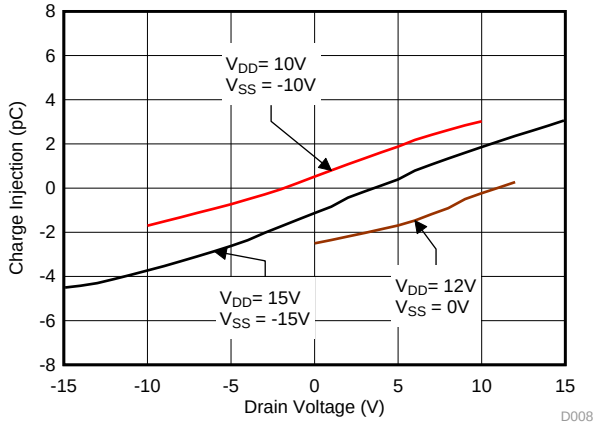
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



T_A = 25°C

Figure 7. Charge Injection vs Source Voltage



T_A = 25°C

Figure 8. Charge Injection vs Drain Voltage

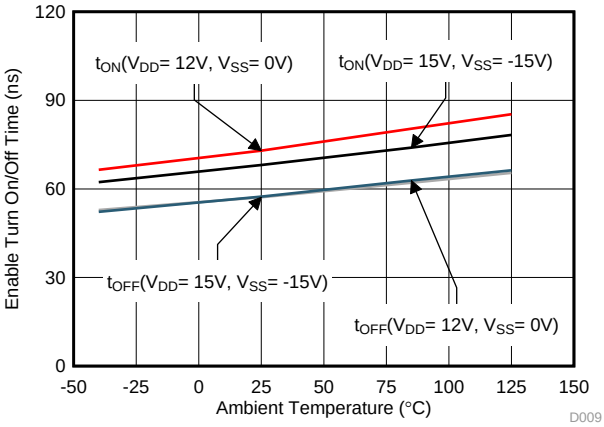
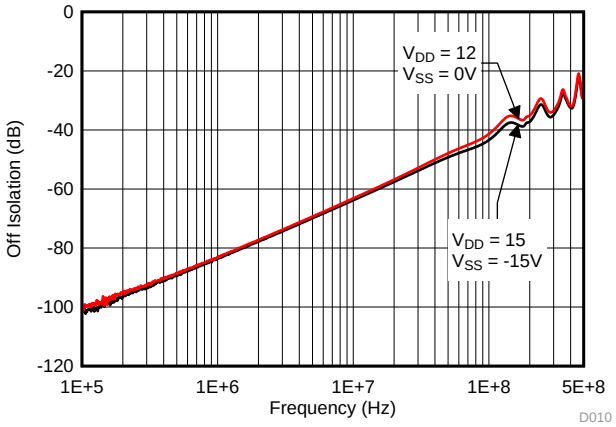
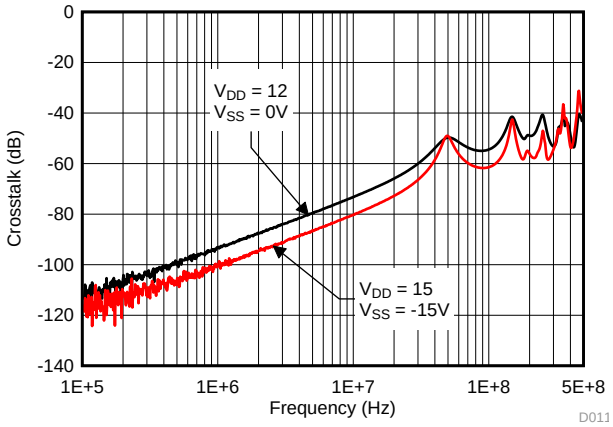


Figure 9. Enable turn-on and turn-off time



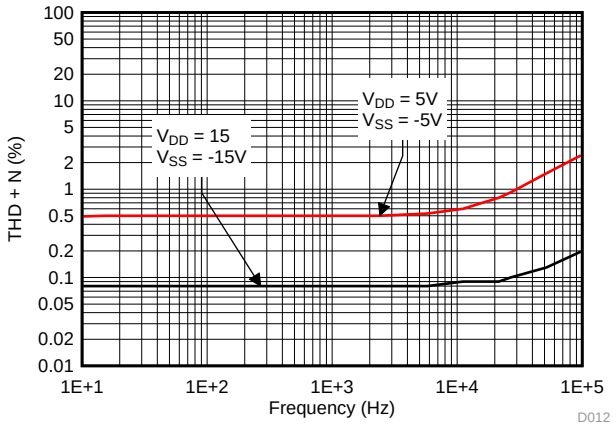
T_A = 25°C

Figure 10. Off Isolation vs Frequency



T_A = 25°C

Figure 11. Crosstalk vs Frequency



T_A = 25°C

Figure 12. THD+N vs Frequency

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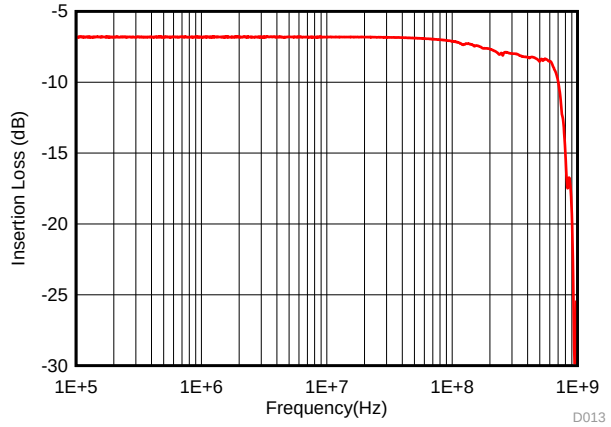
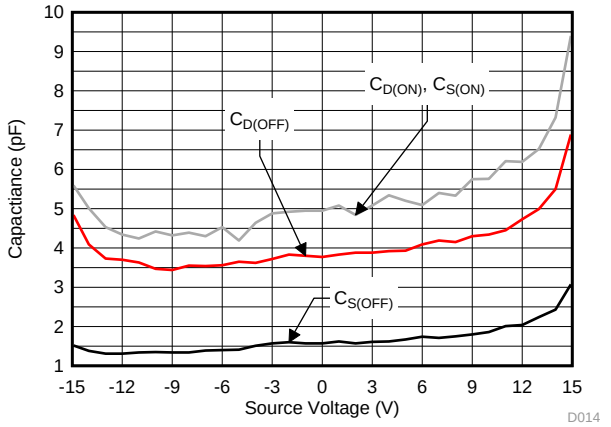
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



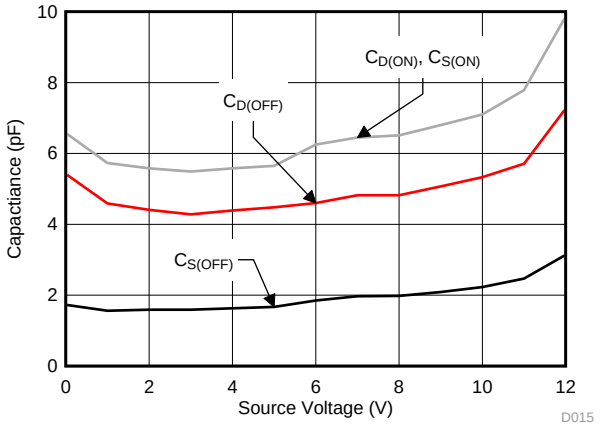
V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

Figure 13. On Response vs Frequency



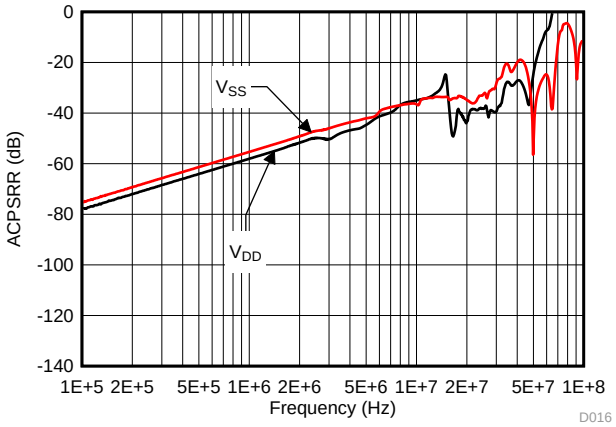
V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

Figure 14. Capacitance vs Source Voltage



V_{DD} = 12 V, V_{SS} = 0 V, T_A = 25°C

Figure 15. Capacitance vs Source Voltage



V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

Figure 16. ACPSRR vs Frequency

7 Parameter Measurement Information

7.1 Truth Tables

Table 1 shows the truth tables for theTMUX6119.

Table 1. TMUX6119 Truth Table

EN	SEL	STATE	
		Switch A (SA to D)	Switch B (SB to D)
0	X(1)	OFF	OFF
1	0	ON	OFF
1	1	OFF	ON

(1) X denotes *don't care*..

8 Detailed Description

8.1 Overview

The TMUX6119 has a low on and off leakage currents and ultra-low charge injection, allowing the device to be used in high precision measurement applications. The device also provides excellent isolation capability by blocking signal levels up to the supplies when the switches are in the OFF position. A low supply current of 17 µA enables usage in portable applications.

8.1.1 On-Resistance

The on-resistance of the TMUX6119 is the ohmic resistance across the source (SA or SB) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 17. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in Equation 1:

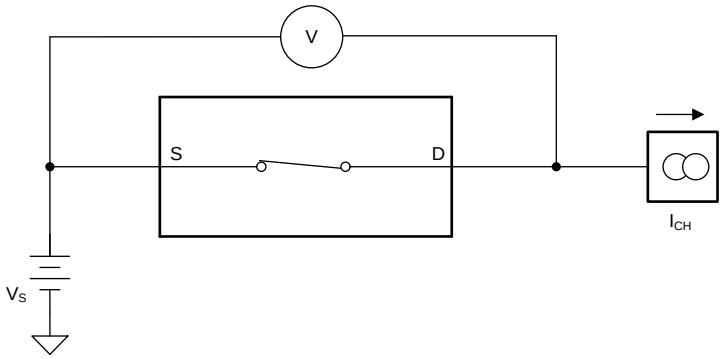


Figure 17. On-Resistance Measurement Setup

$$R_{ON} = V / I_{CH} \quad (1)$$

8.1.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in Figure 18.

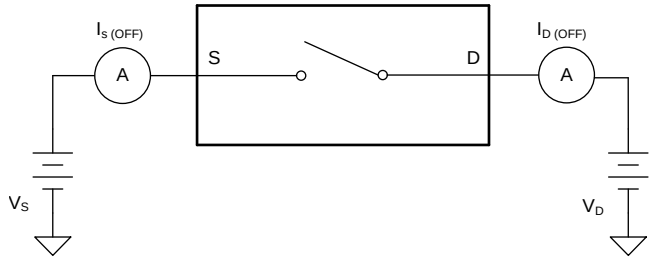


Figure 18. Off-Leakage Measurement Setup

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Overview (continued)

8.1.3 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. Figure 19 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

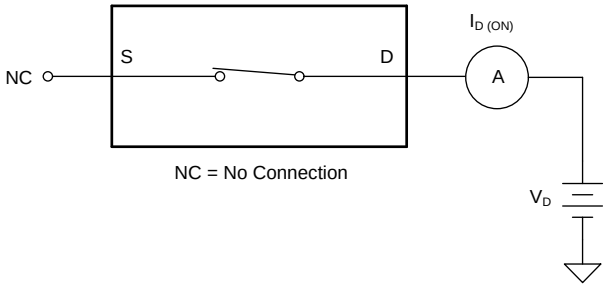

Figure 19. On-Leakage Measurement Setup

8.1.4 Transition Time

Transition time is defined as the time taken by the output of the TMUX6119 to rise or fall to 90% of the transition after the digital address signal has fallen or risen to 50% of the transition. Figure 20 shows the setup used to measure transition time, denoted by the symbol t_t.

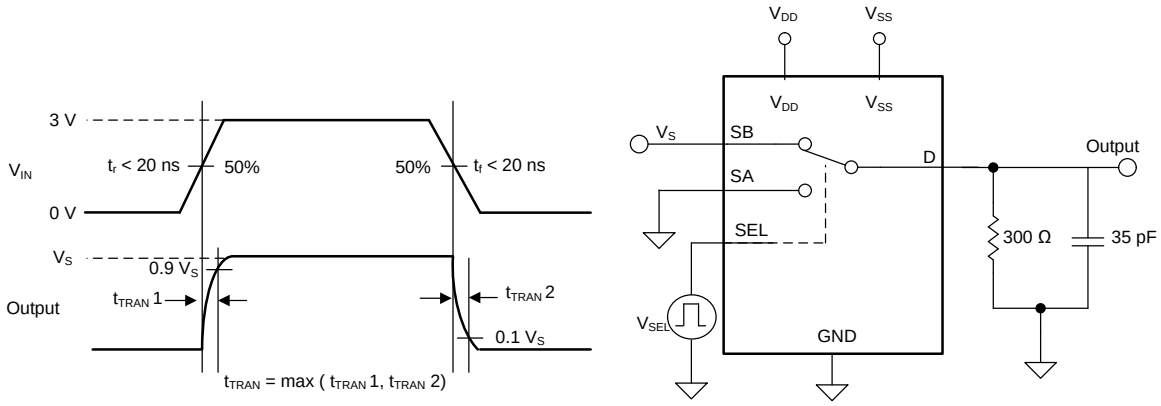

Figure 20. Transition-Time Measurement Setup

Overview (continued)

8.1.5 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the TMUX6119 is switching. The TMUX6119 output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 21 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

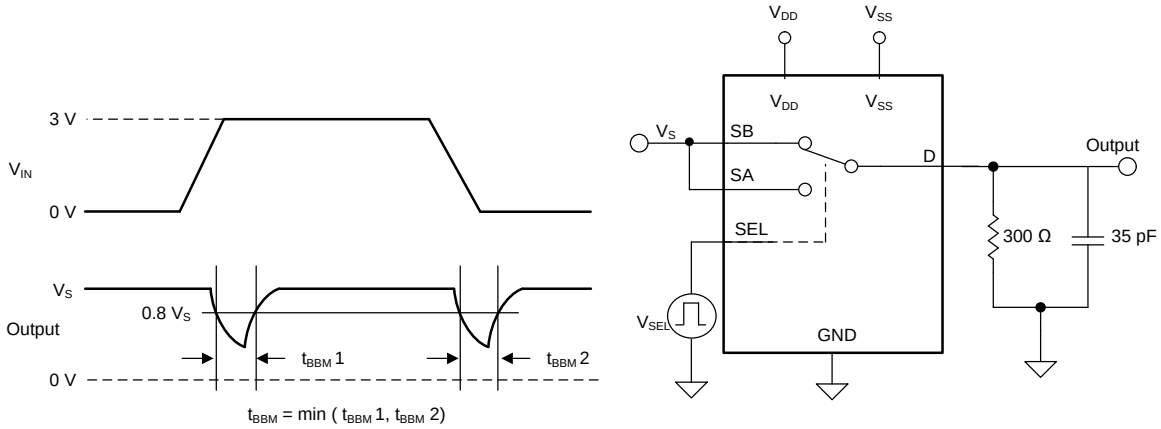

Figure 21. Break-Before-Make Delay Measurement Setup

8.1.6 Enable Turn-On and Enable Turn-Off Time

Enable turn-on time is defined as the time taken by the output of the TMUX6119 to rise to a 90% final value after the EN signal has risen to a 50% final value. Figure 22 shows the setup used to measure turn-on time. Enable turn-on time is denoted by the symbol t_{ON}.

Enable turn off time is defined as the time taken by the output of the TMUX6119 to fall to a 10% initial value after the EN signal has fallen to a 50% initial value. Figure 22 shows the setup used to measure turn-off time. Enable Turn-off time is denoted by the symbol t_{OFF}.

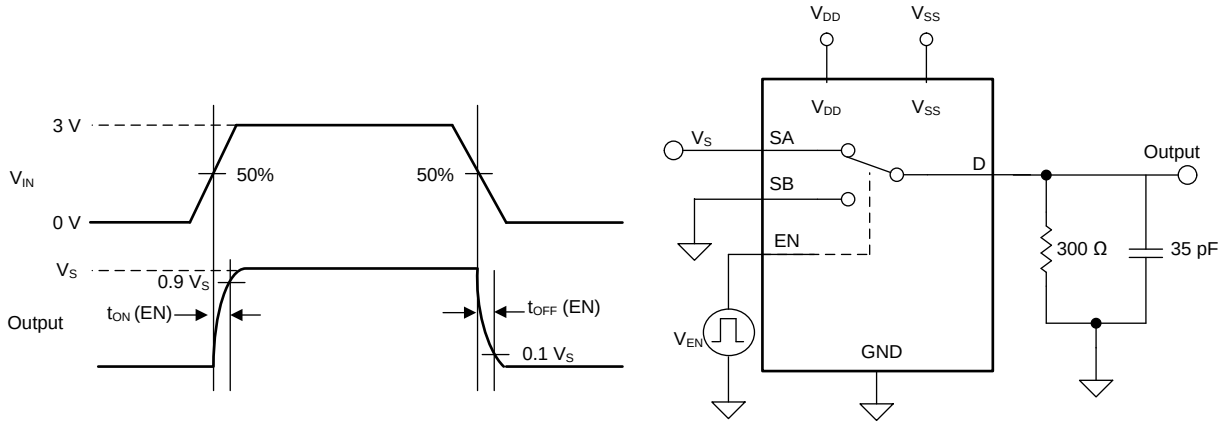

Figure 22. Turn-On and Turn-Off Time Measurement Setup

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Overview (continued)

8.1.7 Charge Injection

The TMUX6119 have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. Figure 23 and Figure 24 shows the setup used to measure charge injection from source to drain and from drain to source. The charge injection is optimized for the TMUX6119 from the direction of source to drain.

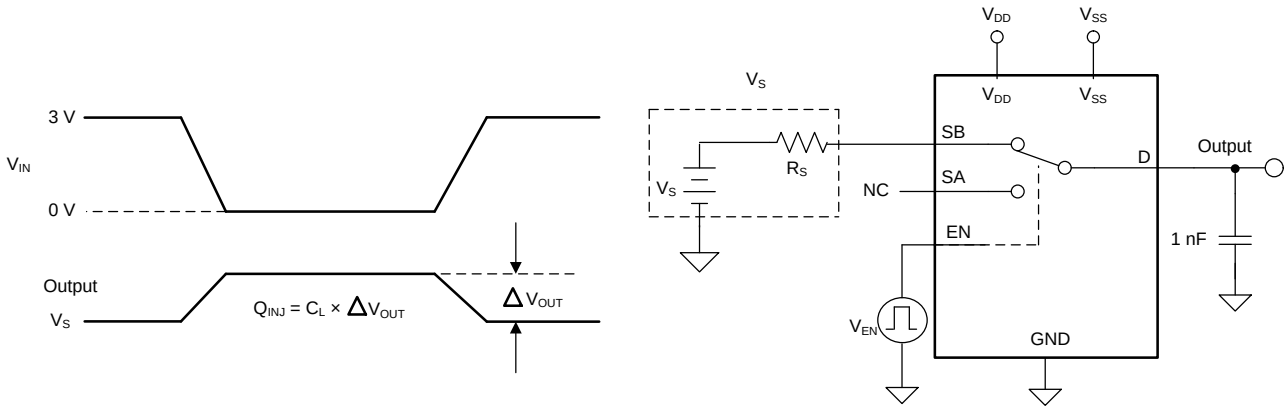

Figure 23. Source to Drain Charge-Injection Measurement Setup

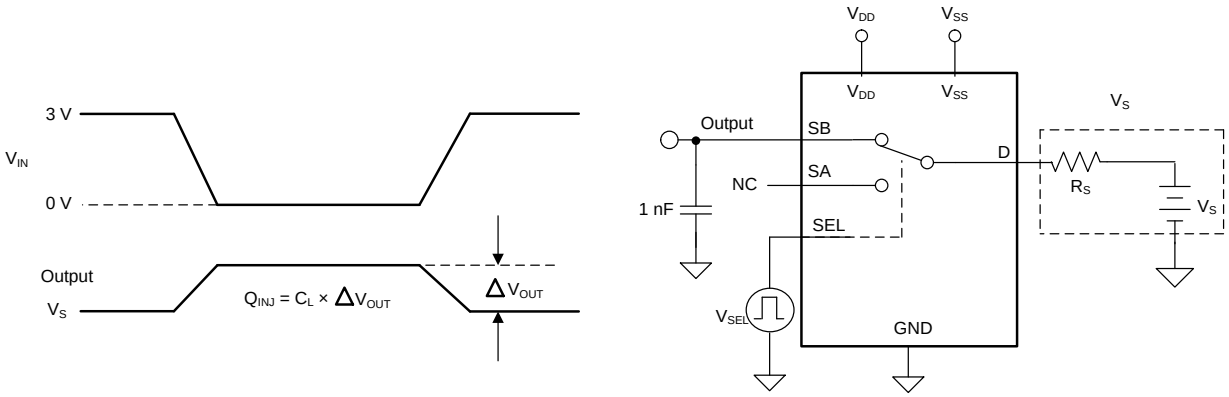

Figure 24. Drain to Source Charge-Injection Measurement Setup

8.1.8 Off Isolation

Off isolation is defined as the voltage at the drain pin (D) of the TMUX6119 when a 1-V_{RMS} signal is applied to the source pin (SA or SB) of an off-channel. Figure 25 shows the setup used to measure off isolation. Use Equation 2 to compute off isolation.

Overview (continued)

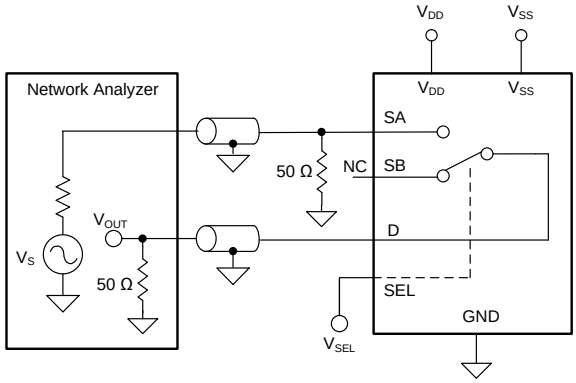

Figure 25. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

8.1.9 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (SA or SB) of an off-channel, when a 1-V_{RMS} signal is applied at the source pin of an on-channel. Figure 26 shows the setup used to measure, and Equation 3 is the equation used to compute, channel-to-channel crosstalk.

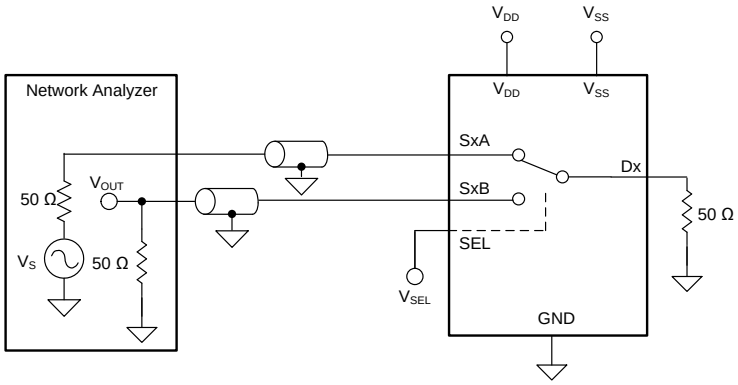

Figure 26. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (3)$$

8.1.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin of an on-channel, and the output is measured at the drain pin of the TMUX6119. Figure 27 shows the setup used to measure bandwidth of the mux. Use Equation 4 to compute the attenuation.

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Overview (continued)

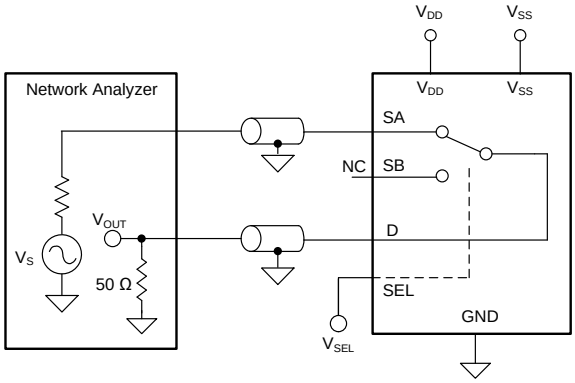

Figure 27. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log}\left(\frac{V_2}{V_1}\right) \quad (4)$$

8.1.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the TMUX6119 varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. Figure 28 shows the setup used to measure THD+N of the TMUX6119.

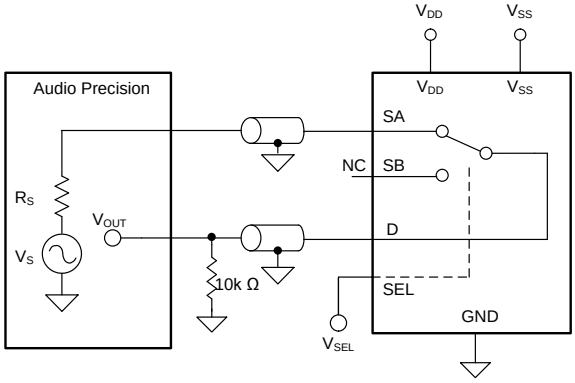

Figure 28. THD+N Measurement Setup

Overview (continued)

8.1.12 AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 mVPP. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR. Figure 29 shows the setup used to measure ACPSRR of the TMUX6119.

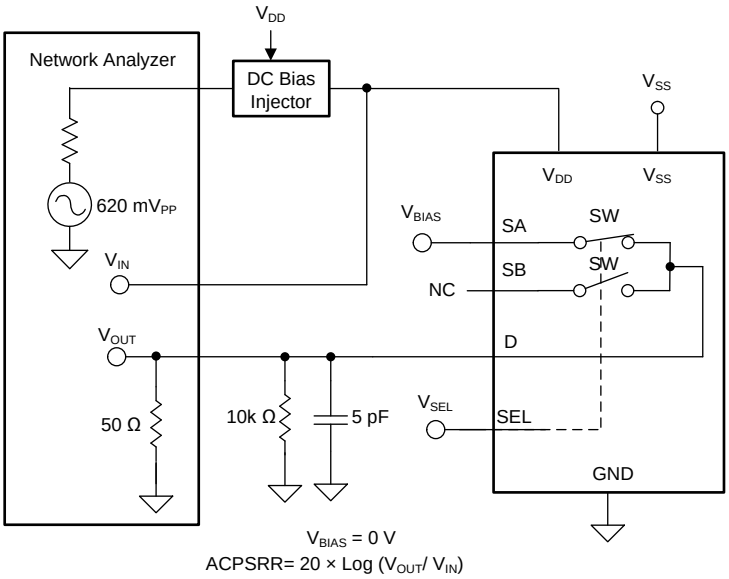

Figure 29. AC PSRR Measurement Setup

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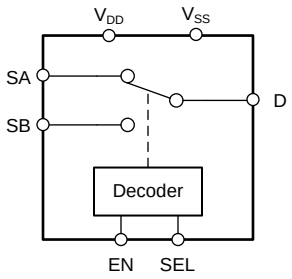
8.2 Functional Block Diagram



TMUX6119

8.3 Feature Description

8.3.1 Ultra-low Leakage Current

The TMUX6119 provide extremely low on- and off-leakage currents. The TMUX6119 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultralow leakage currents. Figure 30 shows typical leakage currents of the TMUX6119 versus temperature.

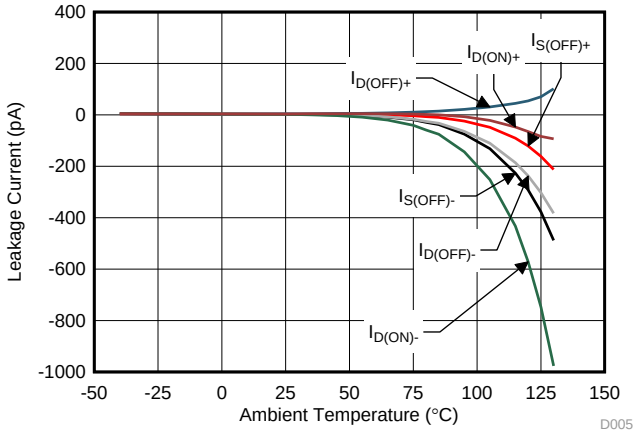


Figure 30. Leakage Current vs Temperature

8.3.2 Ultra-low Charge Injection

The TMUX6119 is implemented with simple transmission gate topology, as shown in Figure 31. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

Feature Description (continued)

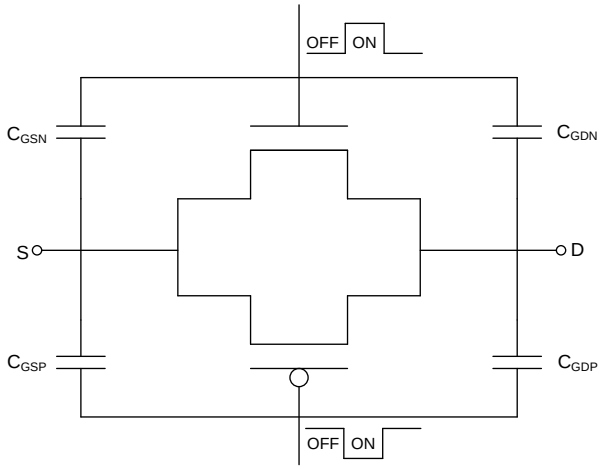


Figure 31. Transmission Gate Topology

The TMUX6119 utilizes special charge-injection cancellation circuitry that reduces the source (SA or SB)-to-drain (D) charge injection to as low as 0.19 pC at V_S = 0 V, as shown in Figure 32.

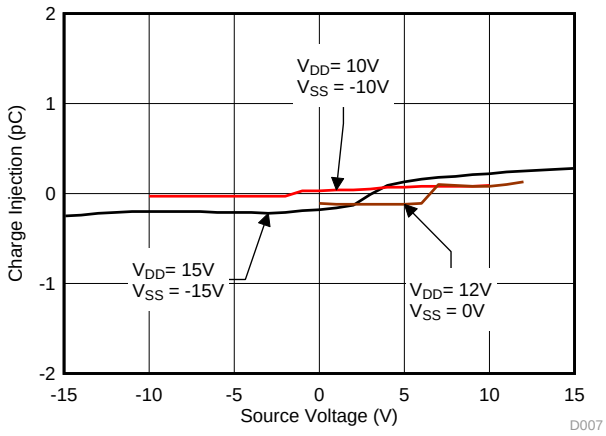


Figure 32. Charge Injection vs Source Voltage

The drain (D)-to-source (SA or SB) charge injection becomes important when the device is used as a demultiplexer (demux), where D becomes the input and Sx becomes the output. Figure 33 shows the drain-to-source charge injection across the full signal range.

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Feature Description (continued)

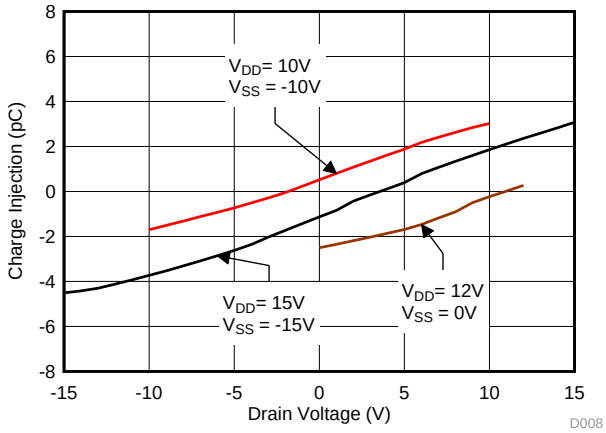

Figure 33. Charge Injection vs Drain Voltage

8.3.3 Bidirectional and Rail-to-Rail Operation

The TMUX6119 conducts equally well from source (SA or SB) to drain (D) or from drain (D) to source (SA or SB). Each TMUX6119 channel has very similar characteristics in both directions. The valid analog signal for TMUX6119 ranges from V_{SS} to V_{DD}. The input signal to the TMUX6119 swings from V_{SS} to V_{DD} without any significant degradation in performance.

8.4 Device Functional Modes

When the EN pin of the TMUX6119 is pulled high, one of the two switches is closed based on the state of the SEL pin. When the EN pin is pulled low, both switches remain open irrespective of the state of the SEL pin. The EN pin is weakly pull-down internally through a 6MΩ resistor, thereby setting each channel to the open state if the EN pin is not actively driven. The SEL pin is also weakly pulled-down through an internal 6Mohm resistor, allowing channel A (SA to D) to be selected by default when EN pin is driven high. Both the EN pin and the SEL pin can be connected to V_{DD} (as high as 16.5 V).

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX6119 offers outstanding input / output leakage current and ultra-low charge injection performance. The on-capacitance of the TMUX6119 is also very low. These properties make the TMUX6119 ideal for implementing high precision industrial systems requiring selection of one of two inputs or outputs.

9.2 Typical Application

One application to take advantage of TMUX6119's precision performance is the implementation of the chopper amplifier. The chopper amplifier was developed in the 1950s to achieve ultra-low offset voltage and low offset voltage drift over time and temperature. It also drastically reduces low frequency 1/f (flicker) noise. These attributes make the chopper amplifier ideal for small signal conditioning. Figure 34 illustrates a classic example of a simple chopper amplifier implemented with two TMUX6119 SPDT switches.

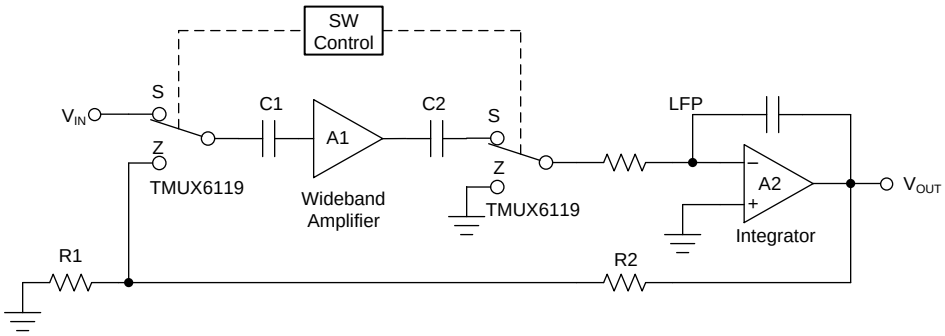

Figure 34. Example of classic chopper amplifier implemented with two TMUX6119

9.2.1 Design Requirements

The goal of a chopper-amplifier design is to produce extremely high DC precision by continuously self-cancelling input offset voltage even during variations in temperature, time, common-mode voltage, and power supply voltage, while reducing low-frequency 1/f (flicker) voltage.

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Typical Application (continued)

9.2.2 Detailed Design Procedure

The theory of operation for the chopper amplifier relies on the concept of converting a DC input signal to AC before feeding it into an AC-coupled wideband amplifier. The conversion utilizes a SPDT switches to “chop” the input DC signal into an AC voltage. The output of the amplifier is then modulated by another SPDT switch to convert the signal back to DC. The output of the switch is then low-pass filtered (or integrated) to smooth and produce the final DC output.

The operation of the chopper amplifier consists of 2 phases, the sampling (S) phase and the auto-zero (Z) phase. During the auto-zero phase, the switches are toggled to the Z position, and capacitors C1 and C2 are charged to the amplifier input and output offset voltage, respectively. During the sampling phase, the switches are toggled to the S position, during which VIN is connected to VOUT through C1, the wideband amplifier, C2, and the integrator. Input DC voltage is AC-coupled by capacitor C1 and amplified by the wideband amplifier A1. C2 helps reduce any DC component caused by the amplifier’s input offset voltage, and the integrator helps smooth out the output signals to produce desired DC voltage output.

Several mechanisms helps reduce overall noise of the chopper-amplifier design. The DC gain, being the product of the AC stage and the DC gain of the integrator, can easily reach an open-loop gain of 160 dB or higher and therefore reduce the gain error, V_{OUT}/ (A1×A2) to almost zero. The offset and drift in the output integrator stage are nulled by the DC gain of the preceding AC stage. DC drifts in the AC stage are also non-factors because the amplification stage is AC-coupled. The 1/f noise of the wideband amplifier is modulated to higher frequencies by the demodulator.

Note that the input signal frequency shall be much less than one-half of the chopping frequency to prevent aliasing errors in this chopper amplifier implementation. The chopper frequency, in turn, is restricted by the wideband amplifier’s gain-phase limitations as well as errors induced by switch transition time and charge injection. The TMUX6119 ‘s switch transition time is only 68 ns (typ) and average charge injection is less than 0.19pC, making it ideal for the chopper amplifier implementation. However, the input signal frequency is still limited by the amplifier’s performance. If higher sampling frequency is required, a chopper-stabilized amplifier, or an integrated zero-drift amplifier (such as the OPA2188), can be used to satisfy the requirement.

9.2.3 Application Curve

Fast transition time and small charge injection are two critical parameters for the SPDT switches used in the chopper amplifier design. Figure 35 shows the plot for the charge injection vs. source voltage for the TMUX6119.

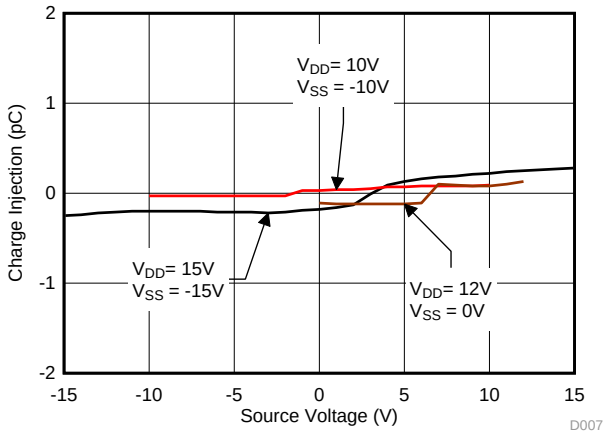

Figure 35. Charge Injection vs Source Voltage

10 Power Supply Recommendations

The TMUX6119 operates across a wide supply range of ±5 V to ±16.5 V (10 V to 16.5 V in single-supply mode). They also perform well with unsymmetric supplies such as V_{DD} = 12 V and V_{SS}= –5 V. For reliable operation, use a supply decoupling capacitor ranging between 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground.

The on-resistance of the TMUX6119 varies with supply voltage, as illustrated in Figure 36.

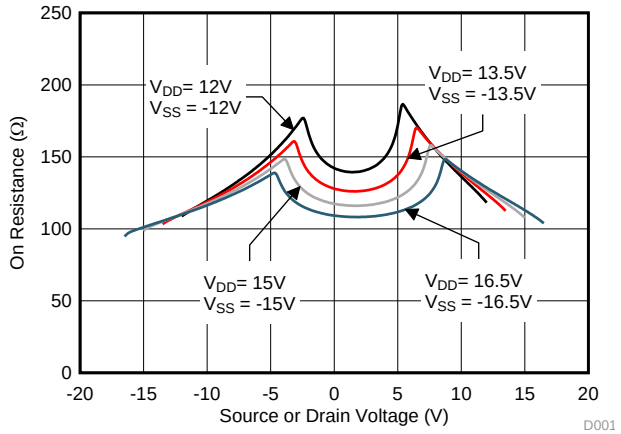

Figure 36. On-Resistance Variation With Supply and Input Voltage

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11 Layout

11.1 Layout Guidelines

Figure 37 shows an example of a PCB layout with the TMUX6119.

Some key considerations are:

1. Decouple the V_{DD} and V_{SS} pins with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as short as possible. In case of the differential signal, make sure the A inputs and B inputs are as symmetric as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

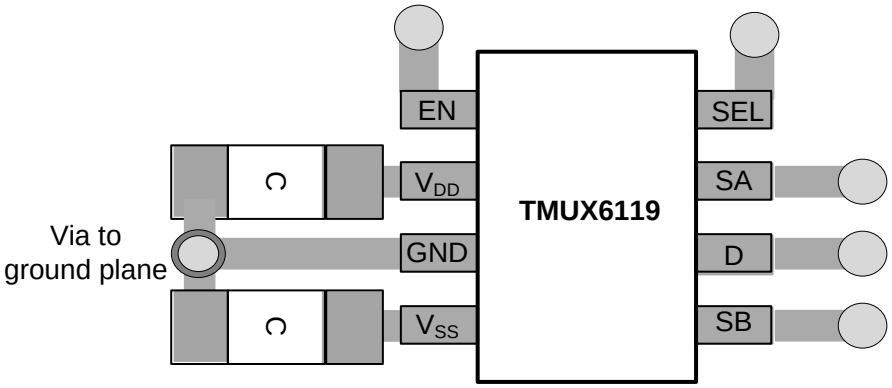

Figure 37. TMUX6119 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- *OPA2188 0.03-μV/°C Drift, Low-Noise, Rail-to-Rail Output, 36-V, Zero-Drift Operational Amplifiers* (SBOS525)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX6119DCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1QAC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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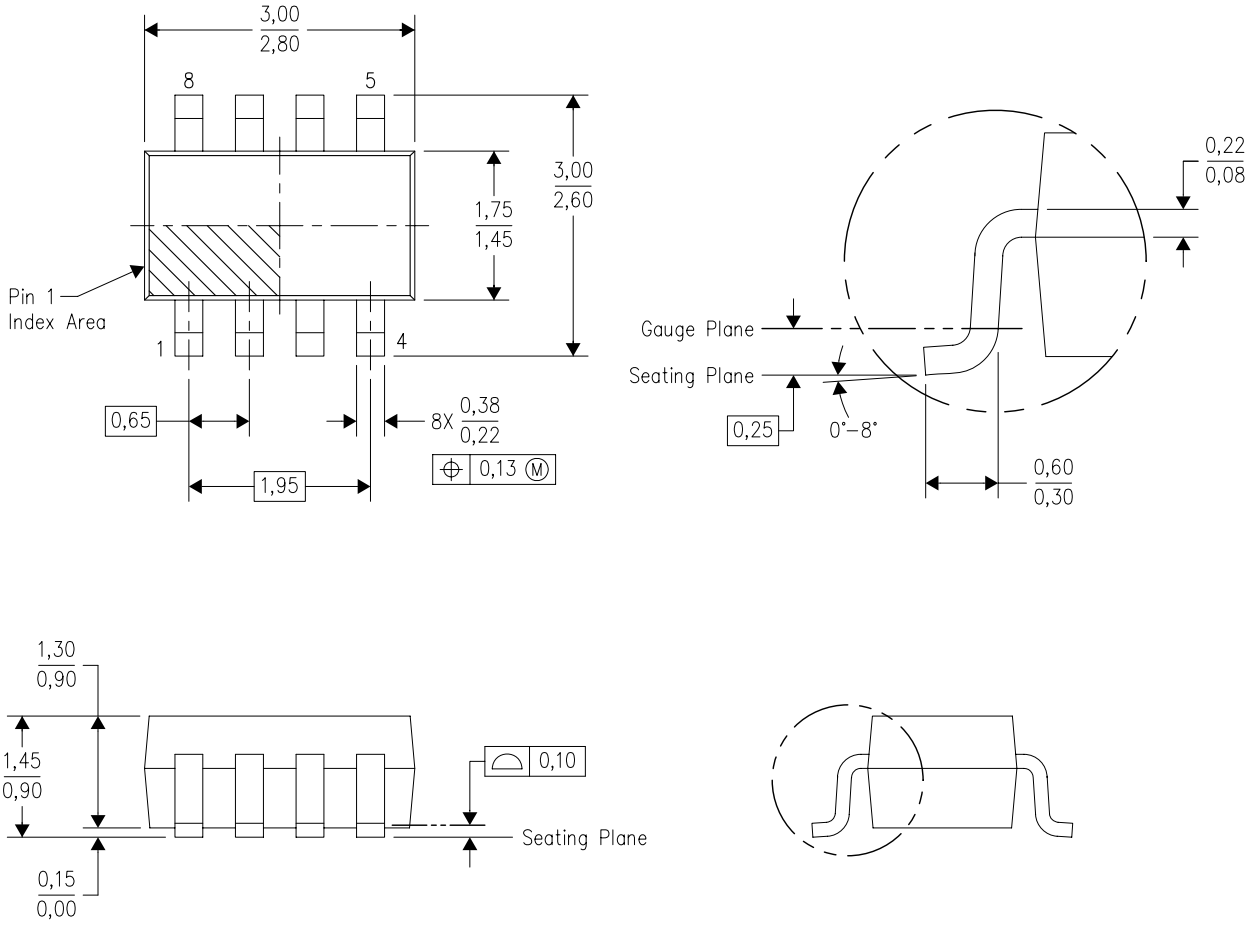
DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

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