ANALOG DEVICES

Single Comparator with Known Power-Up State

Data Sheet

ADCMP391

FEATURES

Single-supply voltage operation: 2.3 V to 5.5 V
Rail-to-rail common-mode input voltage range
Low input offset voltage across V_{CMR}: 1 mV typical
Guarantees comparator output logic low from V_{CC} = 0.9 V to undervoltage lockout (UVLO)
Operating temperature range: −40°C to +125°C
8-lead, narrow body SOIC

APPLICATIONS

Battery management/monitoring
Power supply detection
Window comparators
Threshold detectors/discriminators
Microprocessor systems

FUNCTIONAL BLOCK DIAGRAM

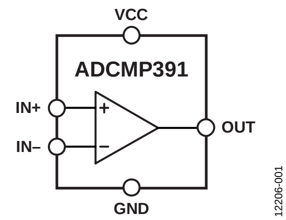

Figure 1.

GENERAL DESCRIPTION

The ADCMP391 is a single, rail-to-rail input, low power comparator ideal for use in general-purpose applications. The device operates from a single supply voltage of 2.3 V to 5.5 V and draws a minimal amount of current. The ADCMP391 consumes only 18.6 µA of supply current. The low voltage and low current operation of the ADCMP391 makes it ideal for battery-powered systems.

The ADCMP391 features a common-mode input voltage range of 200 mV beyond rails, an offset voltage of 1 mV typical across the full common-mode range, and a UVLO monitor. In addition, the design of the comparator allows a defined output state upon power-up. The comparator generates a logic low output if the supply voltage is less than the UVLO threshold.

The ADCMP391 is available in an 8-lead, narrow body SOIC package. The ADCMP391 is specified to operate over the extended temperature range of −40°C to +125°C.

Rev. 0
Document Feedback

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REVISION HISTORY

8/14—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2.3 V to 5.5 V, T_A = −40°C to +125°C, V_{CMR} = −200 mV to V_{CC} + 200 mV, unless otherwise noted. Typical values are at T_A = 25°C.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments[1]
POWER SUPPLY						
Supply Voltage	V_{CC}	2.3		5.5	V	
		0.9		$UVLO_{RISE}$	V	Guarantees comparator output low
V_{CC} Quiescent Current	I_{CC}		18.6	24.7	µA	All outputs in high-Z state, V_{OD} = 0.1 V
			18.5	23.8	µA	All outputs low, V_{OD} = 0.1 V
UNDERVOLTAGE LOCKOUT						
V_{CC} Rising	$UVLO_{RISE}$	2.062	2.162	2.262	V	
Hysteresis	$UVLO_{HYS}$	5	25	50	mV	
COMPARATOR INPUT						
Common-Mode Input Range	V_{CMR}	−200		V_{CC} + 200	mV	
Input Offset Voltage	V_{OS}		0.5	2.5	mV	IN+ = IN− = 1 V
			0.5	2.5	mV	IN+ = IN− = 1 V, T_A = −40°C to +85°C
			1	5	mV	
			1	5	mV	T_A = −40°C to +85°C
Input Offset Current	I_{OS}			10	nA	V_{CMR} = −50 mV to V_{CC} + 50 mV
Input Bias Current	I_{BIAS}			±30	nA	IN+ = IN− = 1 V
				±80	nA	V_{CMR} = −50 mV to V_{CC} + 50 mV
				±10	nA	V_{CMR} = −50 mV to V_{CC} + 50 mV, T_A = −40°C to +85°C
Input Hysteresis	V_{HYST}		3	4	mV	V_{CM} = 1 V
			6	8	mV	
COMPARATOR OUTPUT						
Output Low Voltage	V_{OL}		0.1	0.3	V	V_{CC} = 2.3 V, I_{SINK} = 2.5 mA
			0.01	0.15	V	V_{CC} = 0.9 V, I_{SINK} = 100 µA
Output Leakage Current	I_{LEAK}			150	nA	V_{OUT} = 0 V to 5.5 V
COMPARATOR CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	60	80		dB	
Common-Mode Rejection Ratio	CMRR	50	74		dB	
Voltage Gain	A_V		132		dB	
Rise Time[2]	t_R		1.1		µs	V_{OUT} = 10% to 90% of V_{CC}
Fall Time[2]	t_F		0.15		µs	V_{OUT} = 90% to 10% of V_{CC}
Propagation Delay						
Input Rising[2]	t_{PROP_R}		4.7		µs	V_{CM} = 1 V, V_{CC} = 2.3 V, V_{OD} = 10 mV
			4.9		µs	V_{CM} = 1 V, V_{CC} = 5 V, V_{OD} = 10 mV
				2.8	µs	V_{CM} = 1 V, V_{CC} = 2.3 V, V_{OD} = 100 mV
				3.2	µs	V_{CM} = 1 V, V_{CC} = 5 V, V_{OD} = 100 mV
Input Falling[2]	t_{PROP_F}		4.5		µs	V_{CM} = 1 V, V_{CC} = 2.3 V, V_{OD} = 10 mV
			9.5		µs	V_{CM} = 1 V, V_{CC} = 5 V, V_{OD} = 10 mV
				2	µs	V_{CM} = 1 V, V_{CC} = 2.3 V, V_{OD} = 100 mV
				4.2	µs	V_{CM} = 1 V, V_{CC} = 5 V, V_{OD} = 100 mV

[1] V_{OD} is overdrive voltage.
[2] R_{PULLUP} = 10 kΩ, and C_L = 50 pF.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC Pin	−0.3 V to +6 V
IN+ and IN− Pins	−0.3 V to +6 V
OUT Pin	−0.3 V to +6 V
OUT Pin Sink Current (I_{SINK})	10 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead Narrow-Body SOIC	121	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

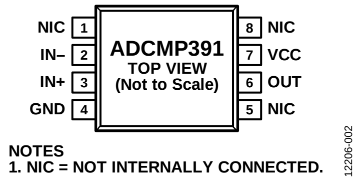

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 8	NIC	Not Internally Connected
2	IN−	Comparator Inverting Input
3	IN+	Comparator Noninverting Input
4	GND	Device Ground
6	OUT	Comparator Output, Open-Drain
7	VCC	Device Supply Input

TYPICAL PERFORMANCE CHARACTERISTICS

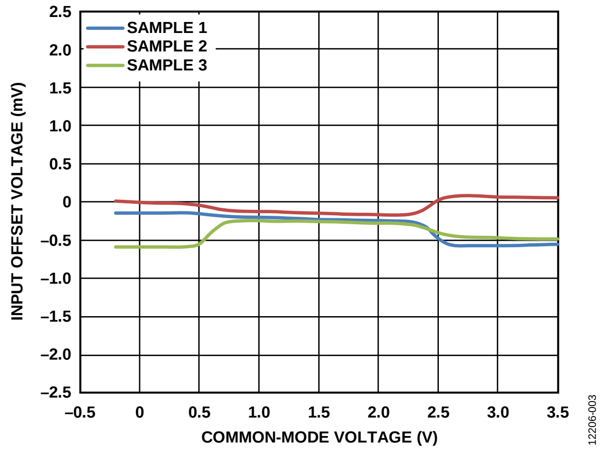

Figure 3. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{CC} = 3.3 V

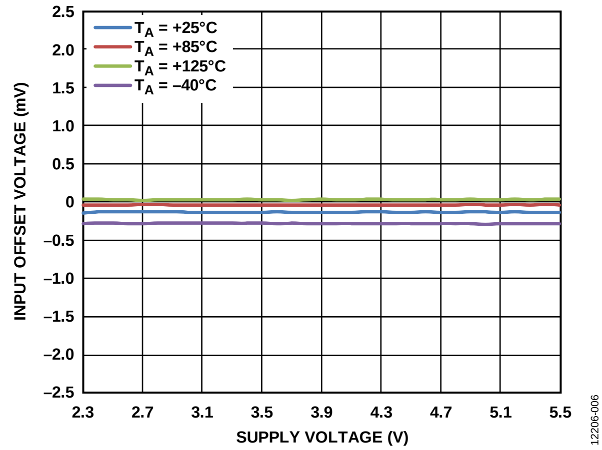

Figure 6. Input Offset Voltage (V_{OS}) vs. Supply Voltage (V_{CC}), V_{CM} = 1 V for Various Temperatures

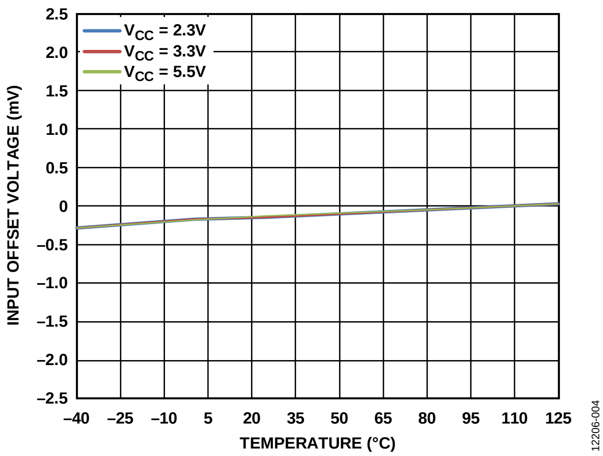

Figure 4. Input Offset Voltage (V_{OS}) vs. Temperature for Various Supply Voltages (V_{CC}), V_{CM} = 1 V

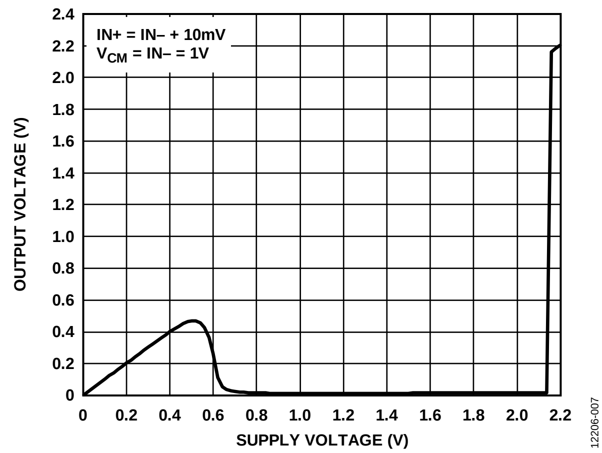

Figure 7. Output Voltage (V_{OUT}) vs. Supply Voltage (V_{CC}), R_{PULLUP} = 10 kΩ

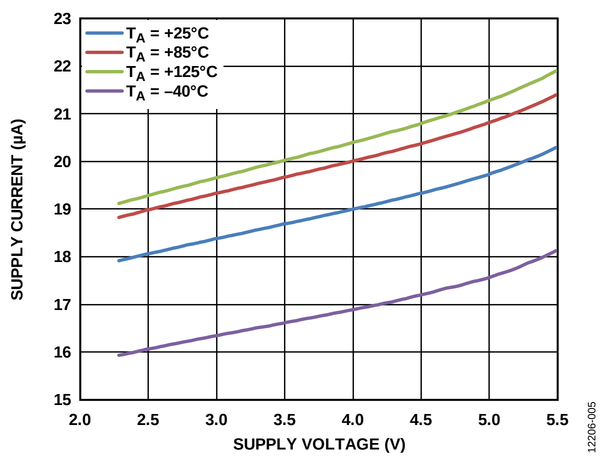

Figure 5. Supply Current vs. Supply Voltage (V_{CC}) at Output Low Voltage for Various Temperatures

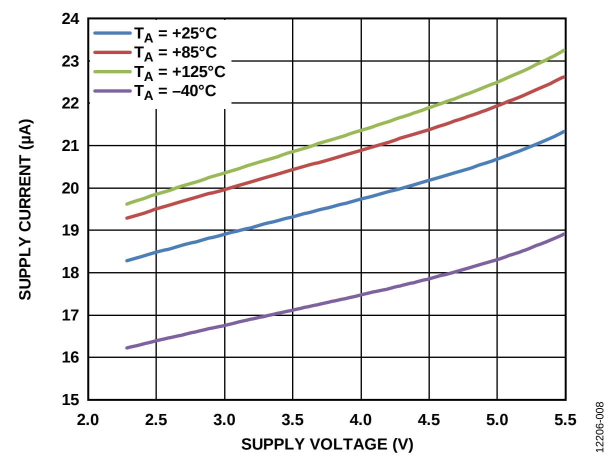

Figure 8. Supply Current vs. Supply Voltage (V_{CC}) at Output High Voltage for Various Temperatures

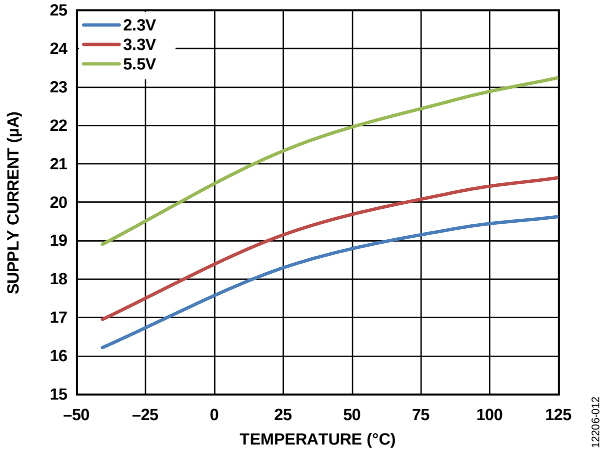

Figure 9. Supply Current vs. Temperature at Output High Voltage for Various Supply Voltages (V_{CC})

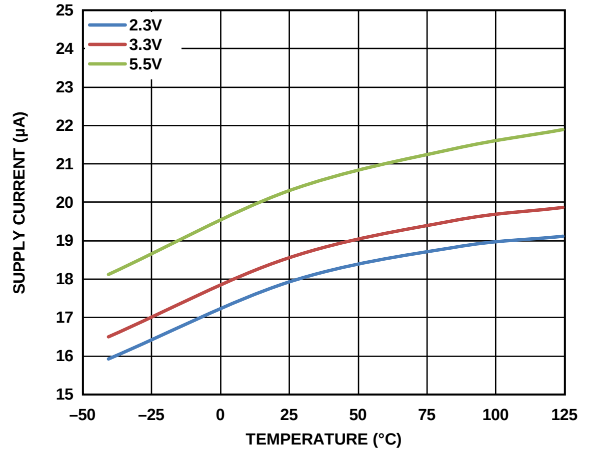

Figure 12. Supply Current vs. Temperature at Output Low Voltage for Various Supply Voltages (V_{CC})

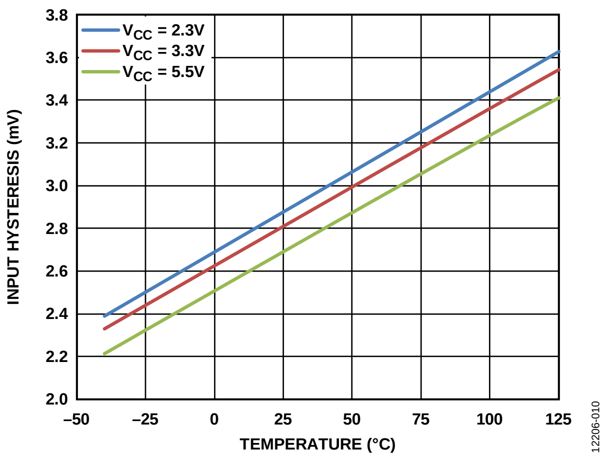

Figure 10. Input Hysteresis vs. Temperature for Various Supply Voltages (V_{CC}), V_{CM} = 1 V

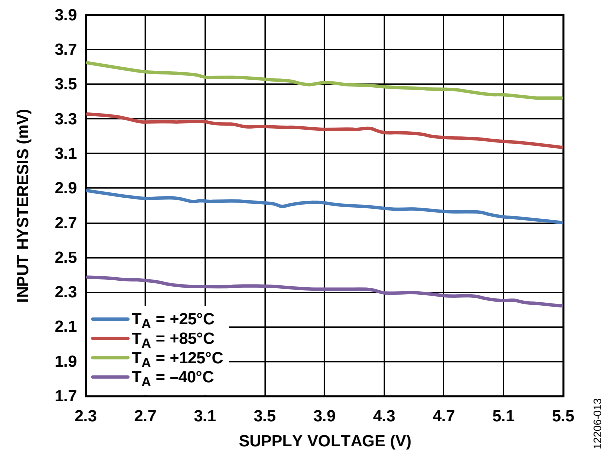

Figure 13. Input Hysteresis vs. Supply Voltage (V_{CC}) for Various Temperatures, V_{CM} = 1 V

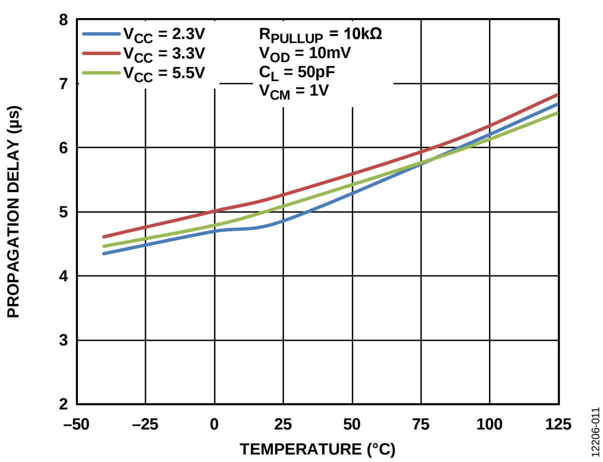

Figure 11. Propagation Delay vs. Temperature, Low to High, V_{OD} = 10 mV

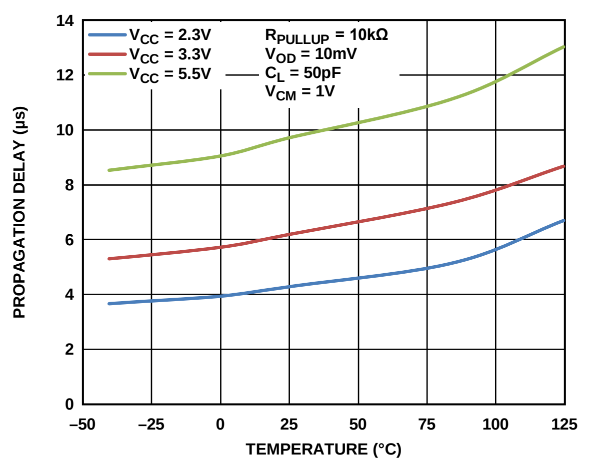

Figure 14. Propagation Delay vs. Temperature, High to Low, V_{OD} = 10 mV

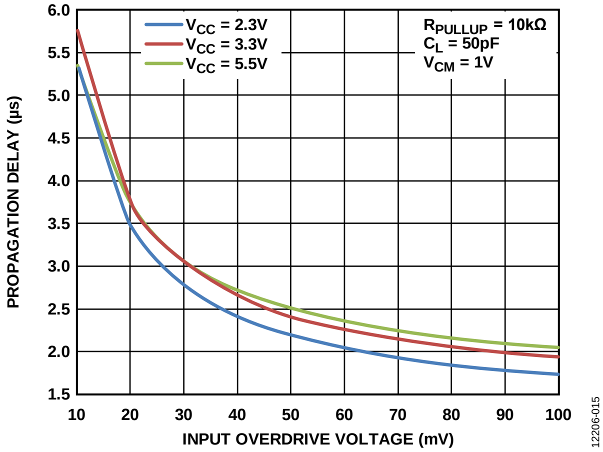

Figure 15. Propagation Delay vs. Input Overdrive Voltage, Low to High

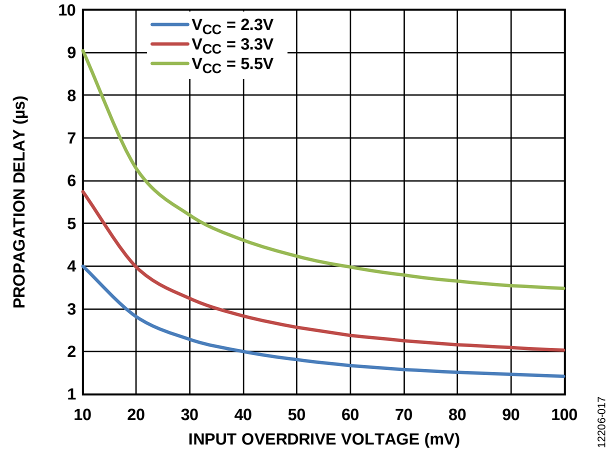

Figure 17. Propagation Delay vs. Input Overdrive Voltage, High to Low

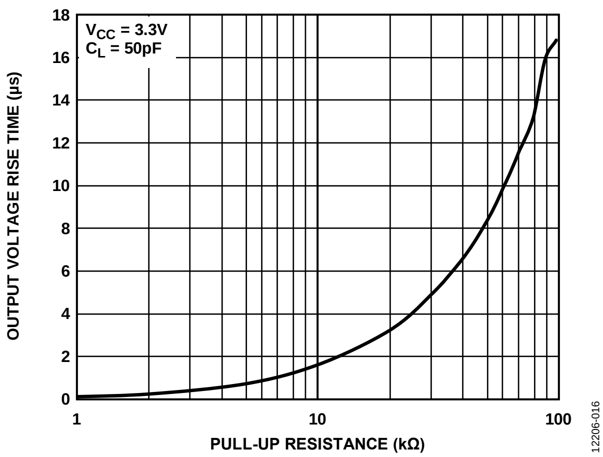

Figure 16. Output Voltage Rise Time (t_R) vs. Pull-Up Resistance (R_{PULLUP})

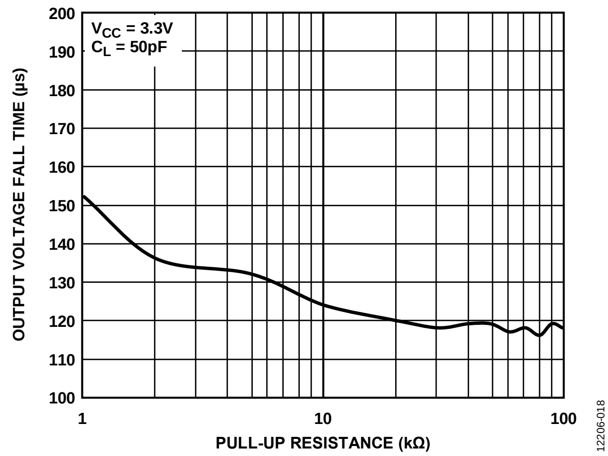

Figure 18. Output Voltage Fall Time (t_F) vs. Pull-Up Resistance (R_{PULLUP})

THEORY OF OPERATION

BASIC COMPARATOR

In its most basic configuration, a comparator can be used to convert an analog input signal to a digital output signal (see Figure 19). The analog signal on IN+ is compared to the voltage on IN−, and the voltage at OUT is either high or low, depending on whether IN+ is at a higher or lower potential than IN−, respectively.

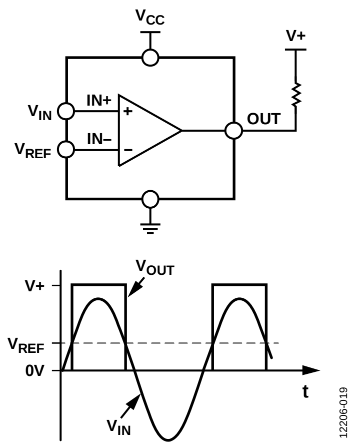

Figure 19. Basic Comparator and Input and Output Signals

RAIL-TO-RAIL INPUT (RRI)

Using a CMOS nonRRI stage (that is, a single differential pair) limits the input voltage to approximately one gate-to-source voltage (V_{GS}) away from one of the supply lines. Because V_{GS} for normal operation is commonly more than 1 V, a single differential pair input stage comparator greatly restricts the allowable input voltage. This restriction can be quite limiting with low voltage supplies. To resolve this issue, RRI stages allow the input signal range to extend up to the supply voltage range. In the case of the ADCMP391, the inputs continue to operate 200 mV beyond the supply rails.

OPEN-DRAIN OUTPUT

The ADCMP391 has an open-drain output stage that requires an external resistor to pull up to the logic high voltage level when the output transistor is switched off. The pull-up resistor must be large enough to avoid excessive power dissipation, but small enough to switch logic levels reasonably quickly when the comparator output is connected to other digital circuitry. The rise time of the open-drain output depends on the pull-up resistor (R_{PULLUP}) and load capacitor (C_L) used.

The rise time can be calculated by

$$t_R = 2.197\, R_{PULLUP}\, C_L \quad (1)$$

POWER-UP BEHAVIOR

On power-up, when V_{CC} reaches 0.9 V, the ADCMP391 is guaranteed to assert an output low logic. When the voltage on the V_{CC} pin exceeds UVLO, the comparator inputs take control.

CROSSOVER BIAS POINT

Rail-to-rail inputs of this type of architecture, in both op amps and comparators, have a dual front-end design. PMOS devices are inactive near the V_{CC} rail, and NMOS devices are inactive near GND. At some predetermined point in the common-mode range, a crossover occurs. At this point, normally 0.8 V and V_{CC} − 0.8 V, the measured offset voltages change.

COMPARATOR HYSTERESIS

In noisy environments, or when the differential input amplitudes are relatively small or slow moving, adding hysteresis (V_{HYST}) to the comparator is often desirable. The transfer function for a comparator with hysteresis is shown in Figure 20. As the input voltage approaches the threshold (0 V in Figure 20) from below the threshold region in a positive direction, the comparator switches from low to high when the input crosses $+V_{HYST}/2$. The new switch threshold becomes $-V_{HYST}/2$. The comparator remains in the high state until the $-V_{HYST}/2$ threshold is crossed from below the threshold region in a negative direction. In this manner, noise or feedback output signals centered on the 0 V input cannot cause the comparator to switch states unless it exceeds the region bounded by $\pm V_{HYST}/2$.

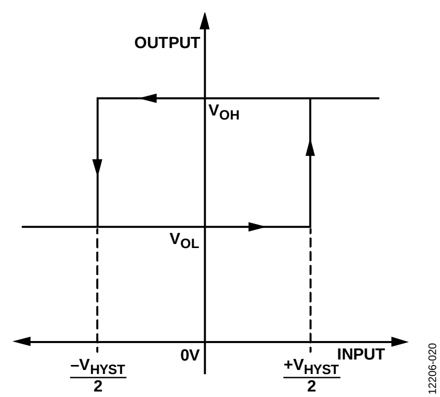

Figure 20. Comparator Hysteresis Transfer Function

TYPICAL APPLICATIONS

ADDING HYSTERESIS

To add hysteresis, see Figure 21; two resistors are used to create different switching thresholds, depending on whether the input signal is increasing or decreasing in magnitude. When the input voltage increases, the threshold is above V_{REF}, and when the input voltage decreases, the threshold is below V_{REF}.

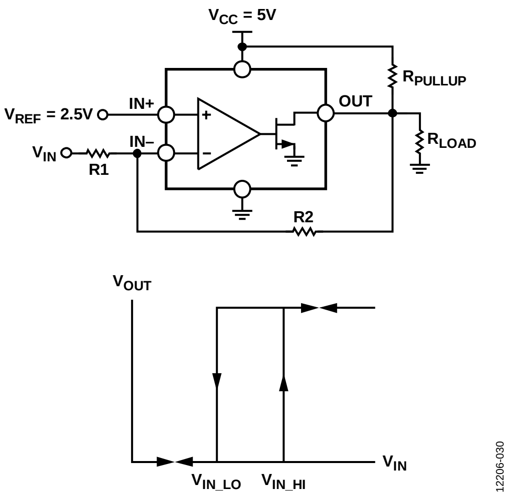

Figure 21. Noninverting Comparator Configuration with Hysteresis

The upper input threshold level is given by

$$V_{IN\_HI} = \frac{V_{REF}(R1 + R2)}{R2} \quad (2)$$

Assuming R_{LOAD} >> R2, R_{PULLUP}.

The lower input threshold level is given by

$$V_{IN\_LO} = \frac{V_{REF}(R1 + R2 + R_{PULLUP}) - V_{CC}R1}{R2 + R_{PULLUP}} \quad (3)$$

The hysteresis is the difference between these voltages levels.

$$\Delta V_{IN} = \frac{V_{CC}R1}{R2 + R_{PULLUP}} \quad (4)$$

WINDOW COMPARATOR FOR POSITIVE VOLTAGE MONITORING

When monitoring a positive supply, the desired nominal operating voltage for monitoring is denoted by V_M, I_M is the nominal current through the resistor divider, V_{OV} is the overvoltage trip point, and V_{UV} is the undervoltage trip point.

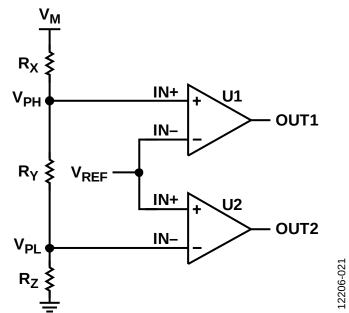

Figure 22. Positive Undervoltage/Overvoltage Monitoring Configuration

Figure 22 illustrates the positive voltage monitoring input connection. Three external resistors, R_X, R_Y, and R_Z, divide the positive voltage for monitoring, V_M, into the high-side voltage, V_{PH}, and the low-side voltage, V_{PL}. The high-side voltage is connected to the IN+ pin of U1 and the low-side voltage is connected to the IN– pin of U2.

To trigger an overvoltage condition, the low-side voltage (in this case, V_{PL}) must exceed the V_{REF} threshold on the IN+ pin of U2. Calculate the low-side voltage, V_{PL}, by the following:

$$V_{PL} = V_{REF} = V_{OV}\left(\frac{R_Z}{R_X + R_Y + R_Z}\right) \quad (5)$$

In addition,

$$R_X + R_Y + R_Z = V_M/I_M \quad (6)$$

Therefore, R_Z, which sets the desired trip point for the overvoltage monitor, is calculated as

$$R_Z = \frac{(V_{REF})(V_M)}{(V_{OV})(I_M)} \quad (7)$$

To trigger the undervoltage condition, the high-side voltage, V_{PH}, must be less than the V_{REF} threshold on the IN– pin of U1. The high-side voltage, V_{PH}, is calculated by

$$V_{PH} = V_{REF} = V_{UV}\left(\frac{R_Y + R_Z}{R_X + R_Y + R_Z}\right) \quad (8)$$

Because R_Z is already known, R_Y can be expressed as

$$R_Y = \frac{(V_{REF})(V_M)}{(V_{UV})(I_M)} - R_Z \quad (9)$$

When R_Y and R_Z are known, R_X can be calculated by

$$R_X = (V_M/I_M) - R_Y - R_Z \quad (10)$$

If V_M, I_M, V_{OV}, or V_{UV} changes, each step must be recalculated.

WINDOW COMPARATOR FOR NEGATIVE VOLTAGE MONITORING

Figure 23 shows the circuit configuration for negative supply voltage monitoring. To monitor a negative voltage, a reference voltage is required to connect to the end node of the voltage divider circuit, in this case, V_{REF}.

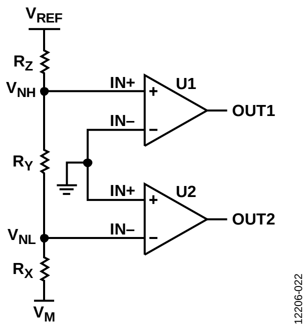

Figure 23. Negative Undervoltage/Overvoltage Monitoring Configuration

Equation 7, Equation 9, and Equation 10 need some minor modifications for use with negative voltage monitoring. The reference voltage, V_{REF}, is added to the overall voltage drop; therefore, it must be subtracted from V_M, V_{UV}, and V_{OV} before using each of them in Equation 7, Equation 9, and Equation 10.

To monitor a negative voltage level, the resistor divider circuit divides the voltage differential level between V_{REF} and the negative supply voltage into the high-side voltage, V_{NH}, and the low-side voltage, V_{NL}. The high-side voltage, V_{NH}, is connected to IN+ of U1, and the low-side voltage, V_{NL}, is connected to IN− of U2.

To trigger an overvoltage condition, the monitored voltage must exceed the nominal voltage in terms of magnitude, and the high-side voltage (in this case, V_{NH}) on the IN+ pin of U1 must be more negative than ground. Calculate the high-side voltage, V_{NH}, with the following formula:

$$V_{NH} = GND = \left[\left(V_{REF} - V_{OV} \right) \left(\frac{R_X + R_Y}{R_X + R_Y + R_Z} \right) \right] + V_{OV} \quad (11)$$

In addition,

$$R_X + R_Y + R_Z = \frac{\left(V_M - V_{REF} \right)}{I_M} \quad (12)$$

Therefore, R_Z, which sets the desired trip point for the overvoltage monitor, is calculated by

$$R_Z = \frac{-V_{REF}\left(V_M - V_{REF} \right)}{I_M\left(V_{OV} - V_{REF} \right)} \quad (13)$$

To trigger an undervoltage condition, the monitored voltage must be less than the nominal voltage in terms of magnitude, and the low-side voltage (in this case, V_{NL}) on the IN− pin of U2 must be more positive than ground. Calculate the low-side voltage, V_{NL}, by the following:

$$V_{NL} = GND = \left[\left(V_{REF} - V_{UV} \right) \left(\frac{R_X}{R_X + R_Y + R_Z} \right) \right] + V_{UV} \quad (14)$$

Because R_Z is already known, R_Y can be expressed as follows:

$$R_Y = \frac{-V_{REF}\left(V_M - V_{REF} \right)}{I_M\left(V_{UV} - V_{REF} \right)} - R_Z \quad (15)$$

When R_Y and R_Z are known, R_X is then calculated by

$$R_X = \frac{\left(V_M - V_{REF} \right)}{I_M} - R_Y - R_Z \quad (16)$$

PROGRAMMABLE SEQUENCING CONTROL CIRCUIT

The circuit shown in Figure 24 is used to control the power supply sequencing. The delay is set by the combination of the pull-up resistor (R_{PULLUP}), the load capacitor (C_L), and the resistor divider network.

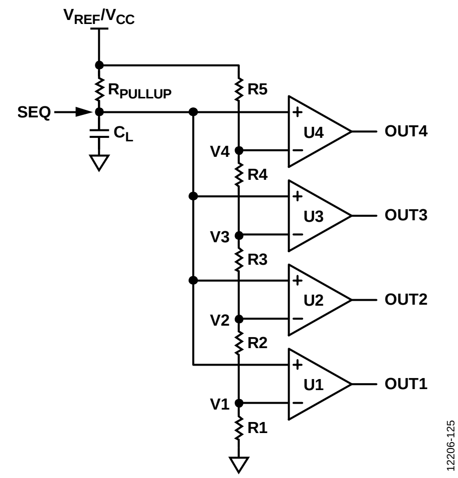

Figure 24. Programmable Sequencing Control Circuit

Figure 25 shows a simplified block diagram for the programmable sequencing control circuit. The application delays the enable signal, EN, of the external regulators (LDO x) in a linear order when the open-drain signal (SEQ) changes from low to high impedance.

The ADCMP391 has a defined output state during startup, which prevents any regulator from turning on if V_{CC} is still below the UVLO threshold.

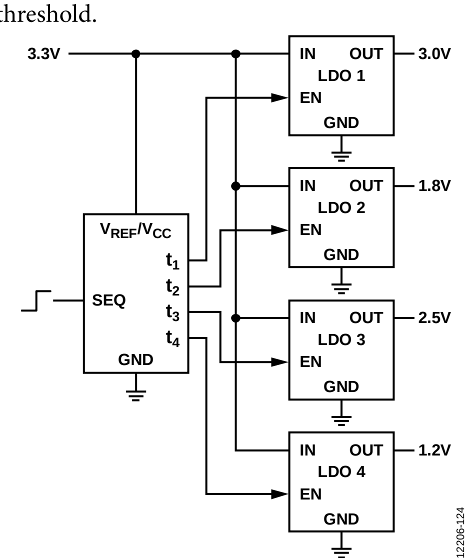

Figure 25. Simplified Block Diagram of a Programmable Sequencing Control Circuit

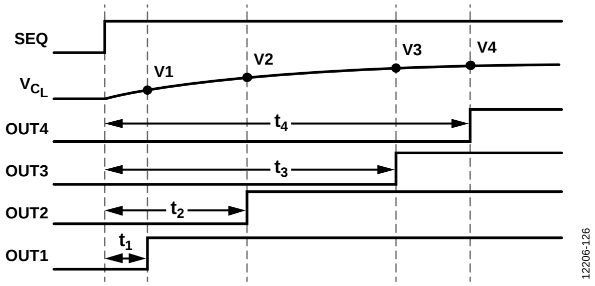

Figure 26. Programmable Sequencing Control Circuit Timing Diagram

When the SEQ signal changes from low to high impedance, the load capacitor, C_L, starts to charge. The time it takes to charge the load capacitor to the pull-up voltage (in this case, V_{REF} or V_{CC}) is the maximum delay programmable in the circuit. It is recommended to have the threshold within 10% to 90% of the pull-up voltage. Calculate the maximum allowable delay by

$$t_{MAX} = t_R = 2.197\ R_{PULLUP}\ C_L \tag{17}$$

The delay of each output is changed by changing the threshold voltage, V1 to V4, when the comparator changes its output state.

To calculate the voltage thresholds for the comparator, use the following formulas:

$$V1 = V_{REF}\left(1 - e^{\frac{-t_1}{R_{PULLUP}C_L}}\right) \tag{18}$$

$$V2 = V_{REF}\left(1 - e^{\frac{-t_2}{R_{PULLUP}C_L}}\right) \tag{19}$$

$$V3 = V_{REF}\left(1 - e^{\frac{-t_3}{R_{PULLUP}C_L}}\right) \tag{20}$$

$$V4 = V_{REF}\left(1 - e^{\frac{-t_4}{R_{PULLUP}C_L}}\right) \tag{21}$$

The threshold voltages can come from a voltage reference or a voltage divider circuit, as shown in Figure 24.

First, determine the allowable current, I_{DIV}, flowing through the resistor divider. After the value for I_{DIV} is determined, calculate R1, R2, R3, R4, and R5 using the following formulas:

$$R_{DIV} = \frac{V_{REF}}{I_{DIV}} = R1 + R2 + R3 + R4 + R5 \tag{22}$$

$$R1 = \frac{V1 R_{DIV}}{V_{REF}} \tag{23}$$

$$R2 = \frac{V2 R_{DIV}}{V_{REF}} - R1 \tag{24}$$

$$R3 = \frac{V3 R_{DIV}}{V_{REF}} - R1 - R2 \tag{25}$$

$$R4 = \frac{V4 R_{DIV}}{V_{REF}} - R1 - R2 - R3 \tag{26}$$

$$R5 = R_{DIV} - R1 - R2 - R3 - R4 \tag{27}$$

To create a mirrored voltage sequence, add a resistor, R_{MIRROR}, between the pull-up resistor (R_{PULLUP}) and the load capacitor (C_L) as shown in Figure 27.

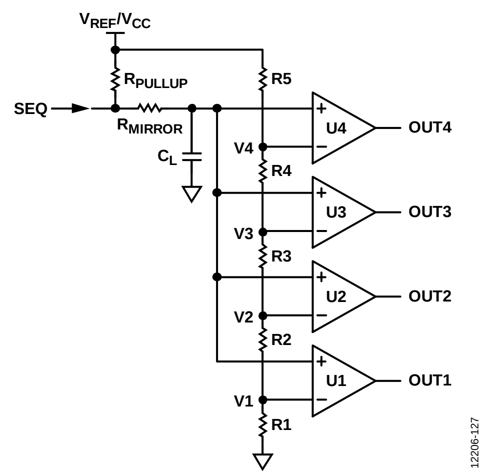

Figure 27. Circuit Configuration for a Mirrored Voltage Sequencer

Figure 27 shows the circuit configuration for a mirrored voltage sequencer. When SEQ changes from low to high impedance, the response is similar to Figure 26. When SEQ changes from high impedance to low, the load capacitor (C_L) starts to discharge at a rate set by R_{MIRROR}. The delay of each comparator is dependent on the threshold voltage previously set for t_1 to t_4. The result is a mirrored power-down sequence.

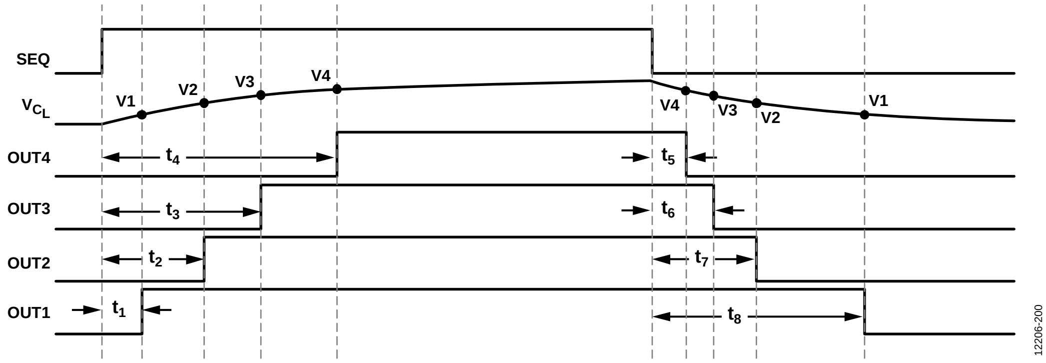

Figure 28. Mirrored Voltage Sequencer Timing Diagram

The timing diagram for the mirrored voltage sequencer is shown in Figure 28.

Equation 18 through Equation 21 must account for the additional resistance, R_{MIRROR}, in the calculations of the voltage thresholds. To calculate these new thresholds, see Equation 28 through Equation 31.

$$V1 = V_{REF}\left(1 - e^{\frac{-t_1}{(R_{PULLUP} + R_{MIRROR})C_L}}\right) \quad (28)$$

$$V2 = V_{REF}\left(1 - e^{\frac{-t_2}{(R_{PULLUP} + R_{MIRROR})C_L}}\right) \quad (29)$$

$$V3 = V_{REF}\left(1 - e^{\frac{-t_3}{(R_{PULLUP} + R_{MIRROR})C_L}}\right) \quad (30)$$

$$V4 = V_{REF}\left(1 - e^{\frac{-t_4}{(R_{PULLUP} + R_{MIRROR})C_L}}\right) \quad (31)$$

R_{MIRROR} provides the mirrored delay by prolonging the discharge time of the capacitor. The mirrored voltage sequencer uses the same threshold in Equation 28 to Equation 31 in a decreasing order. To calculate the exact value of the mirrored delay time, see Equation 32 through Equation 35.

$$t_5 = -R_{MIRROR}C_L \ln\left(\frac{V4}{V_{REF}}\right) \quad (32)$$

$$t_6 = -R_{MIRROR}C_L \ln\left(\frac{V3}{V_{REF}}\right) \quad (33)$$

$$t_7 = -R_{MIRROR}C_L \ln\left(\frac{V2}{V_{REF}}\right) \quad (34)$$

$$t_8 = -R_{MIRROR}C_L \ln\left(\frac{V1}{V_{REF}}\right) \quad (35)$$

MIRRORED VOLTAGE SEQUENCER EXAMPLE

To illustrate how the mirrored voltage sequencer works, see Figure 25 and then consider a system that uses a V_{REF} of 1 V and requires a delay of 50 ms when SEQ changes from low to high impedance, and between each regulator when turning on. These considerations require a rise time of at least 200 ms for the pull-up resistor (R_{PULLUP}) and the load capacitor (C_L). The sum of the resistance of R_{MIRROR} and R_{PULLUP} must be large enough to charge the capacitor longer than the minimum required delay. For a symmetrical mirrored power-down sequence, the value of R_{MIRROR} must be much larger than R_{PULLUP}. A 10 kΩ R_{PULLUP} value limits the pull-down current to 100 μA while giving a reasonable value for R_{MIRROR}. A typical 1 μF capacitor together with a 150 kΩ R_{MIRROR} value gives a value of

$$t_{MAX} = 2.197((160 \times 10^3) \times (1 \times 10^{-6})) = 351 \text{ ms} \quad (36)$$

The threshold voltage required by each comparator is set by Equation 28 to Equation 31. For example,

$$V1 = V_{REF}\left(1 - e^{\frac{-50 \times 10^{-3}}{160 \times 10^3 \times 1 \times 10^{-6}}}\right)$$

where $V1$ = 268.38 mV.

Therefore, V2 = 464.74 mV, V3 = 608.39 mV, and V4 = 713.5 mV.

Next, consider 10 μA as the maximum current (I_{DIV}) flowing through the resistor divider network. This current gives the total resistance of the divider network (R_{DIV}) and the individual resistor values using Equation 22 to Equation 27, resulting in the following:

- R_{DIV} = 100 kΩ
- R1 = 26.84 kΩ ≈ 26.7 kΩ
- R2 = 19.64 kΩ ≈ 19.6 kΩ
- R3 = 14.37 kΩ ≈ 14.3 kΩ
- R4 = 10.51 kΩ ≈ 10.5 kΩ
- R5 = 28.65 kΩ ≈ 28.7 kΩ

Resistor values from the calculation are nonindustry standard, using industry standard resistor values resulted in a new R_{DIV} value of 99.8 kΩ. Due to the discrepancy of the calculated resistor value to the industry standard value, the threshold of each comparator also changed. Calculate the new threshold values by using a simple voltage divider formula:

$$V1 = V_{REF}R1/R_{DIV} \quad (37)$$

where $V1 = \frac{1\text{ V}(26.7\text{ k}\Omega)}{99.8\text{ k}\Omega} = 267.54\text{ mV}$.

Therefore, V2 = 463.93 mV, V3 = 607.21 mV, and V4 = 712.42 mV.

Because the threshold of each comparator has changed, the time when each comparator changes its output has also changed. Calculate the new delay values for each comparator by using the following equation:

$$t_1 = -C_L(R_{PULLUP} + R_{MIRROR})\ln\left(1 - \frac{V1}{V_{REF}}\right) \quad (38)$$

where $t_1 = -1\ \mu\text{F}(10\text{ k}\Omega + 150\text{ k}\Omega)\ln\left(1 - \frac{267.54\text{ mV}}{1}\right) = 49.81\text{ ms}$.

Therefore, t_2 = 99.78 ms, t_3 = 149.52 ms, and t_4 = 199.4 ms.

To calculate t_5 through t_8, use Equation 32 to Equation 35:

$$t_5 = -R_{MIRROR}C_L ln\left(\frac{V4}{V_{REF}}\right)$$

where $t_5 = -150\text{ k}\Omega \times 1\ \mu\text{F} \times \ln\left(\frac{712.42\text{ mV}}{1}\right) = 50.86\text{ ms}$.

Therefore, t_6 = 74.83 ms, t_7 = 115.2 ms, and t_8 = 197.78 ms.

THRESHOLD AND TIMEOUT PROGRAMMABLE VOLTAGE SUPERVISOR

Figure 29 shows a circuit configuration for a programmable threshold and timeout circuit. The timeout, t_{RESET}, defines the duration that the input voltage (V_{IN}) must be kept above the threshold voltage to toggle the $\overline{RESET}$ signal, preventing the device from operating when V_{IN} is not stable. If V_{IN} falls below the threshold voltage, the $\overline{RESET}$ signal toggles quickly.

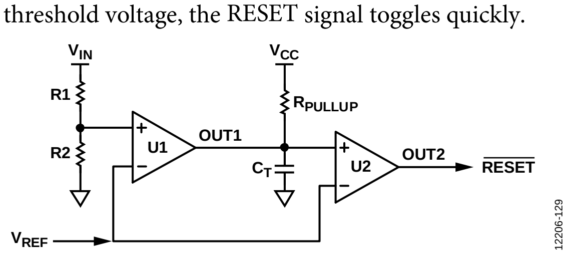

Figure 29. Programmable Threshold and Timeout Circuit

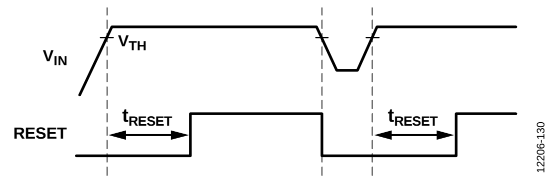

Figure 30. Threshold and Timeout Programmable Voltage Supervisor Timing Diagram

During startup, the ADCMP391 guarantees a low output state when V_{CC} is still below the UVLO threshold, preventing the voltage supervisor from toggling.

When V_{IN} reaches the threshold set by the resistor divider (R1 and R2) and V_{REF}, OUT1 changes from low to high and starts to charge the timeout capacitor (C_T). If V_{IN} is kept above the threshold voltage and the voltage in C_T reaches V_{REF}, OUT2 toggles. If V_{IN} falls below the threshold voltage while C_T is charging, the timeout capacitor quickly discharges, preventing OUT2 from toggling while V_{IN} is not stable.

In the condition that V_{IN} is tied to V_{CC}, the circuit operates when V_{CC} is more than the minimum operating voltage.

The threshold voltage (V_{TH}) is configured by changing the resistor divider or V_{REF}. Calculate the threshold voltage by

$$V_{TH} = V_{REF}\left(1 + \frac{R1}{R2}\right) \quad (39)$$

Timeout is adjusted by changing the values of the pull-up resistor or the timeout capacitor. To set the timeout value, determine the allowable current flowing through R_{PULLUP} and I_{PULLUP}. When I_{PULLUP} is known, calculate R_{PULLUP} and C_T by the following formulas:

$$R_{PULLUP} = V_{CC}/I_{PULLUP} \quad (40)$$

$$C_T = \frac{-t_{RESET}}{R_{PULLUP}\ln\left(1 - \frac{V_{REF}}{V_{CC}}\right)} \quad (41)$$

OUTLINE DIMENSIONS

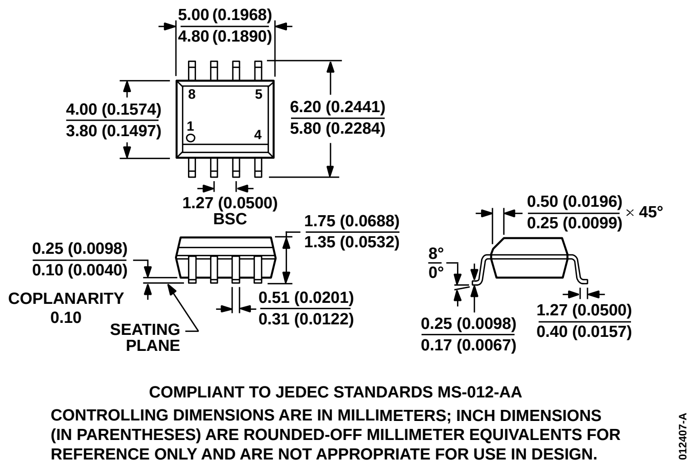

Figure 31. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADCMP391ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADCMP391ARZ-RL7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

[1] Z = RoHS Compliant Part.