HV9980

3-Channel LED Array Driver IC

Features

- Integrated 200V, 25Ω (Typical) MOSFETs
- Programmable Output Current of up to 80 mA per Channel
- TTL-Compatible PWM Dimming Inputs
- Three-Phase Synchronous Operation
- Leading Edge Blanking
- Individual Channel Short-Circuit Protection with Skip Mode
- Overtemperature Protection

Applications

- LCD Panel Backlighting
- DLP RPTV or Projector LED Engine Driver
- RGB Decorative Lighting
- General LED Lighting

General Description

The HV9980 is a fully integrated 3-channel peak-current PWM controller for driving buck converters in Constant Output Current mode. It is optimized for use with a large array of 20 mA to 80 mA LED strings, where multiple HV9980 ICs are used, sharing a common clock and a common reference voltage.

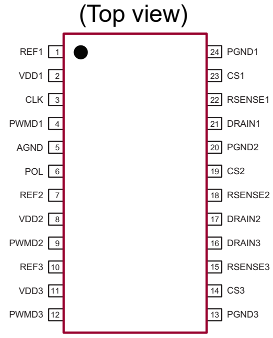
Both the clock and the voltage reference are external to the HV9980 for improved output current accuracy and uniform illumination. The output currents are programmed by controlling peak source current in each of the three internal 200V, 25Ω switching MOSFETs.

The peak current is detected by monitoring voltage at external sense resistors connected to RSENSE1-3. The switching MOSFET is turned off when the corresponding current sense signal exceeds the reference voltage applied at REF1-3 (in the case of normal output signal polarity). The beginning of the next switching cycle is determined by the external clock signal received at the CLK input. All three channels operate at a switching frequency of 1/6 of the external clock frequency and positioned 120º out-of-phase for the purpose of input and output ripple current reduction. Each channel is protected from an output Short-circuit condition. When an Overcurrent condition is detected in the output switch (RSENSE1-3), the corresponding channel shuts down for 200 µs. The HV9980 recovers automatically, when the Short-circuit Overcurrent condition is removed. Each current sense input (CS1-CS3) is equipped with a leading edge blanking delay to prevent false triggering of the current sense comparators due to circuit parasitics.

Overtemperature protection is included to prevent destructive failures due to overheating. Programmable slope compensation is available at each CS input. AGND and PGND1-3 must be tied together on the printed circuit board (PCB). VDD1-3 must be also connected together on the PCB.

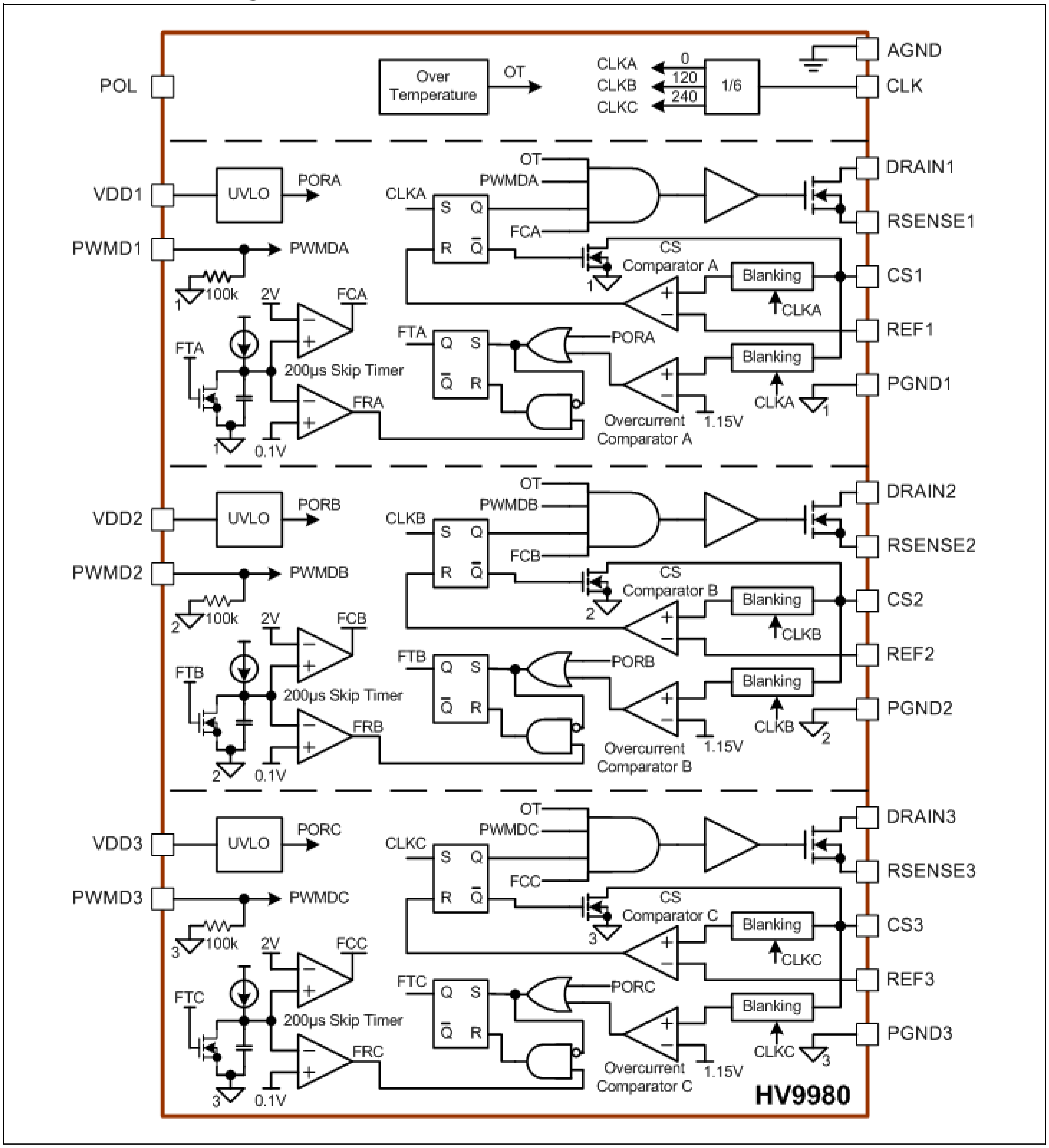
Package Type

24-lead SOW
(Top view)

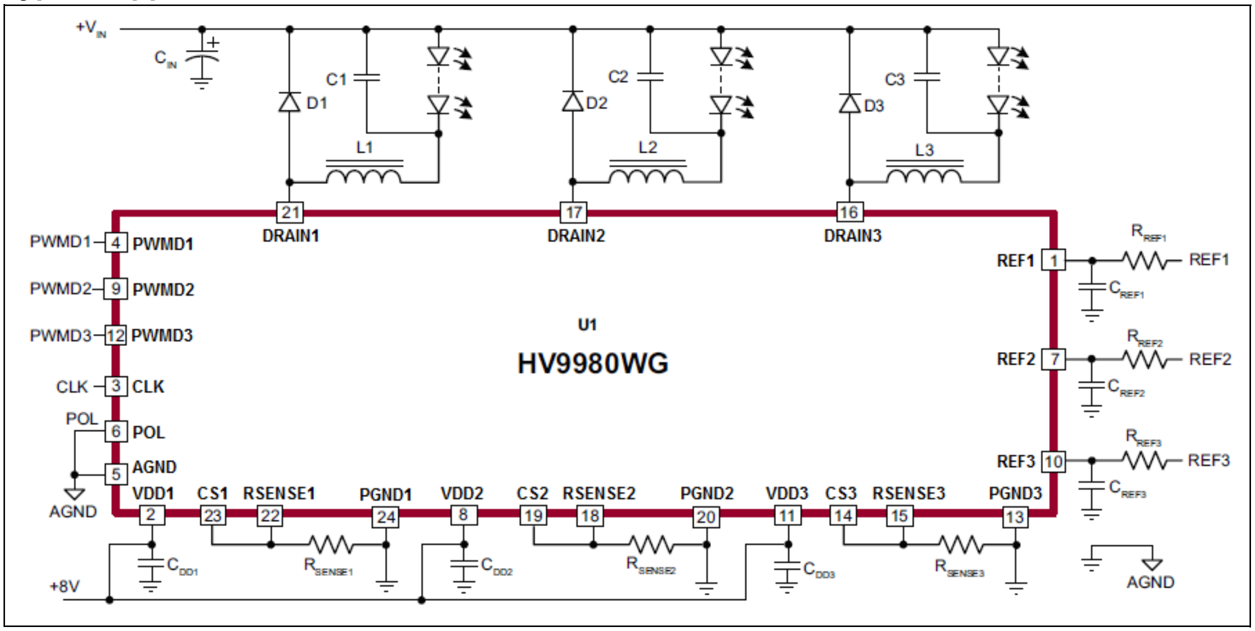


See Table 3-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage, V_{DD1-3} .... –0.3V to +10V
DRAIN1–3 Outputs .... –0.3V to +200V
CS1–3 Inputs .... –0.3V to +5V
Other Inputs and Outputs .... –0.3V to V_{DD}
Supply Current, I_{DD} .... +10 mA
Junction Temperature, T_J (Note 1) .... –40°C to +150°C
Storage Temperature Range, T_S .... –65°C to +150°C
Power Dissipation (T_A= +25°C)
24-lead SOW .... 1300 mW

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Operation out of this range will be destructive to the IC.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C and V_{DD} = 8V unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
SUPPLY INPUT (VDD1, VDD2, and VDD3)						
V_{DD} Supply Voltage Range	V_{DD}	6	—	9.5	V	
V_{DD} Undervoltage Lower Threshold	$V_{DD(UVLOF)}$	—	—	5.3	V	V_{DD} falling (Note 1)
V_{DD} Undervoltage Hysteresis	$\Delta V_{DD(UVLO)}$	—	500	—	mV	
Operating Supply Current	I_{DD}	—	—	3	mA	Total of V_{DD1} + V_{DD2} + V_{DD3} (Note 1)
HIGH VOLTAGE SWITCHES (DRAIN1 – RSENSE1, DRAIN2–RSENSE2, AND DRAIN3 – RSENSE3)						
Breakdown Voltage	V_{BR}	210	—	—	V	Note 1
On-Resistance	R_{ON}	—	25	45	Ω	I_{DRAIN} = 50 mA, V_{RSENSE} = 0V
Drain Saturation Current	I_{SAT}	200	300	—	mA	V_{DRAIN} = 120V, V_{RSENSE} = 1.3V (Note 1)
CURRENT SENSE COMPARATORS (CS1 – REF1, CS2 – REF2, AND CS3 – REF3)						
Short-Circuit Protection Overcurrent Limit Threshold	$V_{CS(LIM)}$	1	1.15	1.3	V	Note 1
Short-Circuit Recovery Delay	T_{SKIP}	—	200	—	µs	
Leading Edge Blanking Delay	T_{BLANK}	120	—	220	ns	
Input Offset Voltage	V_{OS}	–7	—	7	mV	Note 1
Propagation Delay CS-to-DRAIN	T_{DELAY}	—	—	150	ns	V_{CS}–V_{REF} = 50 mV (Note 1)
Short-Circuit Protection Delay CS-to-DRAIN	$T_{DELAY(LIM)}$	—	—	0.5	µs	V_{CS} = $V_{CS(LIM)}$ + 100 mV, V_{REF} > $V_{CS(LIM)}$ (Note 1)
OSCILLATOR INPUT AND FREQUENCY DIVIDER (CLK)						
Maximum Switching Frequency	$F_{SW(MAX)}$	500	—	—	kHz	f_{CLK} = 3 MHz (Note 1)
Frequency Divider Ratio	K_{SW}	—	6	—	—	Note 2

Note 1: The specifications which apply over the full operating temperature range at –40°C < T_A < +85°C are guaranteed by design and characterization.
2: Guaranteed by design

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: T_A = 25°C and V_{DD} = 8V unless otherwise specified.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
DRAIN1-DRAIN2 Phase Delay	φ_2	—	120	—	deg	Note 2
DRAIN1-DRAIN3 Phase Delay	φ_3	—	240	—	deg	Note 2
CLK High Time	T_{OFF}	50	—	—	ns	
CLK Low Time	T_{ON}	50	—	—	ns	
CLK Input High Voltage	$V_{CLK(HI)}$	2	—	—	V	Note 1
CLK Input Low Voltage	$V_{CLK(LO)}$	—	—	0.8	V	Note 1
PWM DIMMING (PWMD1, PWMD2 AND PWMD3)						
PWMD Input Low Voltage	$V_{PWMD(LO)}$	—	—	0.8	V	Note 1
PWMD Input High Voltage	$V_{PWMD(HI)}$	2	—	—	V	Note 1
PWMD Pull-Down Resistance	R_{PWMD}	100	200	300	kΩ	V_{PWMD} = 5V
OVERTEMPERATURE PROTECTION						
Overtemperature Trip Limit	T_{OT}	125	140	—	°C	Note 1
Overtemperature Hysteresis	T_{OTHYST}	—	60	—	°C	Note 1

Note 1: The specifications which apply over the full operating temperature range at –40°C < T_A < +85°C are guaranteed by design and characterization.

2: Guaranteed by design

TEMPERATURE SPECIFICATIONS

Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–40	—	+85	°C	
Operating Junction Temperature	T_J	–40	—	+125	°C	
Maximum Junction Temperature	$T_{J(ABSMAX)}$	—	—	+150	°C	
Storage Temperature	Ts	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
24-lead SOW	θ_{JA}	—	60	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

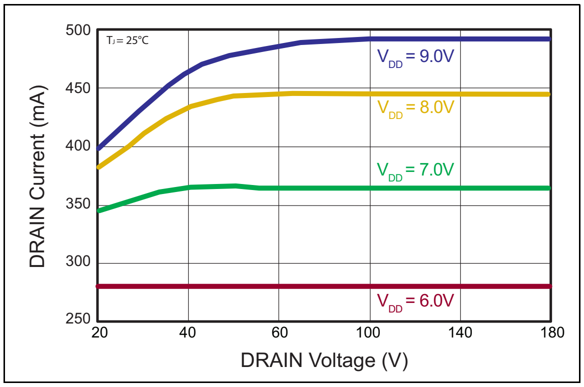


FIGURE 2-1: *Output Saturation Current (I_{DRAIN} vs. V_{DRAIN} at V_{RSENSE} = 0V).*

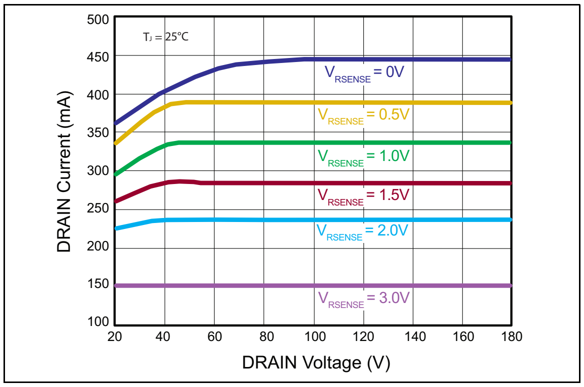


FIGURE 2-2: *Output Saturation Current (I_{DRAIN} vs. V_{DRAIN} at V_{DD} = 8V).*

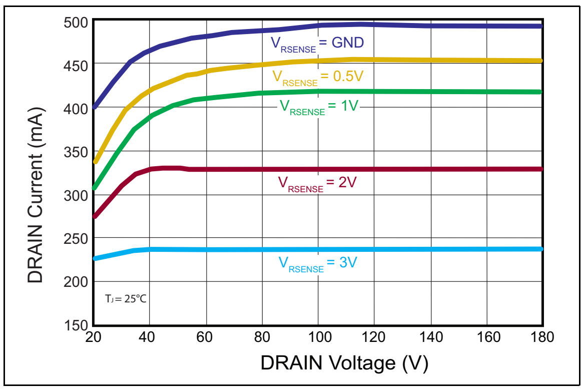


FIGURE 2-3: *Output Saturation Current (I_{DRAIN} vs. V_{DRAIN} at V_{DD} = 9V).*

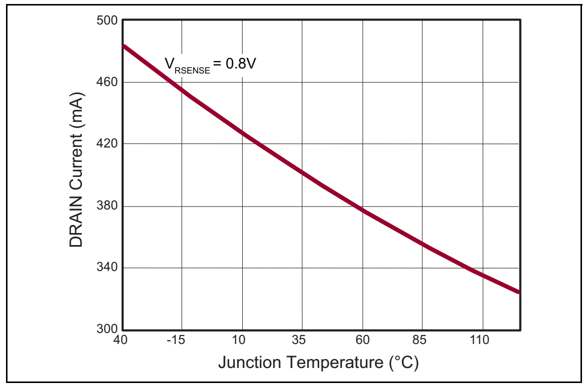


FIGURE 2-4: *Output Saturation Current (I_{DRAIN} vs. T_J at V_{DD} = 9V).*

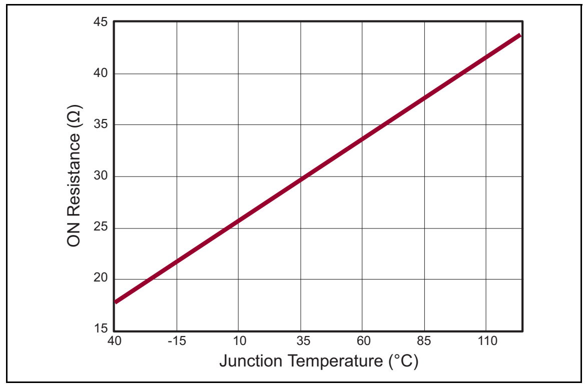


FIGURE 2-5: *ON Resistance (R_{ON} vs. T_J at V_{DD} = 8V or 9V).*

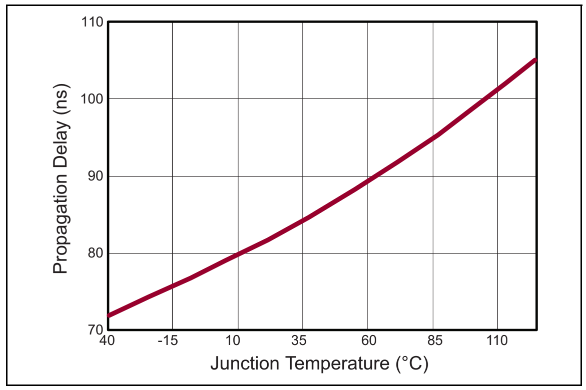


FIGURE 2-6: *CS-to-DRAIN Propagation Delay (T_{DELAY} vs. T_J at V_{DD} = 8V or 9V).*

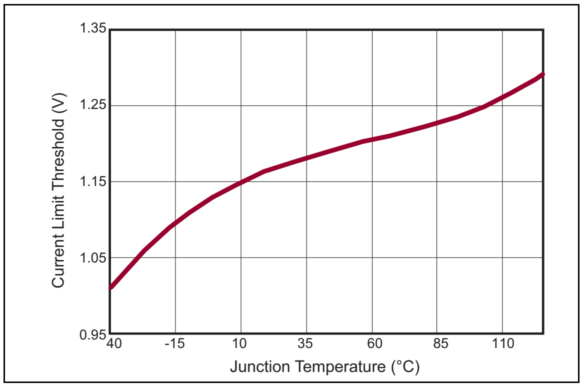


FIGURE 2-7: *Short Circuit Current Limit Threshold Voltage ($V_{CS(LIM)}$ vs. T_J at V_{DD} = 8V or 9V).*

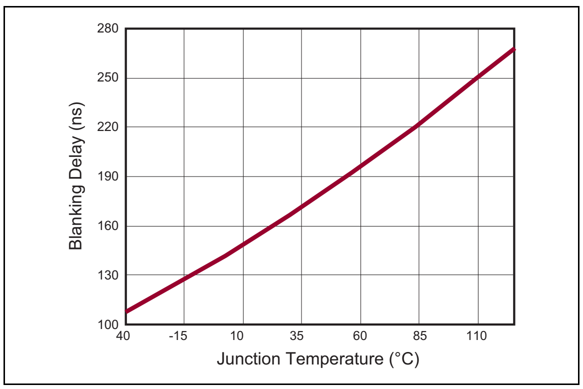


FIGURE 2-8: *Leading Edge Blanking Delay (T_{BLANK} vs. T_J at V_{DD} = 8V or 9V).*

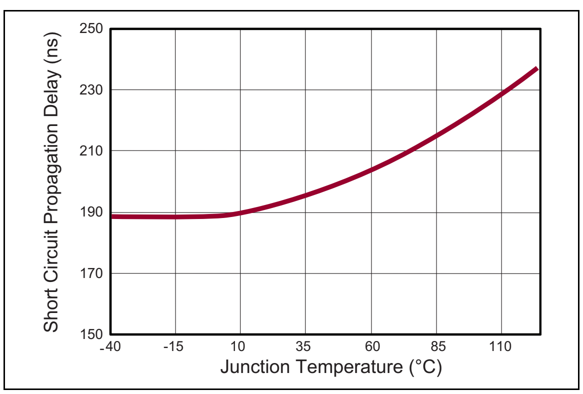


FIGURE 2-9: *Short-Circuit Protection Delay ($T_{DELAY(LIM)}$ vs. T_J at V_{DD} = 8V or 9V).*

3.0 PIN DESCRIPTION

Table 3-1 shows the description of pins in HV9980.
Refer to **Package Type** for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	REF1	Voltage reference input to the current sense comparator. For best noise immunity, connect an RC filter at this pin referenced to the corresponding PGND1 pin. The filter can consist of a 1 nF low-impedance capacitor and a 1 kΩ resistor.
2	VDD1	Power supply input. For best noise immunity, bypass this pin to the corresponding PGND1 pin with a 0.1 µF low-impedance capacitor. The VDD pins must be tied together on the PCB.
3	CLK	Input to an external clock signal common to all three channels. Programs the switching frequency of the power MOSFET outputs at 1/6 of the clock signal frequency.
4	PWMD1	Dedicated PWM dimming input for individual LED string driver Channel 1
5	AGND	Common return pin for CLK, POL and PWMD inputs
6	POL	Must be connected to AGND
7	REF2	Voltage reference input to the current sense comparator. For best noise immunity, connect an RC filter at this pin referenced to the corresponding PGND2 pin. The filter can consist of a 1 nF low-impedance capacitor and a 1 kΩ resistor.
8	VDD2	Power supply input. For best noise immunity, bypass this pin to the corresponding PGND2 pin with a 0.1 µF low-impedance capacitor. The VDD pins must be tied together on the PCB.
9	PWMD2	Dedicated PWM dimming input for individual LED string driver Channel 2
10	REF3	Voltage reference input to the current sense comparator. For best noise immunity, connect an RC filter at this pin referenced to the corresponding PGND3 pin. The filter can consist of a 1 nF low-impedance capacitor and a 1 kΩ resistor.
11	VDD3	Power supply input. For best noise immunity, bypass this pin to the corresponding PGND3 pin with a 0.1 µF low-impedance capacitor. The VDD pins must be tied together on the PCB.
12	PWMD3	Dedicated PWM dimming input for individual LED string driver Channel 3
13	PGND3	Power return terminal for corresponding DRAIN3. The PGND and AGND pins must be tied together on the PCB.
14	CS3	Signal input to the current sense comparator. Connect this pin to the corresponding RSENSE3 output directly when the slope compensation feature is not used. When the slope compensation is needed, connect a capacitor between RSENSE3 and its corresponding CS3 pin, and connect a resistor between CS3 pin and VDD3.
15	RSENSE3	Open source output of the Channel 3 switching power MOSFET. Connect a current sense resistor between the RSENSE3 pin and its corresponding PGND3 pin.
16	DRAIN3	Open DRAIN output of the switching power MOSFET in Channel 3
17	DRAIN2	Open DRAIN output of the switching power MOSFET in Channel 2
18	RSENSE2	Open source output of the Channel 2 switching power MOSFET. Connect a current sense resistor between the RSENSE2 pin and its corresponding PGND2 pin.
19	CS2	Signal input to the current sense comparator. Connect this pin to the corresponding RSENSE2 output directly when the slope compensation feature is not used. When the slope compensation is needed, connect a capacitor between RSENSE2 and its corresponding CS2 pin, and connect a resistor between CS2 and VDD2.
20	PGND2	Power return terminal for corresponding DRAIN2 output. The PGND and AGND pins must be tied together on the PCB.
21	DRAIN1	Open DRAIN output of the switching power MOSFET in Channel 1
22	RSENSE1	Open source output of the Channel 1 switching power MOSFET. Connect a current sense resistor between the RSENSE1 pin and its corresponding PGND1 pin.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
23	CS1	Signal input to the current sense comparator. Connect this pin to the corresponding RSENSE1 output directly when the slope compensation feature is not used. When the slope compensation is needed, connect a capacitor between RSENSE1 and its corresponding CS1 pin, and connect a resistor between CS1 pin and VDD1.
24	PGND1	Power return terminal for corresponding DRAIN1 output. The PGND and AGND pins must be tied together on the PCB.

4.0 APPLICATION INFORMATION

4.1 Programming LED Current and Selecting L and D

The required value of the output inductor, L, is inversely proportional to the ripple current, ΔI_O, in it. Setting the relative peak-to-peak ripple to 20% to 30% of the average output current is a good practice to ensure the noise immunity of the current sense comparator. See Equation 4-3.

EQUATION 4-1:

$$L = \frac{(V_O \times T_{OFF})}{\Delta I_O} = \frac{(V_O \times [1 - D])}{f_S \Delta I_O}$$

Where V_O is the forward voltage of the LED string, f_S is the switching frequency, and $D = V_O/V_{IN}$ is the switching duty cycle.

The output current in each LED string (I_O) is calculated as shown in Equation 4-2.

EQUATION 4-2:

$$I_O = \left(\frac{V_{REF}}{R_{SENSE}}\right) - \frac{1}{2} \times \Delta I_O$$

Where V_{REF} is the voltage at REF1-3 and R_{SENSE} is the current sense resistor at RSENSE1-3. The ripple current introduces a peak-to-average error in the output current setting that needs to be accounted for.

Adding a filter capacitor across the LED string can reduce the output current ripple, yielding a reduced value of L. However, one must keep in mind that the peak-to-average current error is affected by the variation of the input and output voltage. Therefore, the line-and-load regulation of the LED current might be sacrificed at large ripple current in L.

Another important aspect of designing each LED driver channel with the HV9980 is related to certain parasitic elements of the circuit, including distributed coil capacitance C_L of L, junction capacitance, C_J, and reverse recovery time, t_{rr}, of the rectifier diode, D, capacitance of the PCB traces, C_{PCB}, and output capacitance, C_{DRAIN}, of the controller itself. These parasitic elements affect the efficiency of the switching converter and could potentially cause false triggering of the current sense comparator if not properly managed. Minimizing these parasitics is essential for efficient and reliable operation of the HV9980.

Coil capacitance of inductors is typically provided in the manufacturer's data books either directly or in terms of the self-resonant frequency (SRF). Refer to Equation 4-3.

EQUATION 4-3:

$$SRF = \frac{1}{(2\pi\sqrt{L \times C_L})}$$

Where L is the inductance value, and C_L is the coil capacitance for the inductor in each driver channel.

Charging and discharging this capacitance every switching cycle causes high-current spikes in the LED string. Therefore, connecting a small capacitor, C_O (~10 nF), is recommended to bypass these spikes.

Using an ultra-fast rectifier diode for D is recommended to achieve high efficiency and reduce the risk of false triggering of the current sense comparator. Using diodes with shorter reverse recovery time, t_{rr}, and lower junction capacitance, C_J, achieves better performance. The reverse voltage rating, V_R, of the diode must be greater than the maximum input voltage of the LED lamp.

The total parasitic capacitance present at the DRAIN output of the HV9980 can be calculated as shown in Equation 4-5.

EQUATION 4-4:

$$C_P = C_{DRAIN} + C_{PCB} + C_L + C_J$$

When the switch turns on, the capacitance, C_P, is discharged into the DRAIN output of the IC. The discharge current is limited to typically 300 mA of the internal MOSFET switch saturation current. However, it may become lower at increased junction temperature. The duration of the leading edge current spike can be estimated as shown in Equation 4-5.

EQUATION 4-5:

$$T_{SPIKE} = [(V_{IN} \bullet C_P)/I_{SAT}] + t_{rr}$$

In order to avoid false triggering of the current sense comparator C_P must be minimized in accordance with Equation 4-6.

EQUATION 4-6:

$$C_P < \frac{(I_{SAT} \times [T_{BLANK(MIN)} - t_{rr}])}{V_{IN(MAX)}}$$

Where $T_{BLANK(MIN)}$ is the minimum blanking time 120 ns, and $V_{(INMAX)}$ is the maximum instantaneous input voltage.

4.2 Layout Considerations

The HV9980 provides three independent power ground connections, PGND1-3, for each channel. The PGND pins must be wired together on the PCB. To minimize interference between the channels, the PGND pins should be wired to the negative terminal of the input filter capacitor, $C_{IN,}$ using separate tracks. All three power supply inputs VDD1, VDD2, and VDD3 must also be connected together on the PCB.

Although in many layout arrangements wiring the reference pins, REF1-3, together is acceptable, further reduction of the "cross-talk" between the channels is possible by adding low-pass RC filters with the filter capacitors referenced to the corresponding PGND pins. These filters composed from R_{REF1-3} and C_{REF1-3} are shown in the **Typical Application Circuit**.

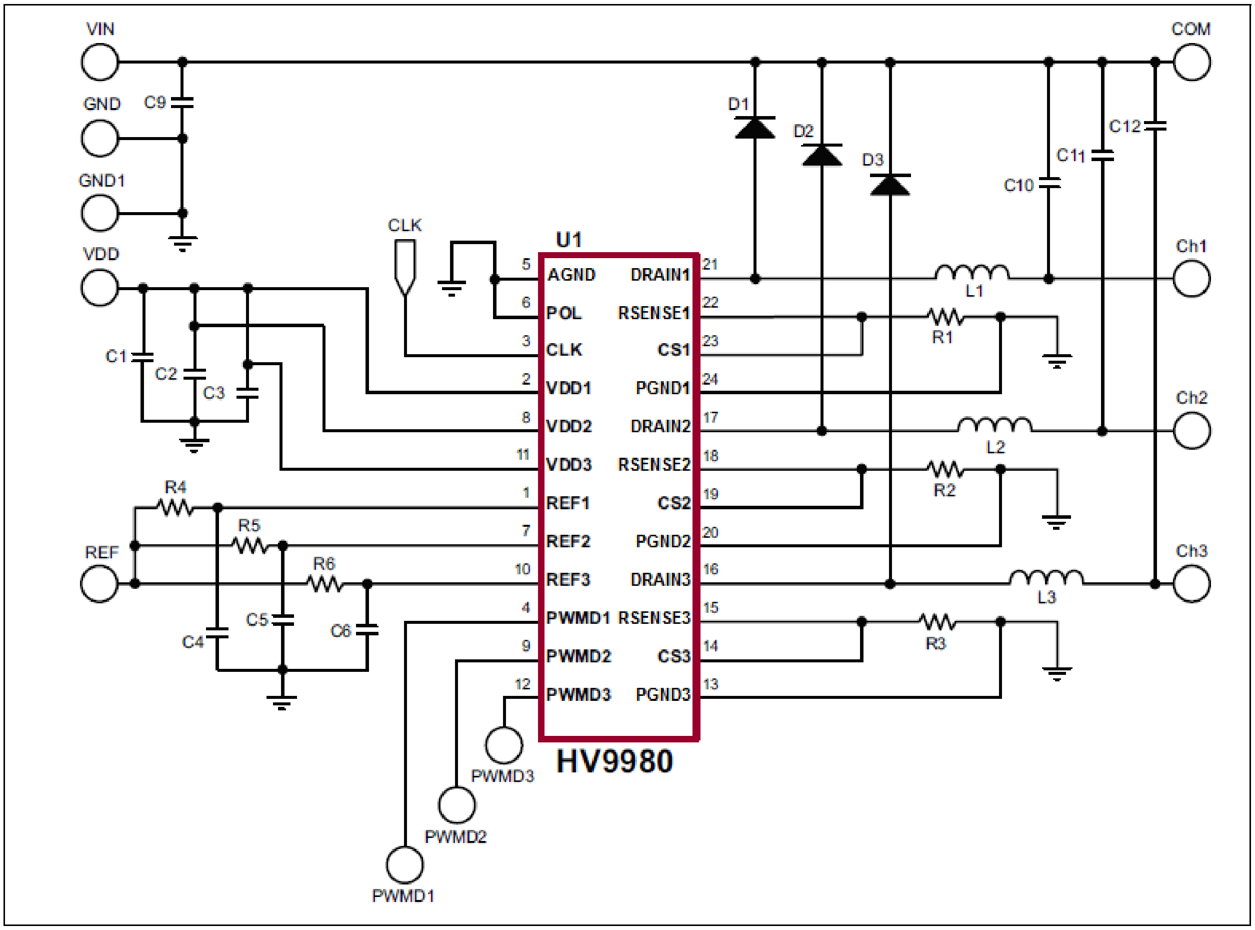


FIGURE 4-1: 110 VDC–190 VDC 3-channel 50V 70 mA LED Driver Schematic.

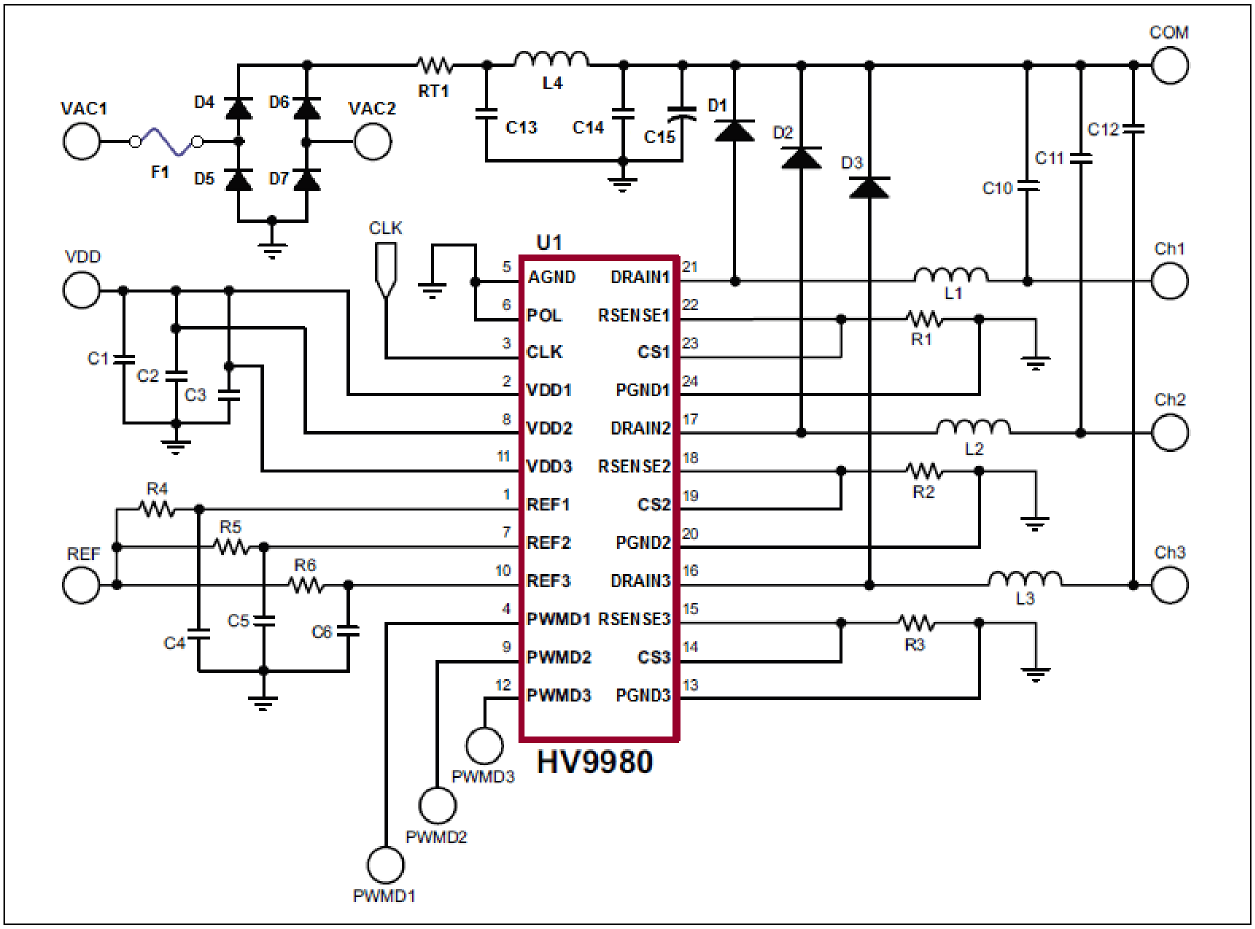
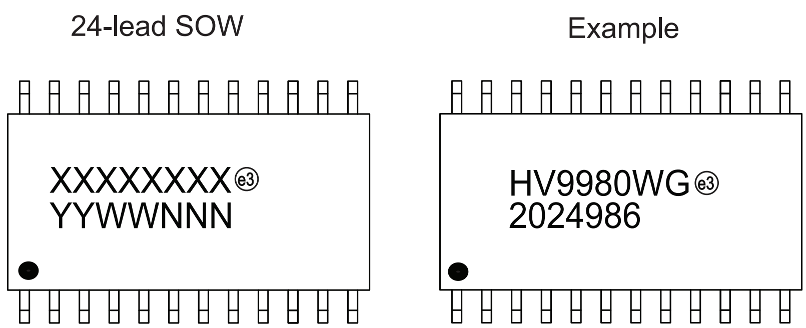


FIGURE 4-2: *90 VAC–135 VAC 3-channel 50V 70 mA LED Driver Schematic.*

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

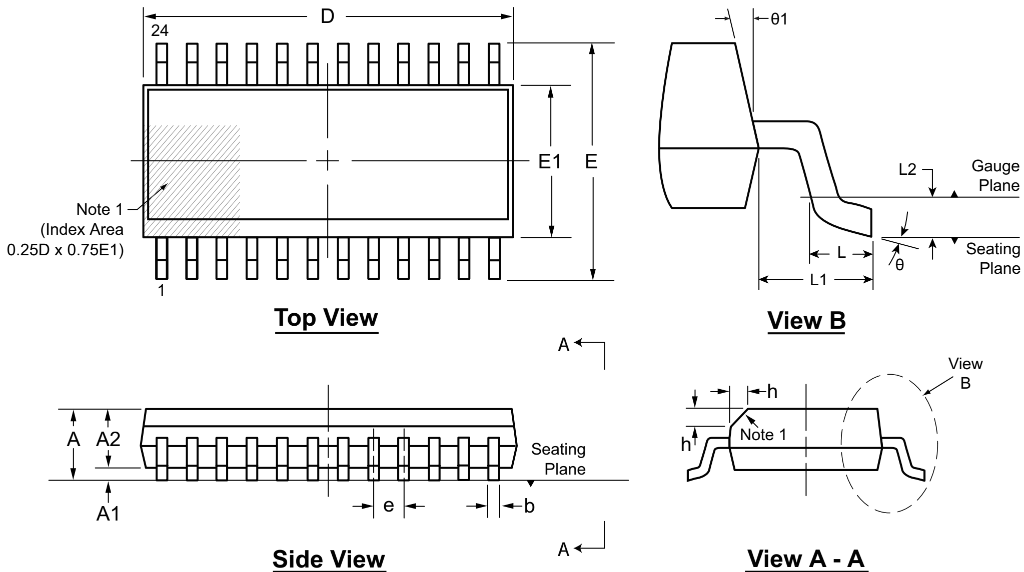


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

24-Lead SOW (Wide Body) Package Outline (WG)

15.40x7.50 body, 2.65mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.15*	0.10	2.05	0.31	15.20*	9.97*	7.40*		0.25	0.40			0°	5°
	NOM	-	-	-	-	15.40	10.30	7.50	1.27 BSC	-	-	1.40 REF	0.25 BSC	-	-
	MAX	2.65	0.30	2.55*	0.51	15.60*	10.63*	7.60*		0.75	1.27			8°	15°

JEDEC Registration MS-013, Variation AD, Issue E, Sep. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.

APPENDIX A: REVISION HISTORY

Revision A (January 2020)

- Converted Supertex Document # DSFP-HV9980 to DS20005915A
- Changed the package marking format
- Made minor changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV9980	=	3-Channel LED Array Driver IC
Package:	WG	=	24-lead SOW
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	1000/Reel for a WG Package

Example:

a) HV9980WG-G: 3-Channel LED Array Driver IC, 24-lead SOW Package, 1000/Reel

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