

NUD4011

Low Current LED Driver

This device is designed to replace discrete solutions for driving LEDs in AC/DC high voltage applications (up to 200 V). An external resistor allows the circuit designer to set the drive current for different LED arrays. This discrete integration technology eliminates individual components by combining them into a single package, which results in a significant reduction of both system cost and board space. The device is a small surface mount package (SO-8).

Features

- Supplies Constant LED Current for Varying Input Voltages
- External Resistor Allows Designer to Set Current – up to 70 mA
- Offered in Surface Mount Package Technology (SO-8)
- Pb-Free Package is Available

Benefits

- Maintains a Constant Light Output During Battery Drain
- One Device can be used for Many Different LED Products
- Reduces Board Space and Component Count
- Simplifies Circuit and System Designs

Typical Applications

- Portables: For Battery Back-up Applications, also Simple Ni-CAD Battery Charging
- Industrial: General Lighting Applications and Small Appliances
- Automotive: Tail Lights, Directional Lights, Back-up Light, Dome Light

PIN FUNCTION DESCRIPTION

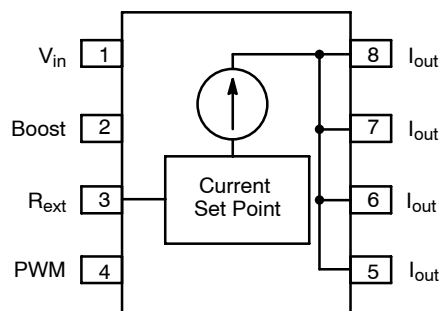
Pin	Symbol	Description
1	V_{in}	Positive input voltage to the device
2	Boost	This pin may be used to drive an external transistor as described in the App Note AND8198/D.
3	R_{ext}	An external resistor between R_{ext} and V_{in} pins sets different current levels for different application needs
4	PWM	For high voltage applications (higher than 48 V), pin 4 is connected to the LEDs array. For low voltage applications (lower than 48 V), pin 4 is connected to ground.
5, 6, 7, 8	I_{out}	The LEDs are connected from these pins to ground



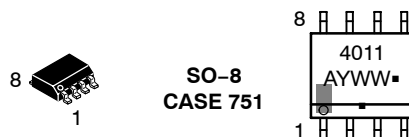
ON Semiconductor®

<http://onsemi.com>

PIN CONFIGURATION AND SCHEMATIC



MARKING DIAGRAM



A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package
 (Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUD4011DR2	SO-8	2500 / Tape & Reel
NUD4011DR2G	SO-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NUD4011

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	200	V
Output Current (For $V_{drop} \leq 16\text{ V}$) (Note 1)	I_{out}	70	mA
Output Voltage	V_{out}	198	V
Human Body Model (HBM)	ESD	500	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. $V_{drop} = V_{in} - 0.7\text{ V} - V_{LEDs}$.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Operating Ambient Temperature	T_A	-40 to +125	$^\circ\text{C}$
Maximum Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 to +150	$^\circ\text{C}$
Total Power Dissipation (Note 2) Derating above 25°C (Figure 3)	P_D	1.13 9.0	W mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	110	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Lead (Note 2)	$R_{\theta JL}$	77	$^\circ\text{C/W}$

2. Mounted on FR-4 board, 2 in sq pad, 1 oz coverage.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Current1 (Note 3) ($V_{in} = 120\text{ Vdc}$, $R_{ext} = 24\ \Omega$, $V_{LEDs} = 90\text{ V}$)	I_{out1}	26.0	27.5	29.5	mA
Output Current2 (Note 3) ($V_{in} = 200\text{ Vdc}$, $R_{ext} = 68\ \Omega$, $V_{LEDs} = 120\text{ V}$)	I_{out2}	11.5	14.0	15.5	mA
Bias Current ($V_{in} = 120\text{ Vdc}$, $R_{ext} = \text{Open}$, $R_{shunt} = 80\text{ k}\Omega$)	I_{Bias}	-	1.1	2.0	mA
Voltage Overhead (Note 4)	V_{over}	5.0	-	-	V

3. Device's pin 4 connected to the LEDs array (as shown in Figure 5).

4. $V_{over} = V_{in} - V_{LEDs}$.

NUD4011

TYPICAL PERFORMANCE CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

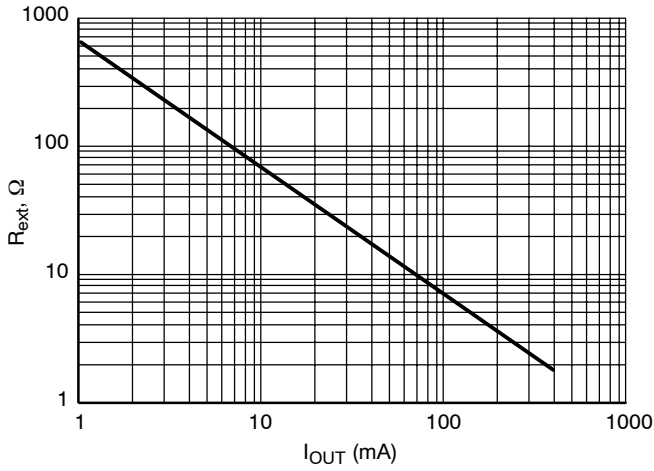


Figure 1. Output Current (I_{OUT}) vs. External Resistor (R_{ext})

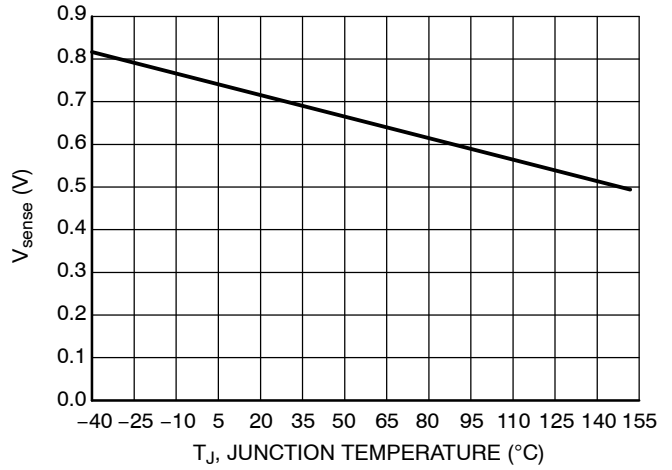


Figure 2. V_{sense} vs. Junction Temperature

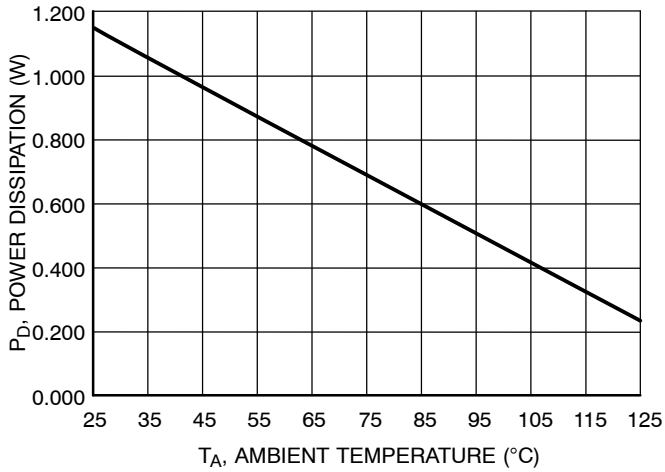


Figure 3. Total Power Dissipation (P_D) vs. Ambient Temperature (T_A)

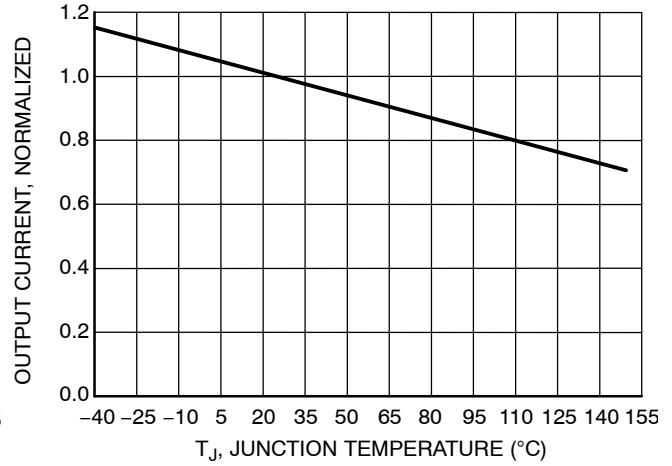


Figure 4. Current Regulation vs. Junction Temperature

APPLICATION INFORMATION

Design Guide for DC Applications

1. Define LED's current:
 - a. $I_{LED} = 30 \text{ mA}$
2. Calculate Resistor Value for R_{ext} :
 - a. $R_{ext} = V_{sense} / I_{LED}$ (see Figure 2)
 - b. $R_{ext} = 0.7(T_J = 25 \text{ }^\circ\text{C}) / 0.030 = 24 \text{ } \Omega$
3. Define V_{in} :
 - a. Per example in Figure 5, $V_{in} = 120 \text{ Vdc}$
4. Define $V_{LED} @ I_{LED}$ per LED supplier's data sheet: per example in Figure 5,
 - a. $V_{LED} = 3.0 \text{ V}$ (30 LEDs in series)
 - b. $V_{LEDs} = 90 \text{ V}$
5. Calculate V_{drop} across the NUD4001 device:
 - a. $V_{drop} = V_{in} - V_{sense} - V_{LEDs}$
 - b. $V_{drop} = 120 \text{ V} - 0.7 \text{ V} - 90 \text{ V}$
 - c. $V_{drop} = 29.3 \text{ V}$
6. Calculate Power Dissipation on the NUD4001 device's driver:
 - a. $P_{D_driver} = V_{drop} * I_{out}$
 - b. $P_{D_driver} = 29.3 \text{ V} \times 0.030 \text{ A}$
 - c. $P_{D_driver} = 0.879 \text{ W}$
7. Establish Power Dissipation on the NUD4001 device's control circuit per below formula:
 - a. $P_{D_control} = (V_{in} - 1.4 - V_{LEDs})^2 / 20,000$
 - b. $P_{D_control} = 0.040 \text{ W}$
8. Calculate Total Power Dissipation on the device:
 - a. $P_{D_total} = P_{D_driver} + P_{D_control}$
 - b. $P_{D_total} = 0.879 \text{ W} + 0.040 \text{ W} = 0.919 \text{ W}$
9. If $P_{D_total} > 1.13 \text{ W}$ (or derated value per Figure 3), then select the most appropriate recourse and repeat steps 1–8:
 - a. Reduce V_{in}
 - b. Reconfigure LED array to reduce V_{drop}
 - c. Reduce I_{out} by increasing R_{ext}
 - d. Use external resistors or parallel device's configuration
10. Calculate the junction temperature using the thermal information on Page 8 and refer to Figure 4 to check the output current drop due to the calculated junction temperature. If desired, compensate it by adjusting the value of R_{ext} .

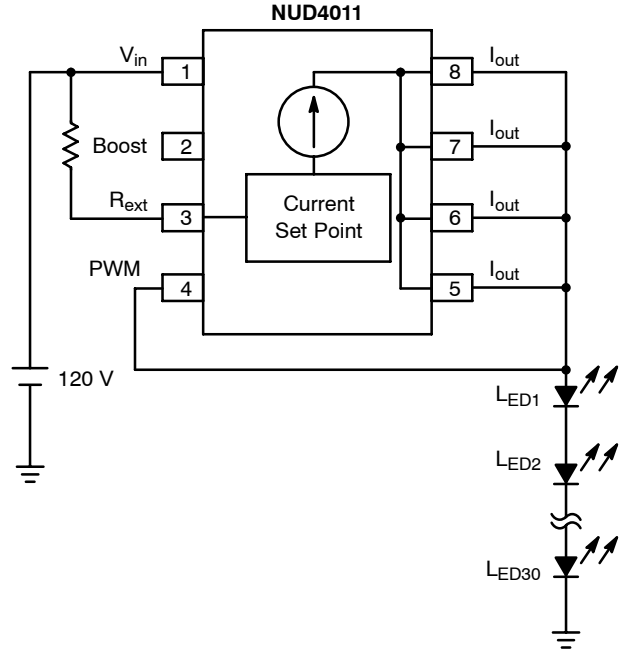


Figure 5. 120 V Application (Series LED's Array)

APPLICATION INFORMATION (continued)

Design Guide for AC Applications

1. Define LED's current:
 - a. $I_{LED} = 30 \text{ mA}$
2. Define V_{in} :
 - a. Per example in Figure 5, $V_{in} = 120 \text{ Vac}$
3. Define $V_{LED} @ I_{LED}$ per LED supplier's data sheet:
 - a. Per example in Figure 6,

$$V_{LED} = 3.0 \text{ V (30 LEDs in series)}$$

$$V_{LEDs} = 90 \text{ V}$$
4. Calculate Resistor Value for R_{ext} :

The calculation of the R_{ext} for AC applications is totally different than for DC. This is because current conduction only occurs during the time that the ac cycles' amplitude is higher than V_{LEDs} . Therefore R_{ext} calculation is now dependent on the peak current value and the conduction time.

 - a. Calculate θ for $V_{LEDs} = 90 \text{ V}$:

$$V = V_{peak} \times \text{Sin } \theta$$

$$90 \text{ V} = (120 \times \sqrt{2}) \times \text{Sin } \theta$$

$$\theta = 32.027^\circ$$
 - b. Calculate conduction time for $\theta = 32.027^\circ$. For a sinusoidal waveform V_{peak} happens at $\theta = 90^\circ$. This translates to 4.165 ms in time for a 60 Hz frequency, therefore 32.027° is 1.48 ms and finally:

$$\text{Conduction time} = (4.165 \text{ ms} - 1.48 \text{ ms}) \times 2$$

$$= 5.37 \text{ ms}$$
 - c. Calculate the I_{peak} needed for $I_{(avg)} = 30 \text{ mA}$
 Since a full bridge rectifier is being used (per Figure 6), the frequency of the voltage signal applied to the NUD4011 device is now 120 Hz. To simplify the calculation, it is assumed that the 120 Hz waveform is square shaped so that the following formula can be used:

$$I_{(avg)} = I_{peak} \times \text{duty cycle};$$
 If 8.33 ms is 100% duty cycle, then 5.37 ms is 64.46%, then:

$$I_{peak} = I_{(avg)} / \text{duty cycle}$$

$$I_{peak} = 30 \text{ mA} / 0.645 = 46 \text{ mA}$$
 - d. Calculate R_{ext}

$$R_{ext} = 0.7 \text{ V} / I_{peak}$$

$$R_{ext} = 15.21 \Omega$$
5. Calculate V_{drop} across the NUD4011 device:
 - a. $V_{drop} = V_{in} - V_{sense} - V_{LEDs}$
 - b. $V_{drop} = 120 \text{ V} - 0.7 \text{ V} - 90 \text{ V}$
 - c. $V_{drop} = 29.3 \text{ V}$

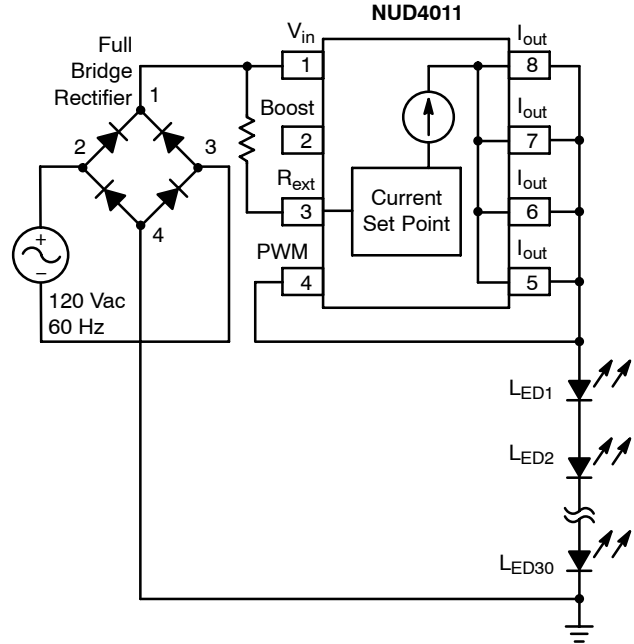


Figure 6. 120 Vac Application (Series LED's array)

6. Calculate Power Dissipation on the NUD4011 device's driver:
 - a. $P_{D_driver} = V_{drop} * I_{(avg)}$
 - b. $P_{D_driver} = 29.3 \text{ V} \times 0.030 \text{ A}$
 - c. $P_{D_driver} = 0.879 \text{ W}$
7. Establish Power Dissipation on the NUD4011 device's control circuit per below formula:
 - a. $P_{D_control} = (V_{in} - 1.4 - V_{LEDs})^2 / 20,000$
 - b. $P_{D_control} = 0.040 \text{ W}$
8. Calculate Total Power Dissipation on the device:
 - a. $P_{D_total} = P_{D_driver} + P_{D_control}$
 - b. $P_{D_total} = 0.879 \text{ W} + 0.040 \text{ W} = 0.919 \text{ W}$
9. If $P_{D_total} > 1.13 \text{ W}$ (or derated value per Figure 3), then select the most appropriate recourse and repeat steps 1-8:
 - a. Reduce V_{in}
 - b. Reconfigure LED array to reduce V_{drop}
 - c. Reduce I_{out} by increasing R_{ext}
 - d. Use external resistors or parallel device's configuration
10. Calculate the junction temperature using the thermal information on Page 8 and refer to Figure 4 to check the output current drop due to the calculated junction temperature. If desired, compensate it by adjusting the value of R_{ext} .

NUD4011

TYPICAL APPLICATION CIRCUITS

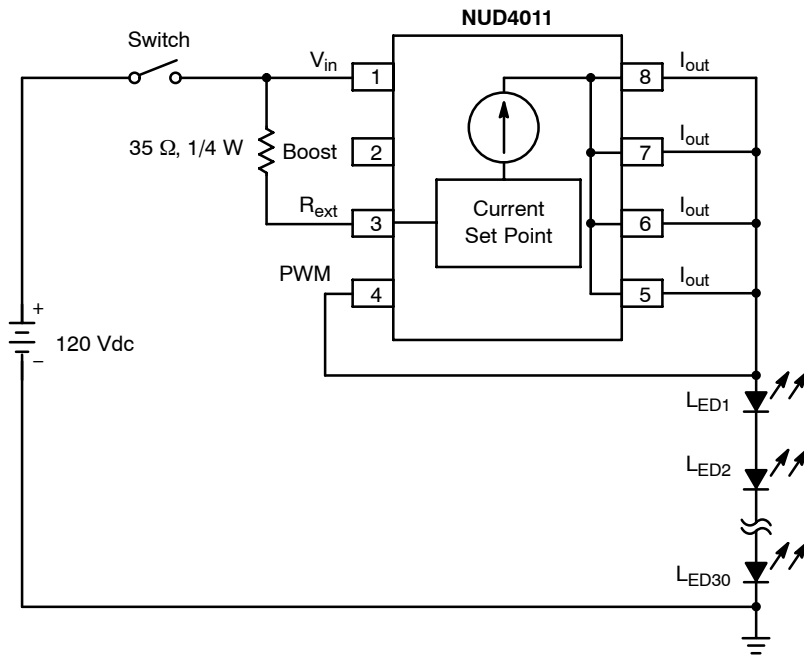


Figure 7. 120 Vdc Application Circuit for a Series Array of 30 LEDs (3.0 V, 20 mA)

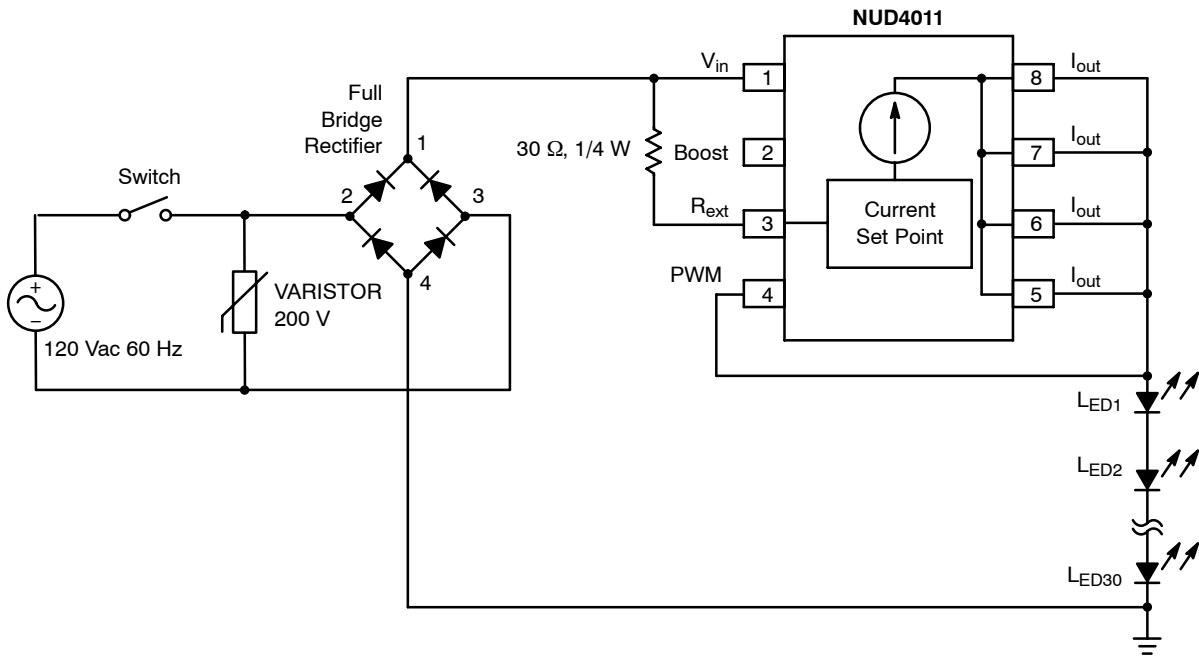


Figure 8. 120 Vac Application Circuit for a Series Array of 30 LEDs (3.0 V, 20 mA)

NUD4011

TYPICAL APPLICATION CIRCUITS (continued)

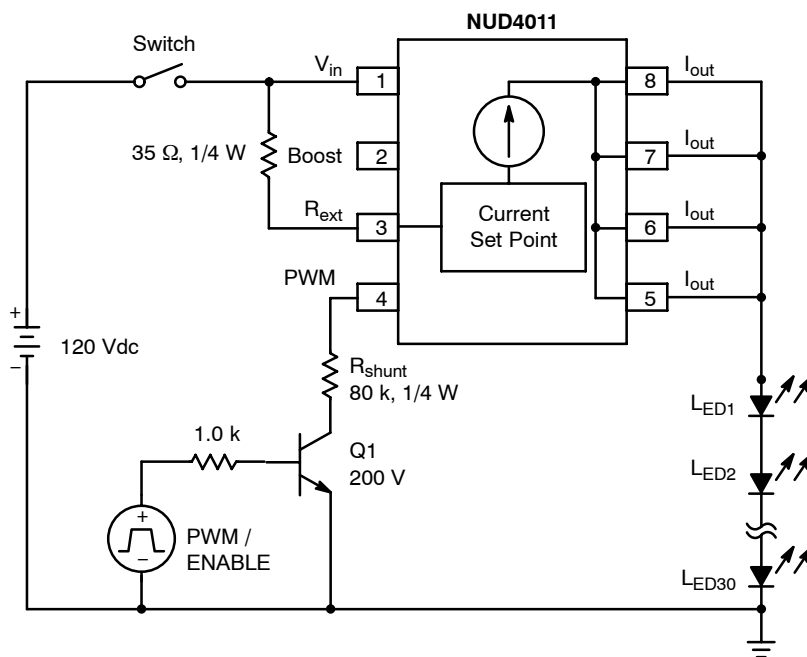


Figure 9. 120 Vdc Application with PWM / Enable Function, 30 LEDs in Series (3.0 V, 20 mA)

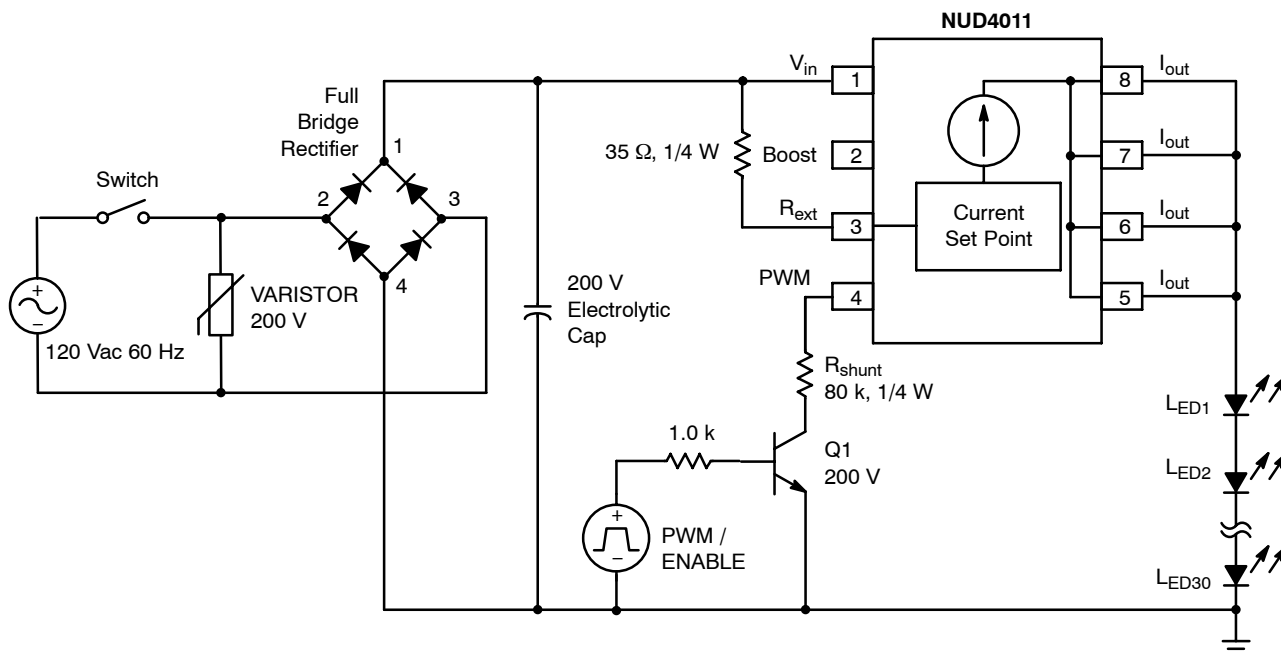


Figure 10. 120 Vac Application with PWM / Enable Function, 30 LEDs in Series (3.0 V, 20 mA)

THERMAL INFORMATION

NUD4011 Power Dissipation

The power dissipation of the SO-8 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A . Using the values provided on the data sheet for the SO-8 package, P_D can be calculated as follows:

$$P_D = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 1.13 W.

$$P_D = \frac{150^{\circ}C - 25^{\circ}C}{110^{\circ}C} = 1.13 W$$

The 110°C/W for the SO-8 package assumes the use of a FR-4 copper board with an area of 2 square inches with 2 oz coverage to achieve a power dissipation of 1.13 W. There are other alternatives to achieving higher dissipation from the SOIC package. One of them is to increase the copper area to

reduce the thermal resistance. Figure 11 shows how the thermal resistance changes for different copper areas. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad or an aluminum core board, the power dissipation can be even doubled using the same footprint.

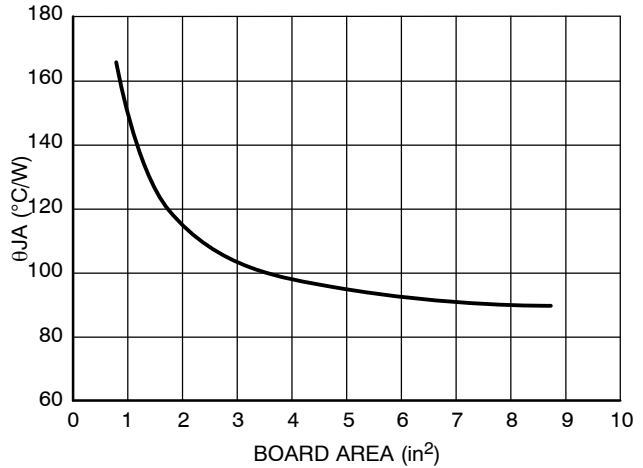


Figure 11. θJA versus Board Area

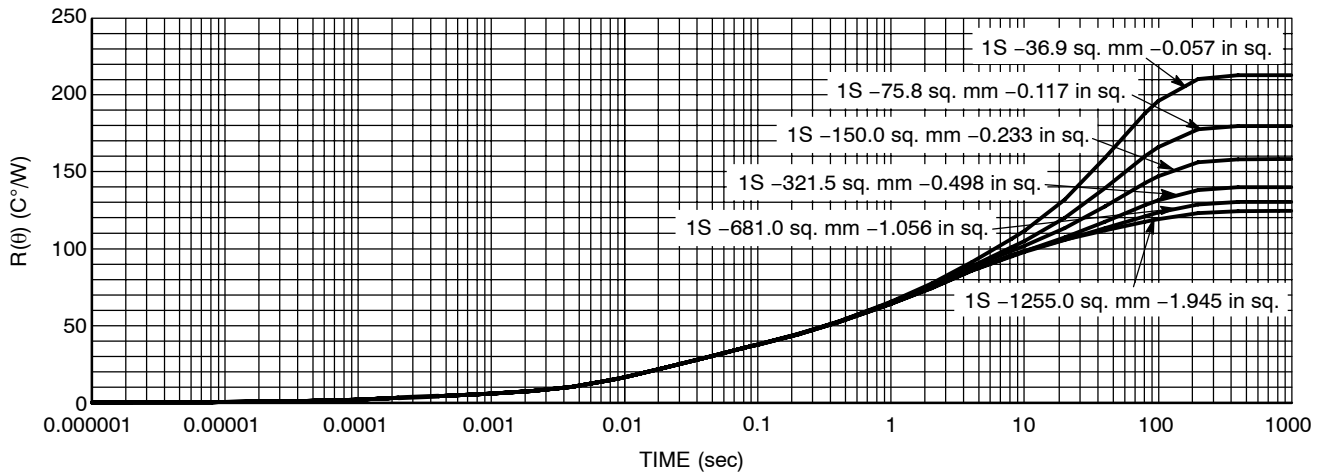


Figure 12. Transient Thermal Response

Thermal Clad is a registered trademark of the Bergquist Company.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

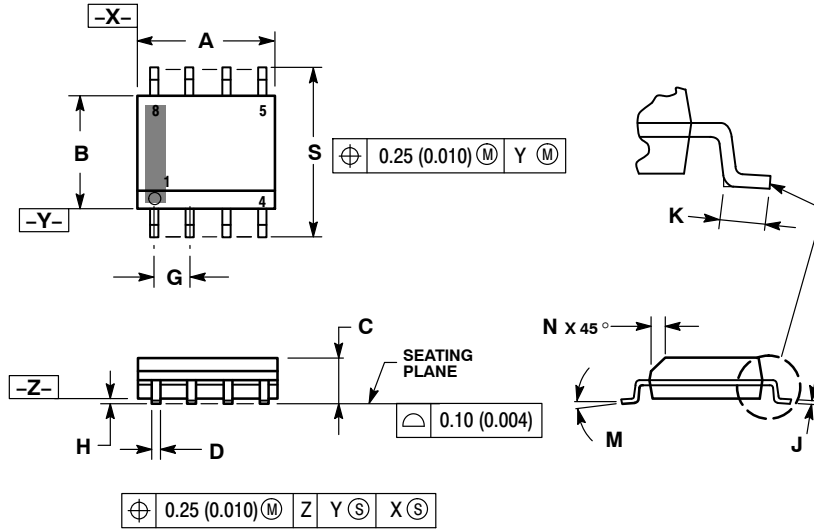
ON Semiconductor®



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|--|---|---|---|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:
Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative