MC14099B

8-Bit Addressable Latches

The MC14099B is an 8−bit addressable latch. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. For the MC14099B the input is a unidirectional write only port.

The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/$\overline{\text{Read}}$ or Chip Enable.

A Master Reset capability is available on both parts.

Features

- Serial Data Input
- Parallel Output
- Master Reset
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−Power Schottky TTL Load over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

ON Semiconductor®

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SOIC−16 WD
DW SUFFIX
CASE 751G

PIN ASSIGNMENT

Q7	1 ●	16	V_DD
RESET	2	15	Q6
DATA	3	14	Q5
WRITE DISABLE	4	13	Q4
A0	5	12	Q3
A1	6	11	Q2
A2	7	10	Q1
V_SS	8	9	Q0

MARKING DIAGRAM

16

14099BG
AWLYYWW

1

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MAXIMUM RATINGS (Voltages Referenced to V_SS)

Symbol	Parameter	Value	Unit
V_DD	DC Supply Voltage Range	−0.5 to +18.0	V
V_in, V_out	Input or Output Voltage Range (DC or Transient)	−0.5 to V_DD + 0.5	V
I_in, I_out	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_stg	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
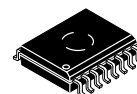1. Temperature Derating: "D/DW" Packages: −7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_in and V_out should be constrained to the range V_SS ≤ (V_in or V_out) ≤ V_DD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_SS or V_DD). Unused outputs must be left open.
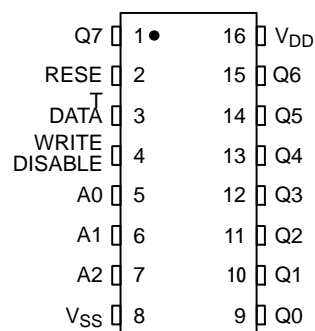
MC14099B

MC14099B
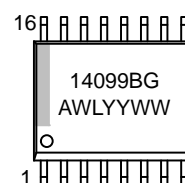

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
			10	–	3.0	–	4.50	3.0	–	3.0	
			15	–	4.0	–	6.75	4.0	–	4.0	
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
			10	7.0	–	7.0	5.50	–	7.0	–	
			15	11	–	11	8.25	–	11	–	
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	mAdc
			5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
			10	−1.6	–	−1.3	−2.25	–	−0.9	–	
			15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
			10	1.6	–	1.3	2.25	–	0.9	–	
			15	4.2	–	3.4	8.8	–	2.4	–	
Input Current		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Input Capacitance MC14599B — Data (pin 3) (V_{in} = 0)		C_{in}	–	–	–	–	15	22.5	–	–	pF
Quiescent Current (Per Package)		I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
			10	–	10	–	0.010	10	–	300	
			15	–	20	–	0.015	20	–	600	
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0	I_T = (1.5 μA/kHz) f + I_{DD}							μAdc
			10	I_T = (3.0 μA/kHz) f + I_{DD}							
			15	I_T = (4.5 μA/kHz) f + I_{DD}							

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.004.

MC14099B

**SWITCHING CHARACTERISTICS** (Note 5) (C$_L$ = 50 pF, T$_A$ = 25°C)

Characteristic	Symbol	V$_{DD}$ Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t$_{TLH}$, t$_{THL}$ = (1.35 ns/pF) C$_L$ + 32 ns t$_{TLH}$, t$_{THL}$ = (0.6 ns/pF) C$_L$ + 20 ns t$_{TLH}$, t$_{THL}$ = (0.4 ns/pF) C$_L$ + 20 ns	t$_{TLH}$, t$_{THL}$	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time Data to Output Q	t$_{PHL}$, t$_{PLH}$	5.0 10 15	– – –	200 75 50	400 150 100	ns
Write Disable to Output Q		5.0 10 15	– – –	200 80 60	400 160 120	ns
Reset to Output Q		5.0 10 15	– – –	175 80 65	350 160 130	ns
CE to Output Q (MC14599B only)		5.0 10 15	– – –	225 100 75	450 200 150	ns
Propagation Delay Time, MC14599B only Chip Enable, Write/$\overline{Read}$ to Data	t$_{PHL}$, t$_{PLH}$	5.0 10 15	– – –	200 80 65	400 160 130	ns
Address to Data		5.0 10 15	– – –	200 90 75	400 180 150	ns
Pulse Widths Reset	t$_{w(H)}$ t$_{w(L)}$	5.0 10 15	150 75 50	75 40 25	– – –	ns
Write Disable		5.0 10 15	320 160 120	160 80 60	– – –	ns
Set Up Time Data to Write Disable	t$_{su}$	5.0 10 15	100 50 35	50 25 20	– – –	ns
Hold Time Write Disable to Data	t$_h$	5.0 10 15	150 75 50	75 40 25	– – –	ns
Set Up Time Address to Write Disable	t$_{su}$	5.0 10 15	100 80 40	45 30 10	– – –	ns
Removal Time Write Disable to Address	t$_{rem}$	5.0 10 15	0 0 0	– 80 – 40 – 40	– – –	ns

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
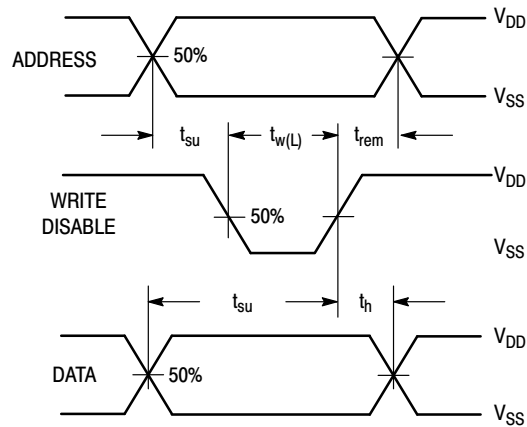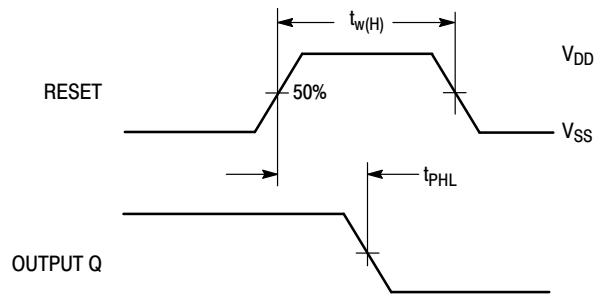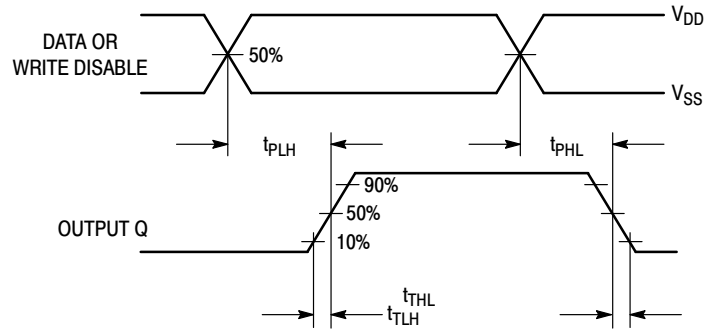
MC14099B

FUNCTION DIAGRAM
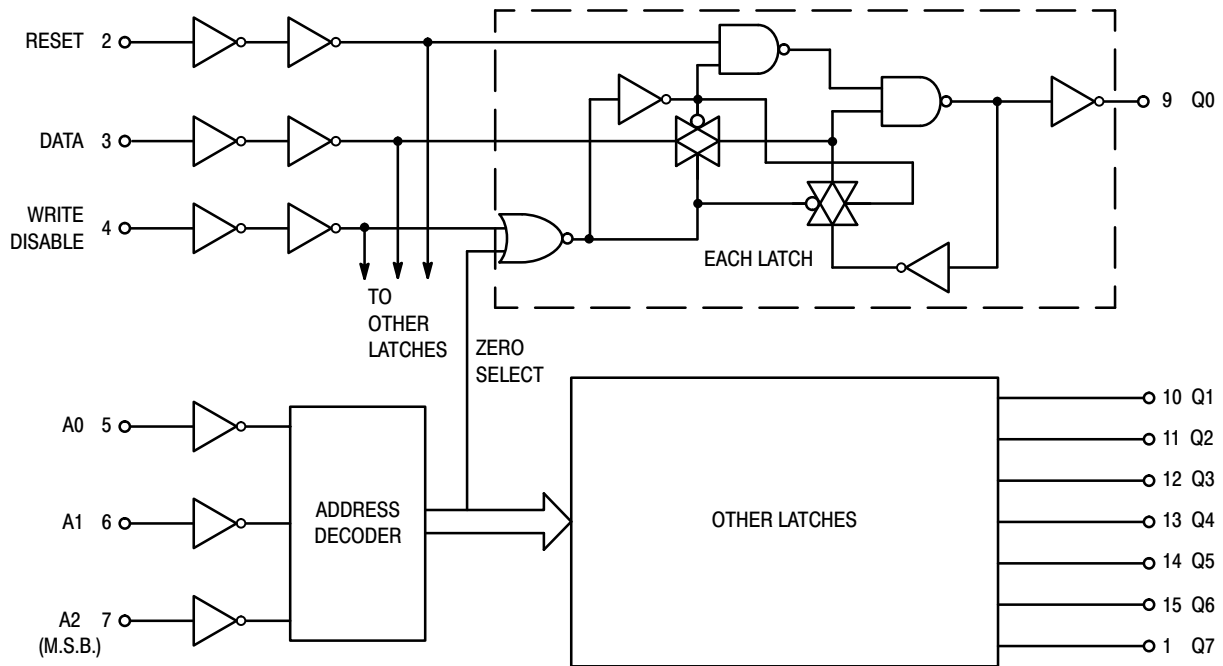
TRUTH TABLE

Write Disable	Reset	Addressed Latch	Unaddressed Latches
0	0	Data	Q_n*
0	1	Data	Reset †
1	0	Q_n*	Q_n*
1	1	Reset	Reset

*Q_n is previous state of latch.
†Reset to zero state.

CAUTION: To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

MC14099B

SWITCHING WAVEFORMS

DATA OR WRITE DISABLE — 50% — V_{DD} / V_{SS}

t_{PLH} t_{PHL}

OUTPUT Q — 90% 50% 10%

t_{THL}
t_{TLH}

$t_{w(H)}$

RESET — 50% — V_{DD} / V_{SS}

t_{PHL}

OUTPUT Q

ADDRESS — 50% — V_{DD} / V_{SS}

t_{su} $t_{w(L)}$ t_{rem}

WRITE DISABLE — 50% — V_{DD} / V_{SS}

t_{su} t_{h}

DATA — 50% — V_{DD} / V_{SS}

MC14099B

ORDERING INFORMATION

Device	Package	Shipping†
MC14099BDWG	SOIC−16 WB (Pb−Free)	47 Units / Rail
MC14099BDWR2G	SOIC−16 WB (Pb−Free)	1000 Units / Tape & Reel
NLV14099BDWR2G*	SOIC−16 WB (Pb−Free)	1000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

SOIC−16 WB
CASE 751G
ISSUE E

DATE 08 OCT 2021

1

SCALE 1:1

TOP VIEW

16   D   9

A

B

H   E

PIN 1
INDICATOR   1   8

16X B

e

⊕ 0.25 M B M

⊕ 0.25 M T A S B S

SIDE VIEW

SEATING
PLANE   T

A1   A

END VIEW

M

h
× 45°

DETAIL A

**DETAIL A
2X SCALE**

16X

L

C
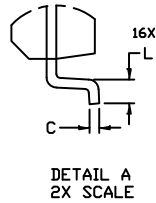
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
   ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS
   OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

DIM	MILLIMETERS	
	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°

16X 0.58

11.00

16X 1.62   1   1.27
PITCH

**RECOMMENDED
MOUNTING FOOTPRINT**

**GENERIC
MARKING DIAGRAM***

16

XXXXXXXXXXX
XXXXXXXXXXX
AWLYYWWG

1

XXXXX = Specific Device Code
A   = Assembly Location
WL   = Wafer Lot
YY   = Year
WW   = Work Week
G   = Pb−Free Package

*This information is generic. Please refer to
device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot "▪", may
or may not be present. Some products may
not follow the Generic Marking.

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PUBLICATION ORDERING INFORMATION

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