



# DDR3 SDRAM Reduced tFAW Addendum

## MT41J256M16 – 32 Meg x 16 x 8 Banks

### Features

- $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- Posted CAS additive latency (AL)
- Programmable CAS WRITE latency (CWL) based on tCK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- $T_C$  of 0°C to 95°C
  - 64ms, 8192 cycle refresh at 0°C to 85°C
  - 32ms, 8192 cycle refresh at 85°C to 95°C
- Self refresh temperature (SRT)
- Write leveling
- Multipurpose register
- Output driver calibration

### Options

- Configuration
  - 256 Meg x 16 256M16
- FBGA package (Pb-free) – x16
  - 96-ball (8mm x 14mm) HA
- Timing – cycle time
  - 938ps @ CL = 14 (DDR3-2133) -093
- Reduced tFAW
  - tFAW = 30ns<sup>1</sup> J
- Operating temperature
  - Commercial (0°C ≤ T<sub>C</sub> ≤ +95°C) None
- Revision :E

- Notes:
1. Standard DDR3-2133, 2KB page size, tFAW specification is 35ns.
  2. For complete device functionality and specifications, refer to the standard 4Gb DDR3 SDRAM data sheet found at [www.micron.com](http://www.micron.com). The information in this data sheet supersedes the standard data sheet.

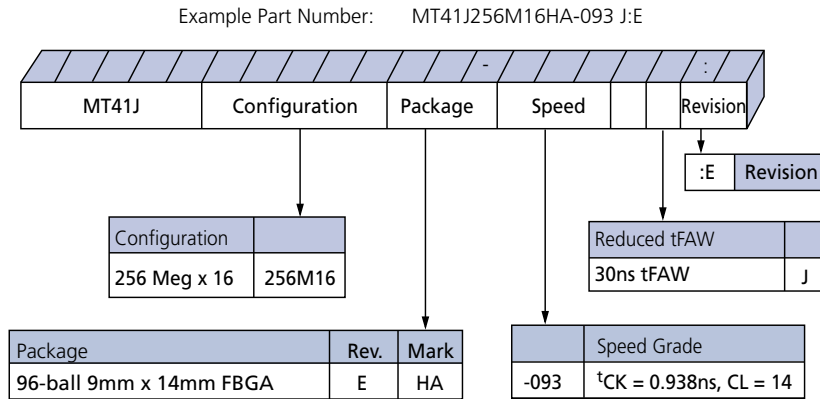
**Table 1: Key Timing Parameters**

Speed Grade	Data Rate (MT/s)	tFAW	Target tRCD-tRP-CL	tRCD (ns)	tRP (ns)	CL (ns)
-093	2133	30ns	14-14-14	13.09	13.09	13.09

**Table 2: Addressing**

Parameter	256 Meg x 16
Configuration	32 Meg x 16 x 8 banks
Refresh count	8K
Row addressing	32K (A[14:0])
Bank addressing	8 (BA[2:0])
Column addressing	1K (A[9:0])
Page size	2KB

**Figure 1: DDR3 Part Numbers**



Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on <http://www.micron.com> for available offerings.

## FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron’s Web site: <http://www.micron.com>.

## AC Timing Adjustments

**Table 3: Electrical Characteristics and AC Operating Conditions for Speed Extensions**

Notes 1–8 apply to the entire table

Parameter	Symbol	DDR3-2133		Unit	Notes
		Min	Max		
<b>Command and Address Timing</b>					
Four ACTIVATE windows	2KB page size	<sup>t</sup> FAW	30	–	ns 9

- Notes:
- AC timing parameters are valid from specified  $T_C$  MIN to  $T_C$  MAX values.
  - All voltages are referenced to  $V_{SS}$ .
  - Output timings are only valid for  $R_{ON34}$  output buffer selection.
  - The unit <sup>t</sup>CK (AVG) represents the actual <sup>t</sup>CK (AVG) of the input clock. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.
  - AC timing and  $I_{DD}$  tests may use a  $V_{IL}$ -to- $V_{IH}$  swing of up to 900mV in the test environment, but input timing is still referenced to  $V_{REF}$  (except <sup>t</sup>IS, <sup>t</sup>IH, <sup>t</sup>DS, and <sup>t</sup>DH use the AC/DC trip points and CK, CK# and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs (DQs are at 2V/ns for DDR3-1866 and DDR3-2133) and 2 V/ns for differential inputs in the range between  $V_{IL(AC)}$  and  $V_{IH(AC)}$ .
  - All timings that use time-based values (ns,  $\mu$ s, ms) should use <sup>t</sup>CK (AVG) to determine the correct number of clocks (Table 3 (page 3) uses CK or <sup>t</sup>CK [AVG] interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
  - Strobe or DQSDiff refers to the DQS and DQS# differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and CK# differential crossing point when CK is the rising edge.
  - This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is  $V_{DDQ}/2$  for single-ended signals and the crossing point for differential signals.
  - For these parameters, the DDR3 SDRAM device supports <sup>t</sup>nPARAM ( $nCK$ ) =  $RU(\text{<sup>t</sup>nPARAM [ns] / <sup>t</sup>CK[AVG] [ns]})$ , assuming all input clock jitter specifications are satisfied. For example, the device will support <sup>t</sup>nRP ( $nCK$ ) =  $RU(\text{<sup>t</sup>RP / <sup>t</sup>CK[AVG]})$  if all input clock jitter specifications are met. This means that for DDR3-800 6-6-6, of which <sup>t</sup>RP = 5ns, the device will support <sup>t</sup>nRP =  $RU(\text{<sup>t</sup>RP / <sup>t</sup>CK[AVG]}) = 6$  as long as the input clock jitter specifications are met. That is, the PRECHARGE command at  $T_0$  and the ACTIVATE command at  $T_0 + 6$  are valid even if six clocks are less than 15ns due to input clock jitter.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.