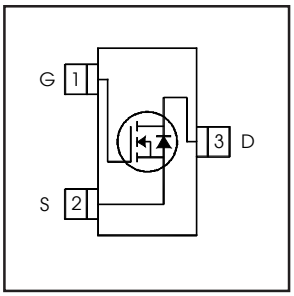
International
IOR Rectifier

PD - 91257E

IRLML2402

HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- N-Channel MOSFET
- SOT-23 Footprint
- Low Profile (<1.1mm)
- Available in Tape and Reel
- Fast Switching



V_{DSS} = 20V

$R_{DS(on)}$ = 0.25Ω

Micro3™

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

A customized leadframe has been incorporated into the standard SOT-23 package to produce a HEXFET Power MOSFET with the industry's smallest footprint. This package, dubbed the Micro3, is ideal for applications where printed circuit board space is at a premium. The low profile (<1.1mm) of the Micro3 allows it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 4.5V	1.2	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 4.5V	0.95	
I_{DM}	Pulsed Drain Current ①	7.4	
P_D@T_A = 25°C	Power Dissipation	540	mW
	Linear Derating Factor	4.3	mW/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	—	230	°C/W

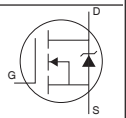
12/14/11

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.024	–––	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	0.25	Ω	V_{GS} = 4.5V, I_D = 0.93A ③
		–––	–––	0.35		V_{GS} = 2.7V, I_D = 0.47A ③
$V_{GS(th)}$	Gate Threshold Voltage	0.70	–––	–––	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	1.3	–––	–––	S	V_{DS} = 10V, I_D = 0.47A
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	1.0	µA	V_{DS} = 16V, V_{GS} = 0V
		–––	–––	25		V_{DS} = 16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	-100	nA	V_{GS} = -12V
	Gate-to-Source Reverse Leakage	–––	–––	100		V_{GS} = 12V
Q_g	Total Gate Charge	–––	2.6	3.9	nC	I_D = 0.93A
Q_{gs}	Gate-to-Source Charge	–––	0.41	0.62		V_{DS} = 16V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	1.1	1.7		V_{GS} = 4.5V, See Fig. 6 and 9 ③
$t_{d(on)}$	Turn-On Delay Time	–––	2.5	–––	ns	V_{DD} = 10V
t_r	Rise Time	–––	9.5	–––		I_D = 0.93A
$t_{d(off)}$	Turn-Off Delay Time	–––	9.7	–––		R_G = 6.2Ω
t_f	Fall Time	–––	4.8	–––		R_D = 11Ω, See Fig. 10 ③
C_{iss}	Input Capacitance	–––	110	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	51	–––		V_{DS} = 15V
C_{rss}	Reverse Transfer Capacitance	–––	25	–––		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	0.54	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	7.4		
V_{SD}	Diode Forward Voltage	–––	–––	1.2	V	T_J = 25°C, I_S = 0.93A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	–––	25	38	ns	T_J = 25°C, I_F = 0.93A
Q_{rr}	Reverse RecoveryCharge	–––	16	24	nC	di/dt = 100A/µs ③



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② I_{SD} ≤ 0.93A, di/dt ≤ 90A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C

③ Pulse width ≤ 300µs; duty cycle ≤ 2%.

④ Surface mounted on FR-4 board, t ≤ 5sec.

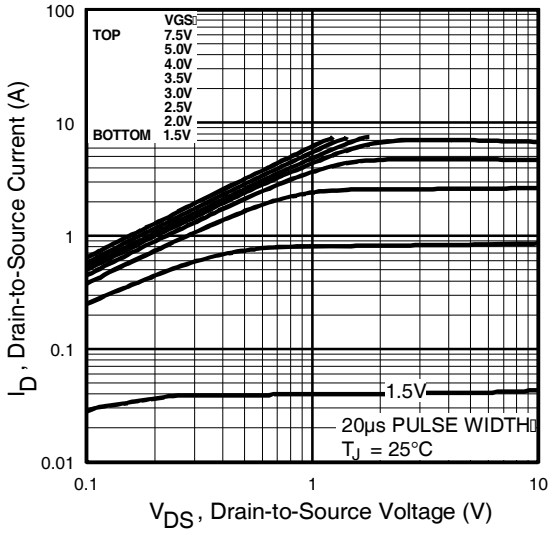


Fig 1. Typical Output Characteristics

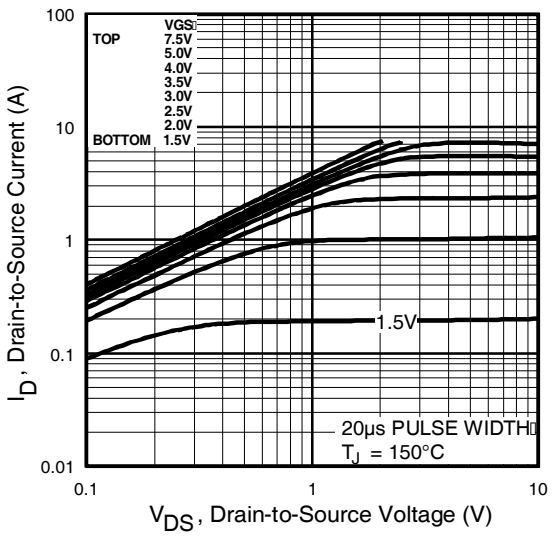


Fig 2. Typical Output Characteristics

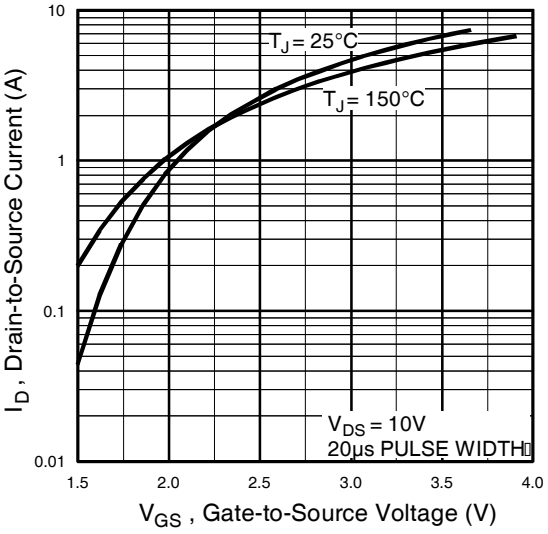


Fig 3. Typical Transfer Characteristics

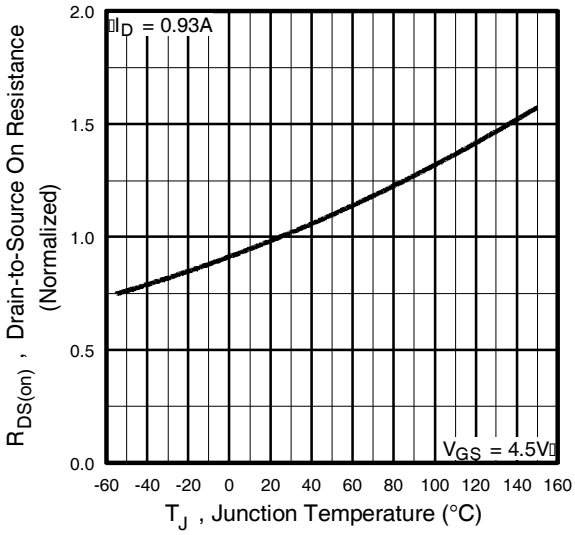


Fig 4. Normalized On-Resistance Vs. Temperature

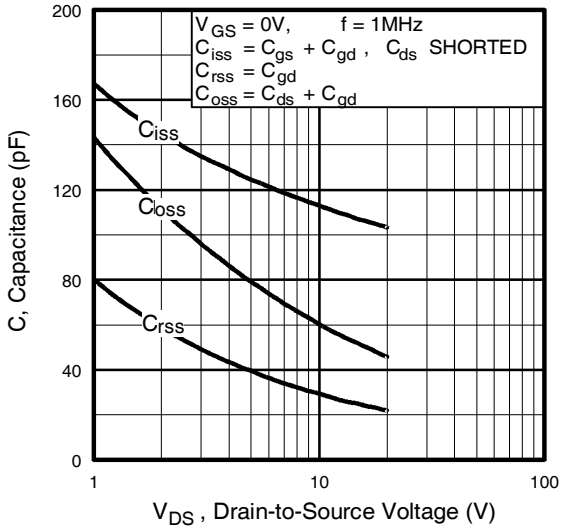


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

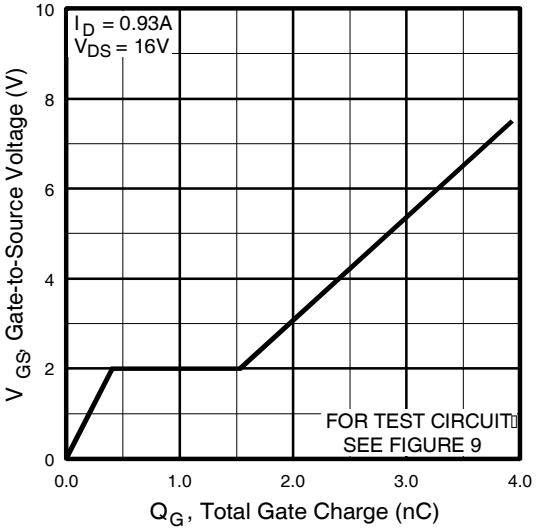


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

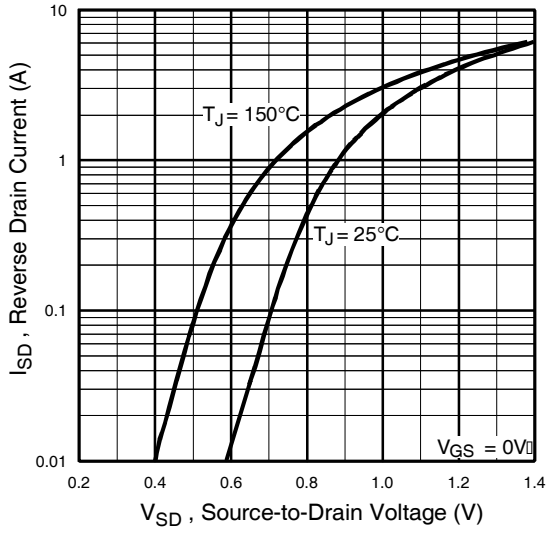


Fig 7. Typical Source-Drain Diode Forward Voltage

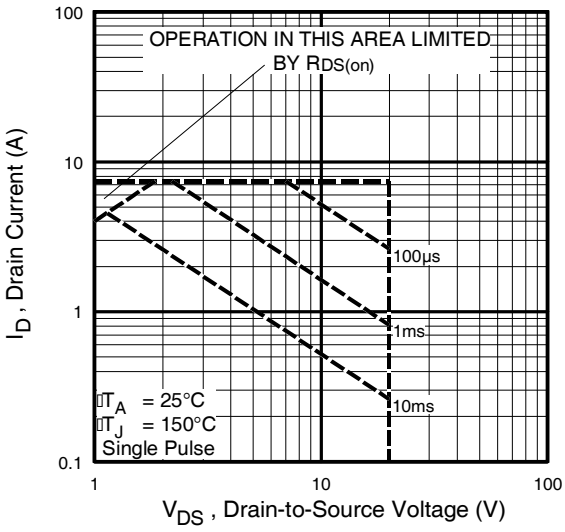


Fig 8. Maximum Safe Operating Area

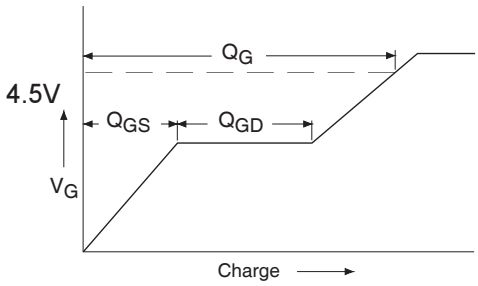


Fig 9a. Basic Gate Charge Waveform

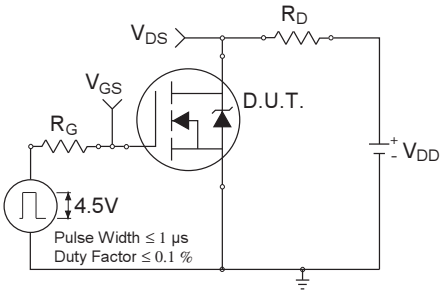


Fig 10a. Switching Time Test Circuit

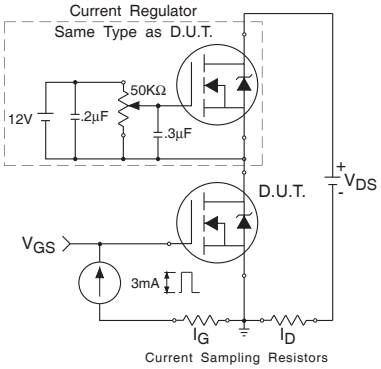


Fig 9b. Gate Charge Test Circuit

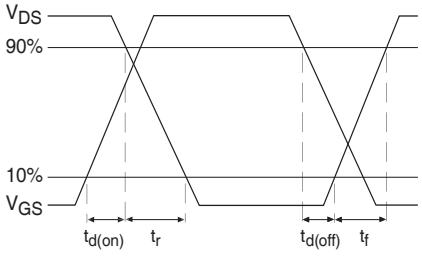


Fig 10b. Switching Time Waveforms

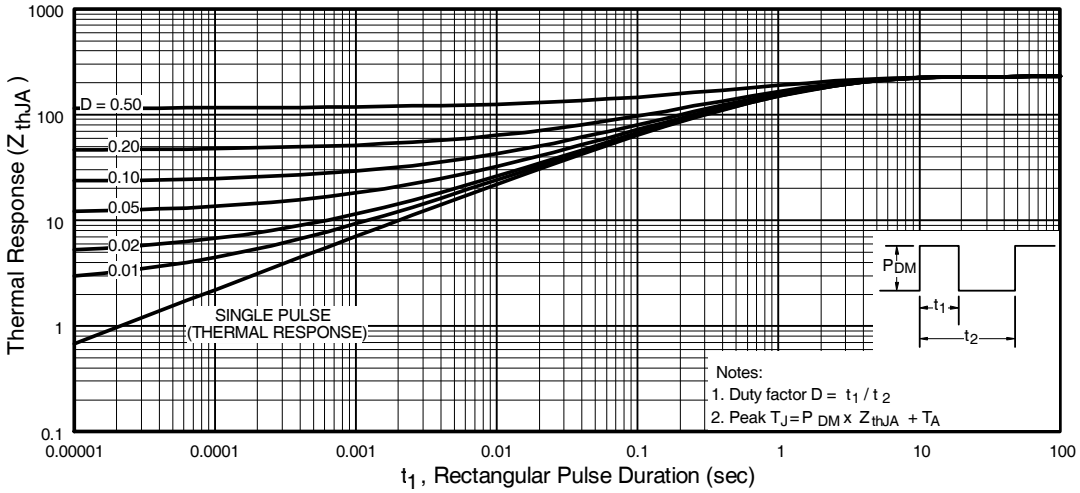
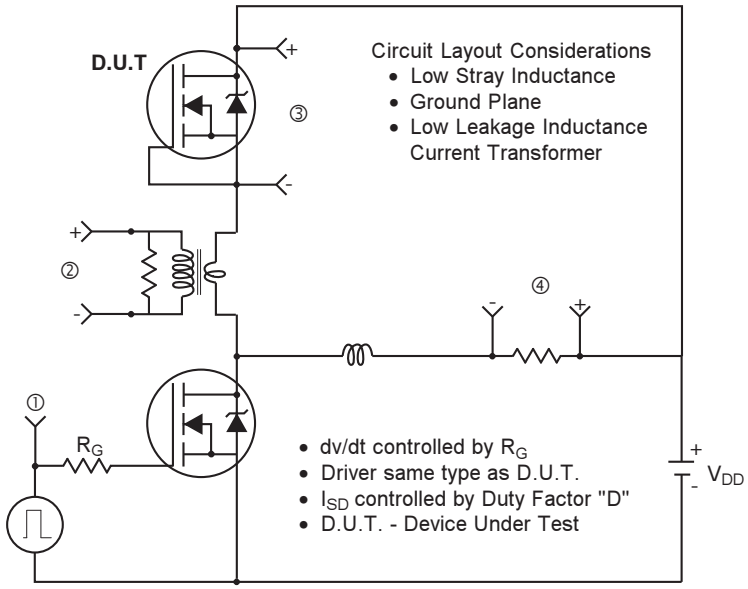
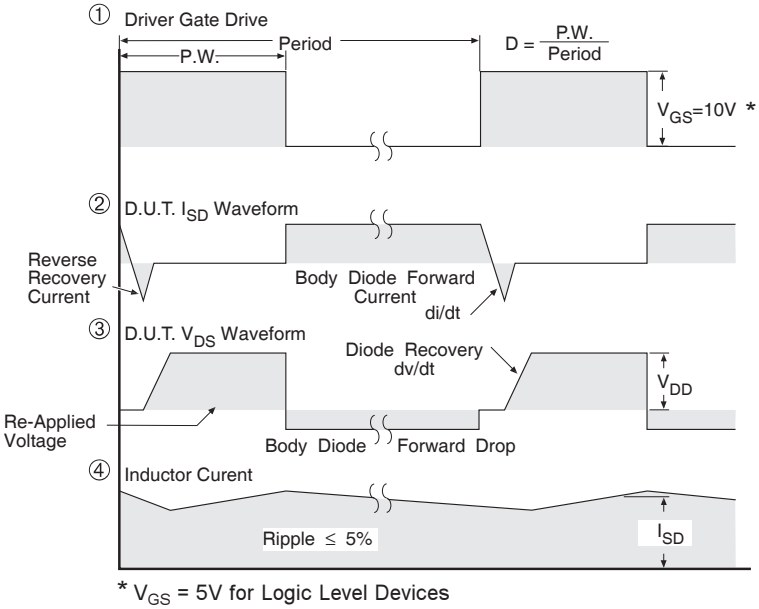


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Peak Diode Recovery dv/dt Test Circuit



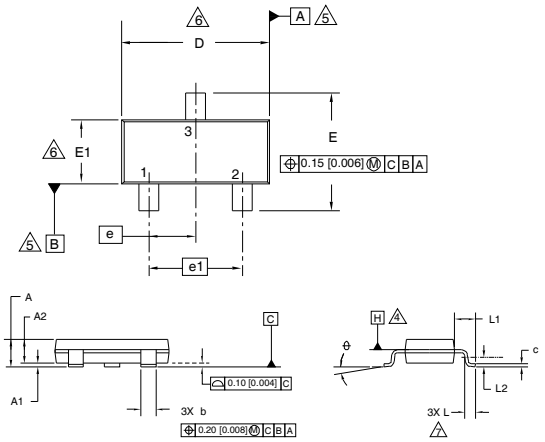


* V_{GS} = 5V for Logic Level Devices

Fig 12. For N-Channel HEXFETS

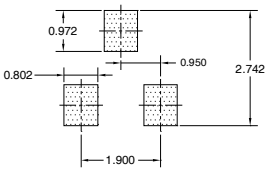
Micro3 (SOT-23) (Lead-Free) Package Outline

Dimensions are shown in millimeters (inches)



DIMENSIONS				
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.89	1.12	0.035	0.044
A1	0.01	0.10	0.0004	0.004
A2	0.88	1.02	0.035	0.040
b	0.30	0.50	0.012	0.020
c	0.08	0.20	0.003	0.008
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E1	1.20	1.40	0.047	0.055
e	0.95	BSC	0.037	BSC
e1	1.90	BSC	0.075	BSC
L	0.40	0.60	0.016	0.024
L1	0.54	REF	0.021	REF
L2	0.25	BSC	0.010	BSC
θ	0	8	0	8

Recommended Footprint

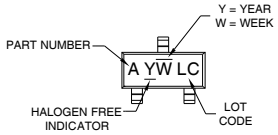


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: MILLIMETER.
4. DATUM PLANE H IS LOCATED AT THE MOLD PARTING LINE.
5. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
6. DIMENSIONS D AND E1 ARE MEASURED AT DATUM PLANE H. DIMENSIONS DOES NOT INCLUDE MOLD PROTRUSIONS OR INTERLEAD FLASH. MOLD PROTRUSIONS OR INTERLEAD FLASH SHALL NOT EXCEED 0.25 MM [0.010 INCH] PER SIDE.
7. DIMENSION L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-236 AB.

Micro3 (SOT-23 / TO-236AB) Part Marking Information

Micro3 / SOT-23 Package Marking



PART NUMBER CODE REFERENCE:

A = IRLML2402
B =IRLML2803
C = IRLML2402
D = IRLML5103
E = IRLML6402
F = IRLML6401
G = IRLML2502
H = IRLML5203

Note: A line above the work week
(as shown here) indicates Lead-free

W = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5		
2006	6		
2007	7		
2008	8		
2009	9		
2010	0	24	X
		25	Y
		26	Z

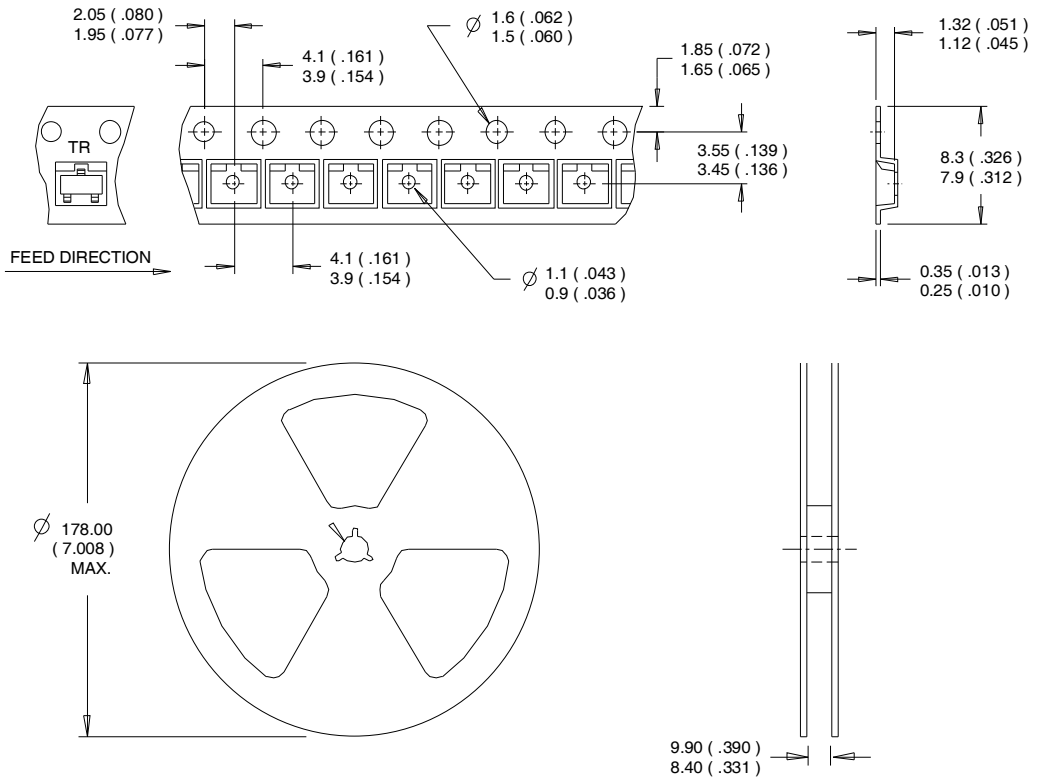
W = (27-52) IF PRECEDED BY A LETTER

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E		
2006	F		
2007	G		
2008	H		
2009	J		
2010	K	50	X
		51	Y
		52	Z

Note: For the most current drawing please refer to IR website at http://www.irf.com/package

Micro3™ Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package

Data and specifications subject to change without notice.

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